PRELIMINARY

VF1 FPGA Family

FEATURES AND BENEFITS

- **The industry's first Variable-Grain-Architecture™ enables high-density, high-performance designs for a wide range of applications**
  - — Architecture adapts to logic to enable synthesis-friendly, high-performance designs
  - — From three to six parallel inputs with all possible input combinations decoded in a single level of high-speed logic
  - — Up to 32 parallel input functions with a subset of input combinations decoded in only two logic levels
  - — Available in four sizes with 12K, 20K, 25K, and 36K gates
- **Variable-Length-Interconnect™ delivers predictable performance and First-Time-Fit™ layouts**
  - — High-speed direct connectivity minimizes connection lengths for maximum performance
  - — Variable-length connections span from two logic blocks to the entire chip, including I/Os
  - — Result is optimal length resource for every net
- **Flexible on-chip clocking options deliver up to 250MHz performance**
  - — Four low-skew global clocks minimize clock variations within the chip
  - — Two on-chip phase-locked loops (PLLS) synchronize on-chip clocks with the system clock
  - — PLLs provide 1x, 2x, and 3x frequency multiplication for on-chip clock synthesis
  - — Clocks generated on-chip may be used as global clocks
- **Vantis' hierarchical design methodology and DesignDirect™ software provide Ease-of-Success™ and First-Time-Fit**
  - — DesignDirect software supports Verilog and VHDL hardware description languages (HDLs) for design flexibility
  - — Integrates easily with a variety of third-party front-end design entry, simulation, and synthesis tools
  - — Easy-to-learn mapping and layout software coupled with fast run times and superior quality of results contribute to maximum productivity
  - — Vantis design software ensures First-Time-Fit results by examining a design prior to the place-and-route phase and determining whether or not it will fit into the chosen VF1™ FPGA
- **Pin-locking feature ensures that I/O pin assignments will not change when moving a design from one VF1 FPGA size to another or when making design changes**
  - — When making design changes or shifting density, special routing logic enables pin-locking with minimal performance degradation
  - — Allows shifting to higher or lower density FPGA without making changes to board layout
- **Zero-power Edge Connect lines allow easy implementation of NOR functions on input lines**
  - — Eight Edge Connect lines—two per side of the chip
  - — Input pins may be connected to these lines to implement NOR functions
  - — NOR functions consume zero power

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- **High-speed embedded dual-port memory simplifies the implementation of on-chip FIFOs and RAM**
  - — Needs fewer bits than single-port architectures to implement FIFOs and register stacks
  - — Minimizes access time for both read and write cycles
  - — Over 6K bits of embedded SRAM in the largest VF1 FPGA device in 32x4 configurable blocks
  - — Specific configurations may be defined by the user
- **Flexible I/O buffers allow interfacing to a wide variety of systems**
  - — I/O buffers are compatible with both 3.3V and 5V I/O levels
  - — Programmable slew rates reduce output signal over/under shoot
  - — Three-state control for I/O bus interconnections allow multiplexing on long interconnect lines
  - — PCI-compatible I/Os, coupled with optional 33MHz and 66MHz PCI buffers, allow easy interfacing to PCI buses
- **In-system programming via the built-in JTAG boundary scan port**
  - — Allows VF1 FPGAs to be programmed after mounting on a printed-circuit board
  - — Reduces the need for on-board SPROM
  - — When coupled with pin-locking, allows design changes to be made and loaded without removing the device from the board
- **Outperforms systems implemented with competitive reprogrammable FPGAs by 67% to 100%**
  - — High-performance registered I/O improves chip speed
  - — On-chip phase-locked loops with the ability to double or triple input clocks, up to 200 MHz, allows the Vantis FPGA to run up to three times faster than the system clock
  - — Embedded memory has 5ns read/write access time for fast loads and stores
  - — Pipelined logic capable of 250 MHz operation supports the development of high-performance systems

Table 1. Available Devices in the VF1 Family

Features	VF1012	VF1020	VF1025	VF1036
Typical gates	12,000	20,000	25,000	36,000
Array size (VGB)	14x14	18x18	20x20	24x24
Logic flip-flops	784	1296	1600	2304
DPSRAM blocks (32x4)	28	36	40	48
Total RAM bits	3584	4608	5120	6144
Clock pins	4	4	4	4
Maximum I/Os	168	216	240	288
Maximum I/O flip-flops	336	432	480	576

Table 2. Package Types and Total I/O Pins (including clock pins)

Packages	VF1012	VF1020	VF1025	VF1036
352 BGA			244	292
256 BGA	172	208	208	208
208 PQFP	168	168	168	168
160 PQFP	128	128		
144 TQFP	112			

OPERATIONAL DESCRIPTION

The Vantis VF1 FPGA family offers FPGA designers a level of performance that was once available only to ASIC gate array designers. The VF1's Variable-Grain-Architecture minimizes the logic and interconnect resources needed to implement high-performance, complex functions. It supports logic configurations with three to six logic inputs with all possible input combinations decoded in a single LUT (look-up table) level. It also supports configurations with up to thirty-two partially-decoded parallel inputs that use only two LUT levels.

Coupled with high-performance Variable-Length-Interconnect (VLI) and from 3.6K to 6.1K bits of embedded dual-port SRAM, the Variable-Grain-Architecture delivers the best performance in the FPGA industry in a cost-effective solution that virtually guarantees design success.

Superior performance coupled with densities from 12K to 36K logic gates makes the Vantis VF1 family the best choice for high-performance, complex FPGA-based designs. Designers who create high-performance, high-density designs typically employ a design methodology based on hardware description languages (HDLs) such as Verilog or VHDL to speed the design process and manage complexity. The Vantis design methodology employs third-party HDL design tools coupled with Vantis' physical mapping and layout software.

The VF1 overview that follows describes a new, sophisticated FPGA architecture that includes a rich set of building blocks and interconnect resources. The VF1 family is manufactured in a state-of-the-art deep-submicron 0.18-micron ($L_{effective}$) process technology for high performance and small die size. It uses four layers of metal interconnect to further enhance performance, reduce die size, and lower cost.

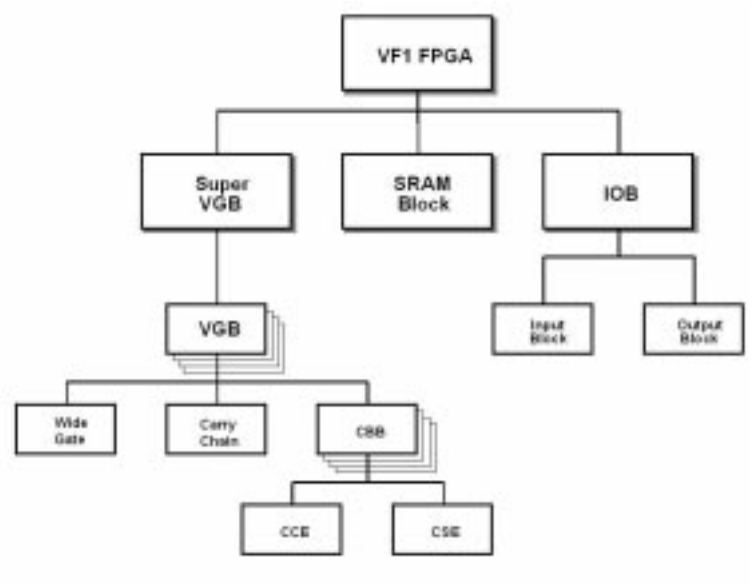
Variable-Grain-Architecture

The VF1 FPGA family employs a new variable-granularity architecture that allows virtually any level of logic complexity to be implemented using minimum chip resources. It comprises three levels of logic hierarchy (Figure 1):

Top Level: Super Variable-Grain-Block (Super VGB), SRAM, and I/O Block (IOB). The highest level building block in the VF1 architecture is the Super VGB. It is a symmetrical structure, made up of four VGBs, that can be combined to create complex, high-performance functions using local building blocks and local interconnect resources. Supporting Super VGBs at the top level are dual-port embedded SRAM and input/output blocks.

Second Level: Variable-Grain-Block (VGB). The next level, the VGB, includes four CBBs, logic to combine two or more CBBs to implement wide logic functions. Wide-gating logic supports complex functions with up to sixteen parallel inputs within a single VGB. The VGB also includes high-speed carry logic to build high-performance arithmetic functions and common control logic.

Configurable Building Blocks (CBB). The CBB is the lowest level building block. It includes six logic inputs, two 8-bit look-up tables (LUTs) to define logic functions, a flip-flop to save results, selectable outputs, and interconnections to other FPGA resources. A single CBB can implement two 3-input functions or one 4-input function using only the logic within the CBB.

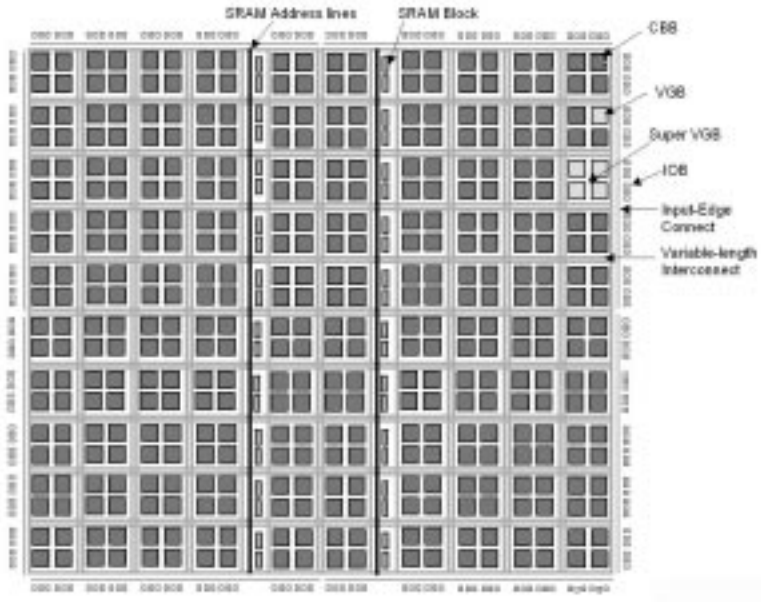


VF1ds-001

Figure 1. VF1 Family Architecture Hierarchy

A VF1 FPGA (Figure 1) is arranged in a matrix of Super VGBs, separated by routing channels made up of interconnect resources called Variable-Length-Interconnect. Figure 2 shows the architecture of the VF1025 FPGA. The VF1025 consists of a 20x20 matrix of VGBs with two columns of embedded SRAM running vertically near the center of the device. Each column of SRAM is supported by dedicated SRAM address lines.

There are three IOBs for each row and column of VGBs on each side of the chip. The VF1025, therefore, has 60 IOBs per side, giving a total of 240 IOBs for the device. Two input Edge Connect lines on each side of the device (eight lines total) may be connected to their adjacent IOBs to implement an input NOR function. The Edge Connect lines consume no power, even when implemented as a NOR function



VF1ds-002

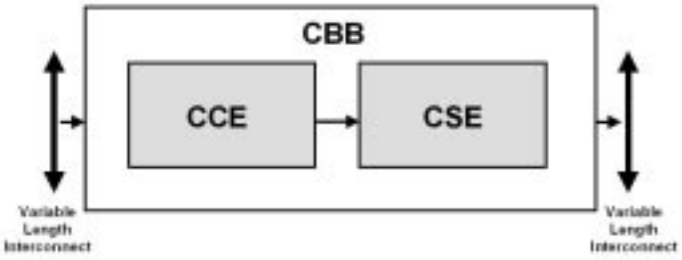
Figure 2. VF1 FPGA Architecture (VF1025 Shown)

A VGB in a VF1 FPGA corresponds roughly to one of the coarse-grained logic blocks found in competitive FPGA products—but a VGB is much more flexible. Its four CBBs can work independently as fine-grained elements to implement simple logic functions while using minimum resources, or they can be combined within the VGB and with other VGBs to handle very complex functions.

The following sections describe the VF1 architecture, starting at the CBB level and moving up the hierarchy.

CBB

A CBB consists of two parts: a configurable combinatorial element (CCE) and a configurable sequential element (CSE) (Figure 3). In general terms, the CCE receives logic inputs and generates outputs. The CSE stores and routes the outputs.

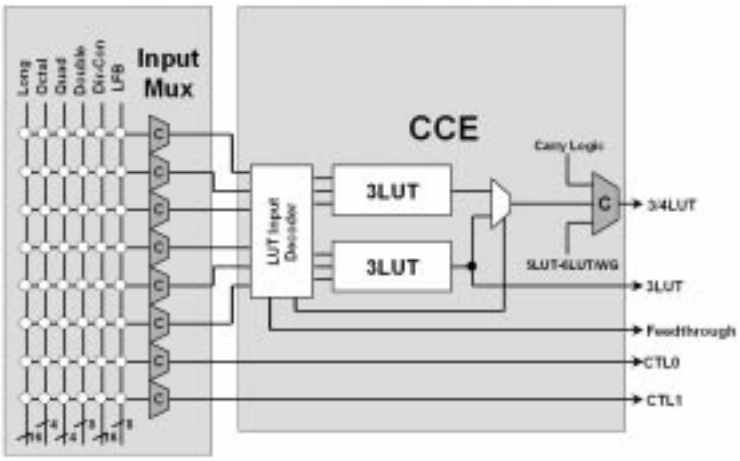


VF1ds-003

Figure 3. Configurable Building Block (CBB)

A CCE (Figure 4) contains two 8-bit, three-input look-up tables (3LUTs). The CCE receives inputs via VF1 Variable-Length-Interconnect routing resources, direct connections from adjacent VGBs, and local feedback within the VGB. (Inputs are covered in more detail later.) A LUT input decoder routes the inputs to the LUTs. The LUT input decoder spans all four CBBs in a VGB to enable the combining of CBBs to create five- and six-input functions. These wider functions are described later.

Bit patterns loaded into the LUTs define the output generated by each input combination.



VF1ds-004

Figure 4. Configurable Combinatorial Element (CCE)

Note:
A C in a mux block indicates that the block's function is set by the VF1 configuration bitstream and is not a logical block that can be controlled dynamically

The two 3LUTs may generate individual outputs (Figure 4), or they may be combined into a 16-bit 4LUT that decodes four inputs (Figure 5). If the 3LUTs operate independently, one output follows the Feedthrough route to the CBB output while the other goes to the following CSE via the 3/4LUT path shown in Figure 4.

The Feedthrough line coming from the Input Switch is a special high-speed path that allows long-line routing resources to be routed from one line to another without going through a long-line switch matrix. The Feedthrough path provides better performance than the switch matrix path. This is covered in the *VGB Interconnect* section.

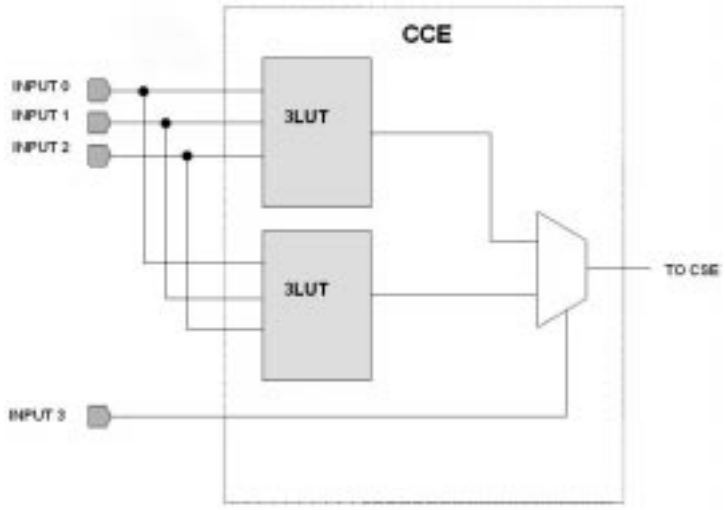


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Figure 5. Four-Input CCE Configuration

The CSE (Figure 6) receives the outputs from the CCE via the top mux on the left (along with Carry Logic, CCE, and Wide Gating inputs) and the Feedthrough line on the bottom left. The top mux output may be stored in the CSE register or it may bypass the register and go directly to an output via a second mux. The output of the second mux goes to a direct connect line that connects to other VGBs and IOBs, and to a local feedback (LFB) line that connects to other CBBs within the same VGB.

The Feedthrough line from the lower 3LUT can be routed to VLI resources and to a second LFB line.

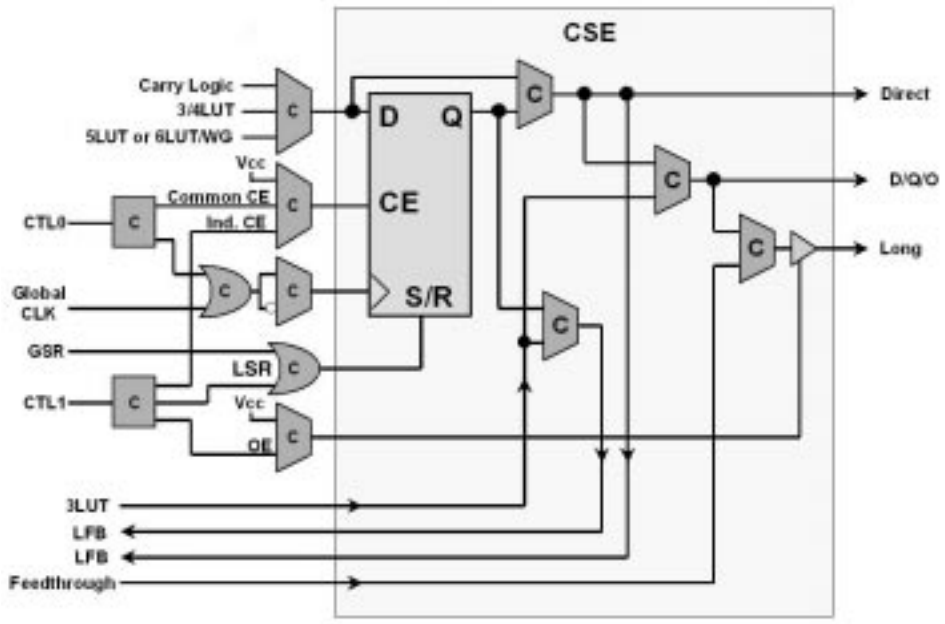

Figure 6. Configurable Sequential Element (CSE)

CSE register control signals consist of a clock enable (CE), a clock, and a direct set/reset. The register clock enable may be a common enable, a separately generated independent enable, or it may be tied to V_{cc}.

Both the register clock (CLK) and the set/reset signal (S/R) may be configured to meet specific design requirements. The polarity of the clock can be selected by configuring the mux that precedes the clock input to the register. The set/reset source may be configured as either local (LSR) or global (GSR). If a local set/reset is selected, it applies to all the registers in one VGB.

The Feedthrough line can be routed to a long interconnect line via a dedicated driver. The driver can be enabled by either being tied to V_{cc} or by a locally-generated output enable (OE). This function allows a signal from a long interconnect line to enter a Super VGB via a CBB input, bypass CBB logic, and connect directly to a shared Super VGB long-line driver. The long-line driver connects the signal to another long interconnect line. This is an alternative to using a switch at an intersection of long lines. It adds additional drive to the signal, allows the signal to be connected to lines that are parallel to the original line as well as perpendicular, and may have less delay than a switch at a line intersection.

VGB

The second level in the VF1 FPGA family hierarchy is the Variable-Grain-Block, or VGB (Figure 7). A VGB contains four CBBs plus common control functions, wide gating logic, and high-speed carry logic.

A VGB is a very flexible structure that can be combined in a variety of ways to create very simple or very complex logic structures. A VGB can be viewed as a fine-grained architecture when each CBB is used to implement a separate logic function. It becomes a coarse-grained architecture when the entire VGB is dedicated to a single function.

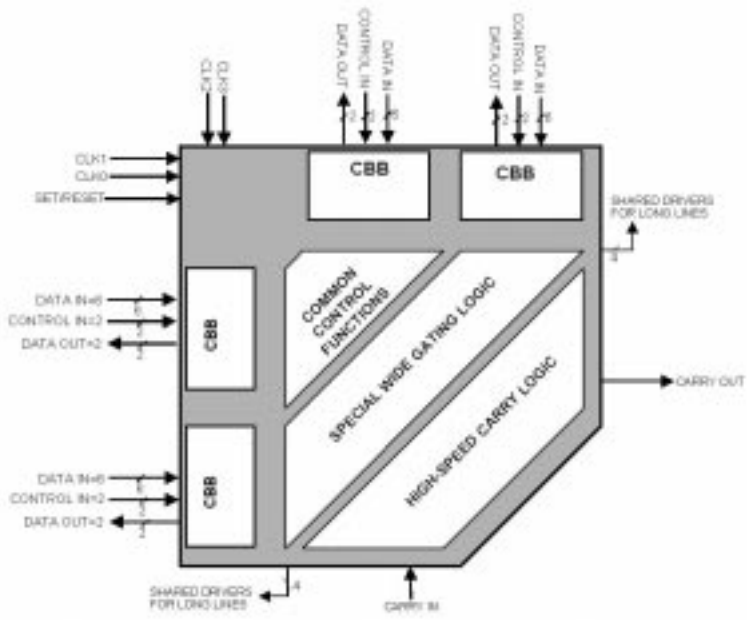

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Figure 7. Variable-Grain-Block (VGB)

Just as the LUTs within a single CBB can be combined to create complex functions, the CBBs within a VGB can be combined. By combining the four 8-bit 3LUTs in two CBBs into a single 32-bit 5LUT, all possible combinations of five logic inputs can be decoded (Figure 8). By combining all four CBBs in a VGB into a single 64-bit 6LUT, all possible combinations of six inputs can be decoded (Figure 9). The combined output becomes an input to one of the CSEs (Figure 6, upper-left mux).

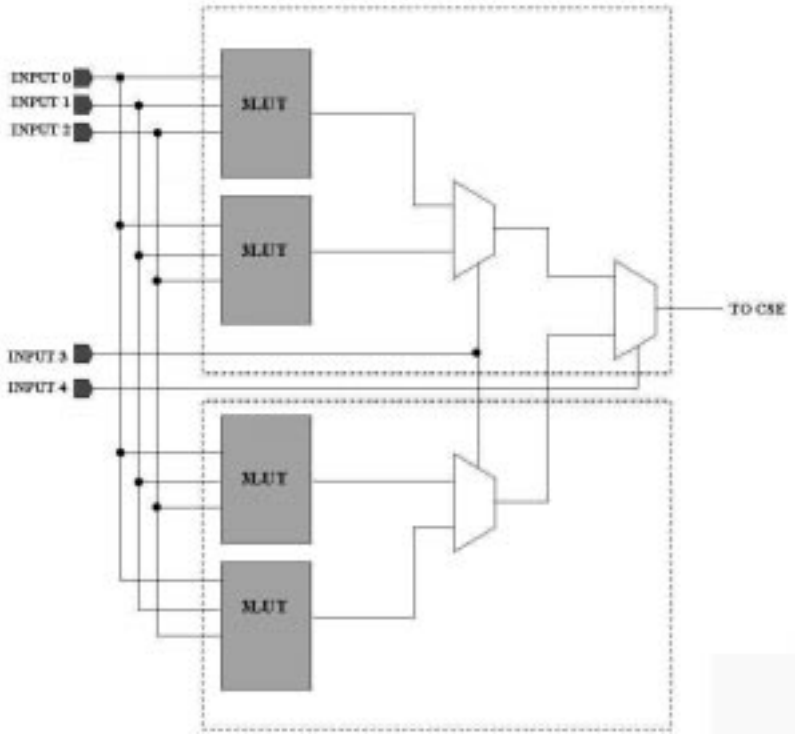

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Figure 8. Five-Input Function Using Two CBBs

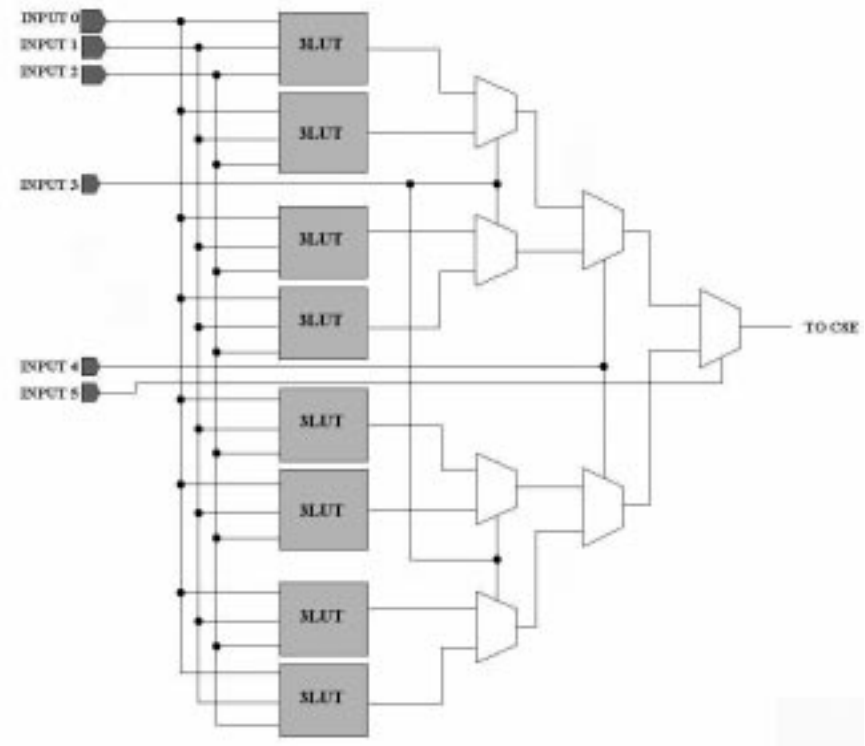

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Figure 9. Six-Input Function Using Four CBBs in One VGB

Figure 10 shows some of the possible fully-decoded combinations that can be implemented in a single VGB. The left VGB in Figure 10 shows some combinations that are possible without combining CBBs. A single VGB can implement eight three-input functions, or four four-input functions, or four three-input functions plus two four-input functions. Other combinations are also possible.

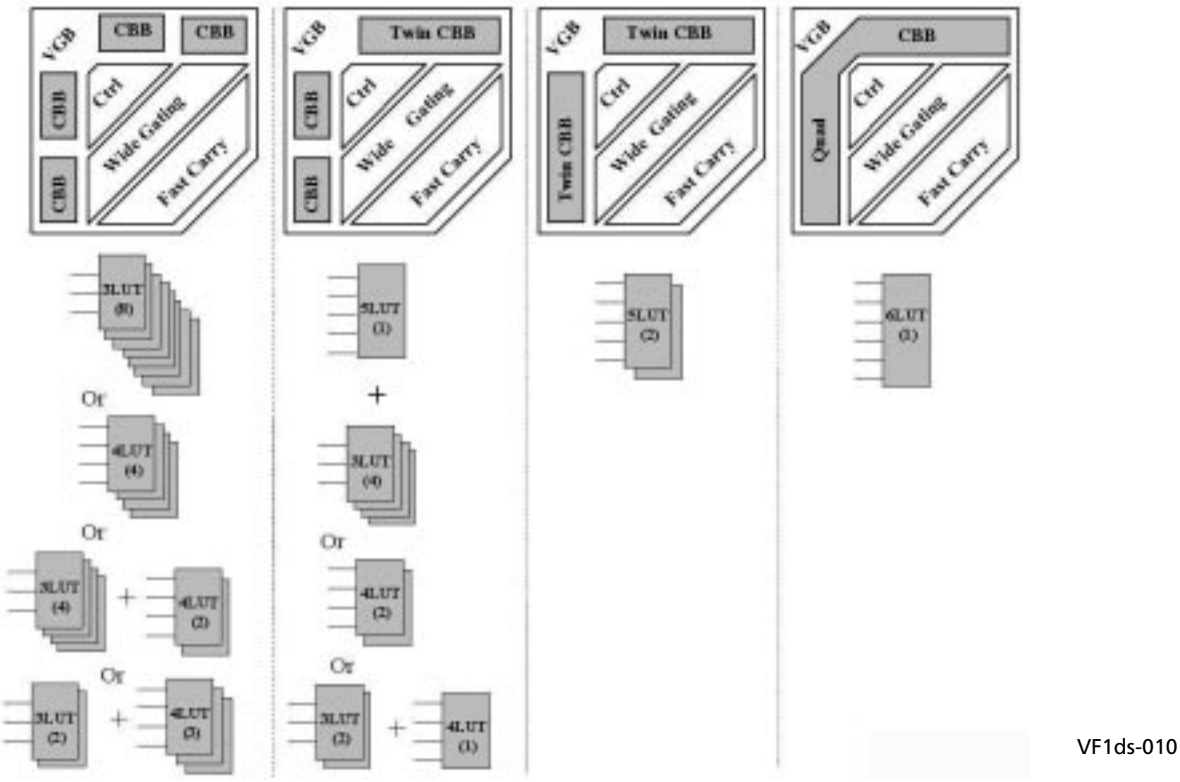

Figure 10. Examples of Logic Configurations in One VGB

The second VGB in Figure 10 shows some possible combinations when two CBBs are combined while two CBBs function independently. The combined CBBs form a 5LUT that implements a five-input function, while the independent CBBs implement various combinations of three- and four-input functions. The third VGB is configured for two five-input functions, and the fourth is configured for a single six-input function.

In many cases, however, an application does not require the decoding of every possible combination of a set of inputs. In these cases, configuring CBBs in combinations other than those described above can save device resources. For example, two CBBs may be configured as separate 4-input elements with their outputs multiplexed to decode an 8-input function using only two CBBs. Since each CBB decodes 16 combinations of four inputs, this configuration decodes 32 possible combinations of eight inputs.

Special wide-gating logic that is part of the VGB architecture is used to implement configurations up to 32 inputs in only two logic levels. The wide gating logic includes a dedicated 4LUT that is used to combine CBBs into functions with up to sixteen inputs using all four CBBs in one VGB (Figure 11). In this example, each CBB within a VGB is configured to fully decode four inputs.

Each of the four CBBs generates an output that becomes an input to the 4LUT in the wide gating logic. The 4LUT fully decodes the four inputs from the CBBs.

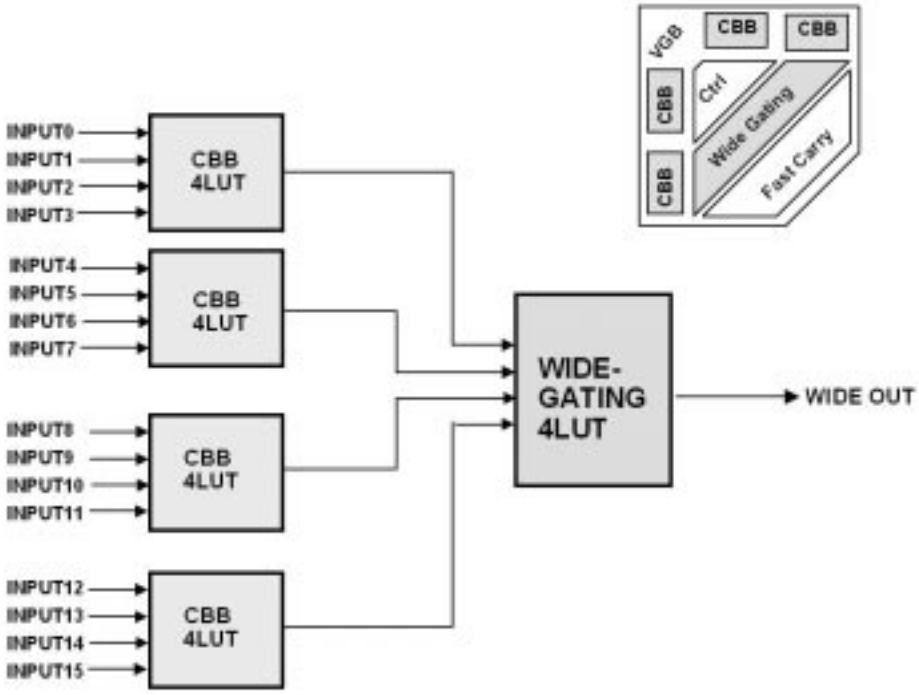

Figure 11. Decoding 16-Input Function Using Wide Gating Logic

The configuration in Figure 11 does not decode all 65,536 possible combinations of sixteen inputs. Instead, it decodes sixteen combinations of four inputs in each CBB for a total of 64 possible combinations. The wide-gating 16-bit LUT decodes sixteen possible combinations. The circuit, therefore, decodes 1024 combinations (16*64). For most logic functions this is quite adequate, and it is accomplished using only the high-speed, short-intraconnect logic contained in a single VGB.

Super VGB

The third hierarchical level is the Super VGB (Figure 12). It consists of four mirrored VGBs with four sets of shared long-connect multiplexers/drivers. The symmetrical arrangement of the Super VGB improves logic density and minimizes interconnect length for implementing complex functions. Inputs can come from any direction on the chip and outputs can go in any direction. Compared to architectures that force logic paths to flow in one general direction, this Super VGB symmetry shortens signal paths and thus improves both performance and density.

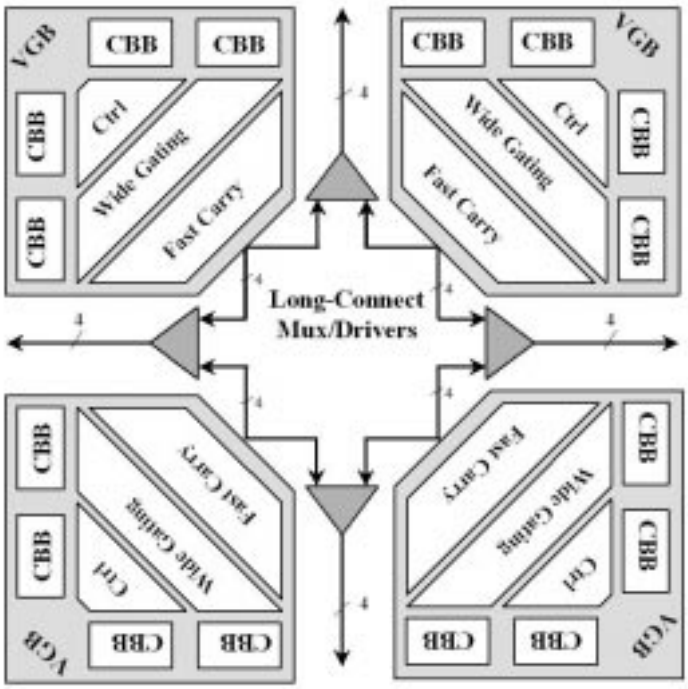

Figure 12. Super VGB Architecture

Each Super VGB has four sets of shared drivers, each set pointing in a different direction on the chip. These drivers allow a Super VGB to connect to the VLI lines (see *Interconnecting VGBs*) that provide general signal routing throughout the chip. Each set of shared drivers contains four individual drivers for a total of sixteen drivers in each Super VGB.

In addition to general interconnection of VGBs to long interconnect lines, the shared drivers are used to implement logic functions with up to 32 parallel inputs. Two 16-input functions (Figure 11) can be multiplexed using a shared driver, thus providing a 32-input function that decodes 2,048 possible conditions.

Interconnect Resources

In today's deep-submicron technologies, interconnect length often has a greater impact on device performance than gate or logic-block delays. The Vantis VF1 family minimizes most interconnect delays by providing multiple levels of interconnect resources that often allow complex functions to be implemented completely within a VGB or Super VGB. These complex functions, however, must be connected to other VGBs and to I/O blocks, therefore longer routing resources are needed.

The VF1 architecture provides three levels of high-performance interconnect resources:

- **Local feedback** allows CBB outputs to feed back to the inputs of all CBBs within the same VGB.
- **Inter-VGB Direct connect** routes the outputs of every CBB in every VGB to the inputs of eight nearby VGBs and to IOBs.
- **Variable-Length-Interconnect** resources provide programmable interconnects that may span two VGBs, four VGBs, eight VGBs, and the entire FPGA.

These interconnect resources provide highly efficient routes for making component connections while maintaining maximum performance levels. In addition to maximizing performance, the VF1 family interconnect methodology allows Vantis' optimization, mapping, and place-and-route software tools to achieve First-Time-Fit results. It also simplifies pin locking and density shifting when moving from one VF1 FPGA to another within the same package type.

Local Feedback

The earlier description of CBBs shows how local feedback lines (LFBs) are routed back from the CBB outputs toward the CBB inputs. These LFBs are then routed to the inputs of every CBB in the same VGB (Figure 13). Local feedback provides a very powerful, high-performance routing resource that works entirely within the VGB and uses no general routing resources.

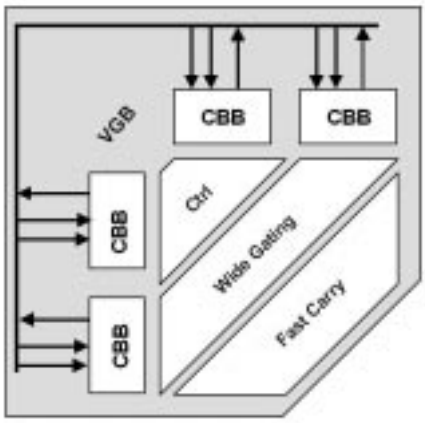

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Figure 13. Local Feedback

Inter-VGB Direct Connect

Every CBB in every VGB has a direct-connect output that connects it to the inputs of two CBBs in eight other nearby VGBs (Figure 14). The direct connect routing shown in the upper left portion of Figure 14 shows how direct-connect lines are routed when the output CBB is not near the edge of the VF1 FPGA. The routing shown in the lower right shows how a direct-connect output connects to three IOBs when the output CBB is near the edge of the device.

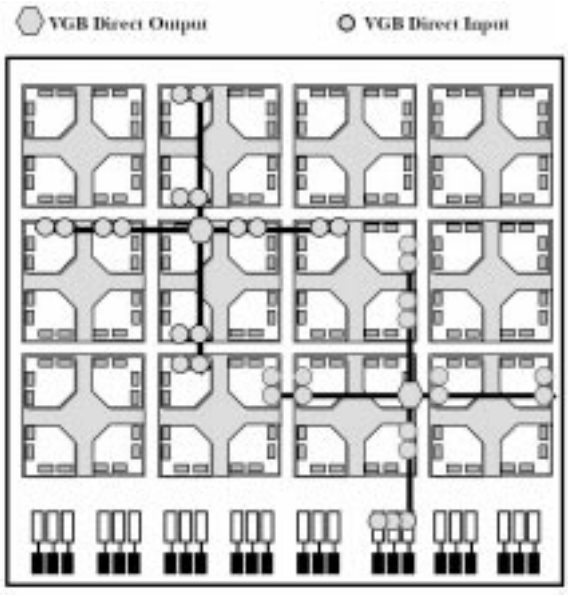

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Figure 14. Inter-VGB Direct Connect

Only two direct-connect routes are shown in Figure 14, but every CBB in every VGB has the same direct-connect routing resources. The direct-connect capability allows VGBs that are adjacent to each other to be combined in very powerful logic structures without using slower general routing resources.

Variable-Length-Interconnect Resources

The VF1 family provides four types of Variable-Length-Interconnect resources that run in channels between Super VGBs, both horizontally and vertically (Figure 15). Two groups of interconnects run within each channel. Each group of interconnects includes the following:

- **Long Connect:** 16 lines run from edge to edge on the chip, both vertically and horizontally.
- **Octal Connect:** 4 lines span 8 VGBs both horizontally and vertically.
- **Quad Connect:** 4 lines span 4 VGBs (two Super VGBs) both horizontally and vertically.
- **Double (or Twin) Connect:** 8 lines span 2 VGBs both horizontally and vertically.

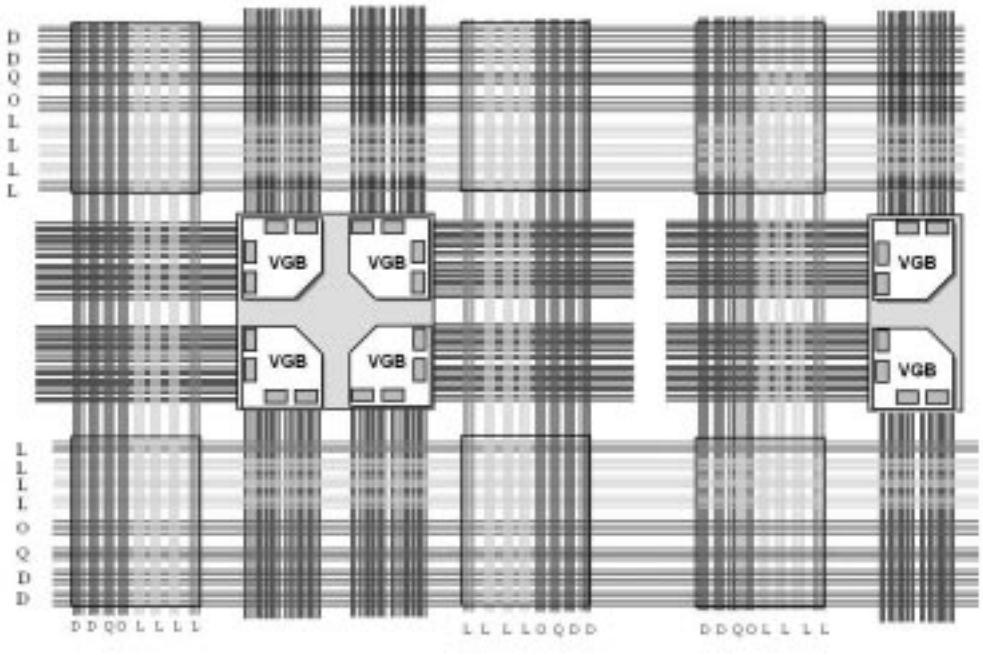

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Figure 15. Variable-Length Interconnect Resources

The sixteen long-connect lines can be used to implement three-state buses, whereas octal, quad, and double connect lines cannot. CBBs can connect directly to octal, quad, and double connect lines, but cannot connect directly to long lines. A VGB output connects to a long line resource by using a shared long-line driver in a Super VGB.

VLI lines change direction by connecting with other VLI lines at switch matrixes located at the intersections of the horizontal and vertical groups of lines. Long lines, however, can bypass the switch matrix by using a CBB Feedthrough line, as described in the CBB section.

Interconnect Performance Considerations

Short connections deliver better performance than long connections. Interconnect resources, in order of performance, are:

- Local feedback within a single VGB
- Direct-connect lines between VGBs and from VGBs to IOBs
- Dual lines that span two VGBs
- Quad lines that span four VGBs
- Octal lines that span eight VGBs
- Long lines that span the entire VF1 FPGA

Vantis' DesignDirect software selects routing resources and calculates timing for both routing and logic delays. Designers can control routing indirectly by specifying timing constraints that must be met by the DesignDirect tools.

Carry Logic

Every VGB includes high-speed carry logic that facilitates the implementation of arithmetic circuits such as adders, subtracters, bit shifters, up/down counters, and comparators. To improve arithmetic speed, the carry chain within a VGB is placed between the CCEs and the CSEs within each CBB (Figure 16).

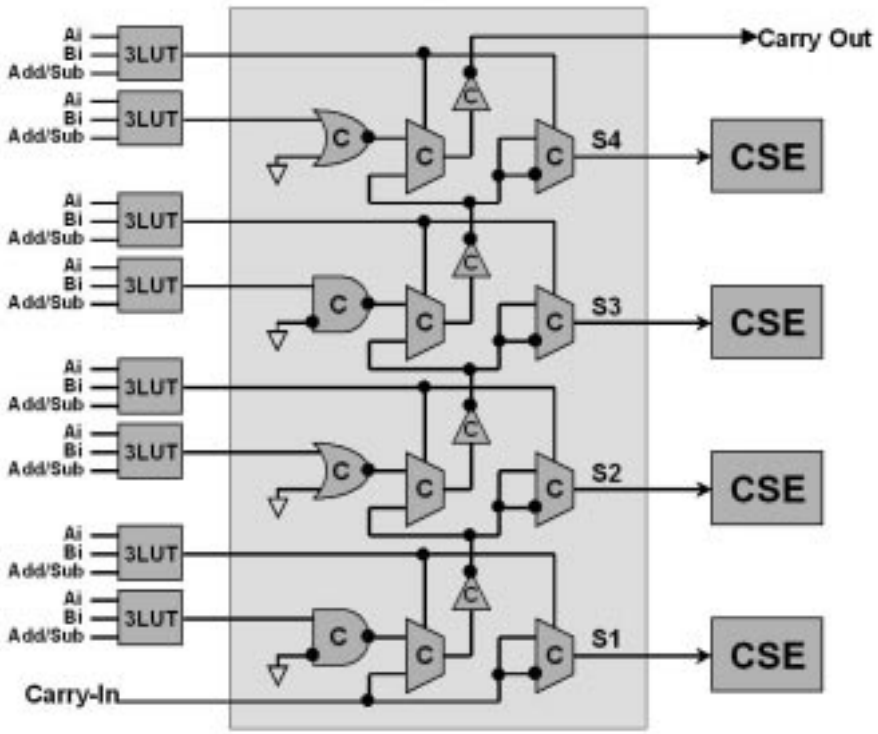

Figure 16. Carry Routing Within a VGB

A VGB receives a carry input from a preceding VGB in the arithmetic chain, and generates a carry for the following VGB (Figure 17). The carry chain between VGBs starts with the bottom VGB in a column and proceeds vertically through the column. Each column of VGBs has its own carry chain.

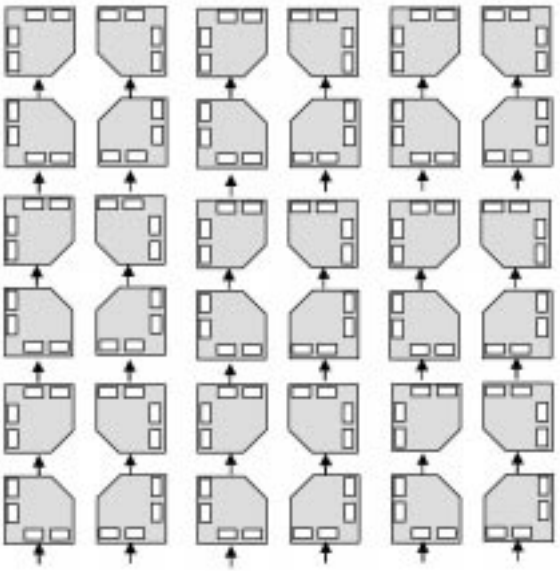

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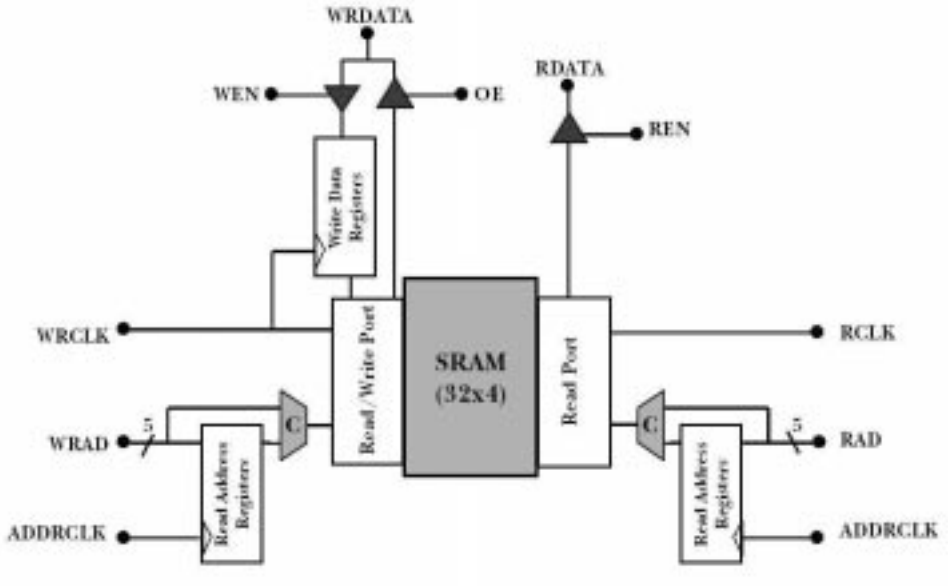
Figure 17. Carry Routing Between VGBs

Embedded Memory

Every VF1 FPGA family member includes embedded memory configured as 32x4 dual-port SRAM blocks (Figure 2). The dual-port configuration (one read/write port and one read port) allows an application to read from the read port while it is reading from or writing to the read/write port. This allows applications such as FIFOs and register stacks to run much faster, and requires only half as many memory bits to implement as a single-port RAM would require.

Specific memory structures are created by the Vantis DesignDirect software and are implemented by the configuration bitstream. In addition, initial memory contents can be loaded at configuration time.



VF1ds-018

Figure 18. VF1 Dual-Port SRAM

The embedded memory is implemented as two columns of memory blocks that run the full length of the FPGA device (Figure 2). Two columns of Super VGBs (four columns of VGBs) run between the memory columns, and additional columns of Super VGBs are outside the memory columns. This configuration minimizes the distance between Super VGBs and embedded memory, thus allowing shorter interconnects and faster memory access. It also simplifies density shifting and pin locking features. Table 3 lists the memory capacity of each VF1 FPGA family member.

Table 3. VF1 Embedded Memory Capacity

	VF1012	VF1020	VF1025	VF1036
VGB Array Size	14 x 14	18 x 18	20 x 20	24 x 24
Embedded Memory Blocks	28	36	40	48
Total Memory Bits	3584	4608	5120	6144

Note:
For a detailed description of memory access modes and timing, refer to the "VF1 Dual-Port SRAM Architecture and Timing" Technical Note.

One port of each SRAM block is a read/write port and the other is a read-only port (Figure 18). The read/write port on the left of Figure 18 consists of a write/read address input (WRAD) that may be stored in Read Address Registers, or may bypass the registers and go directly to the Read/Write Port. For write operations, the write address is stored in the Read/Write Port and write data is stored in the Write Data Registers.

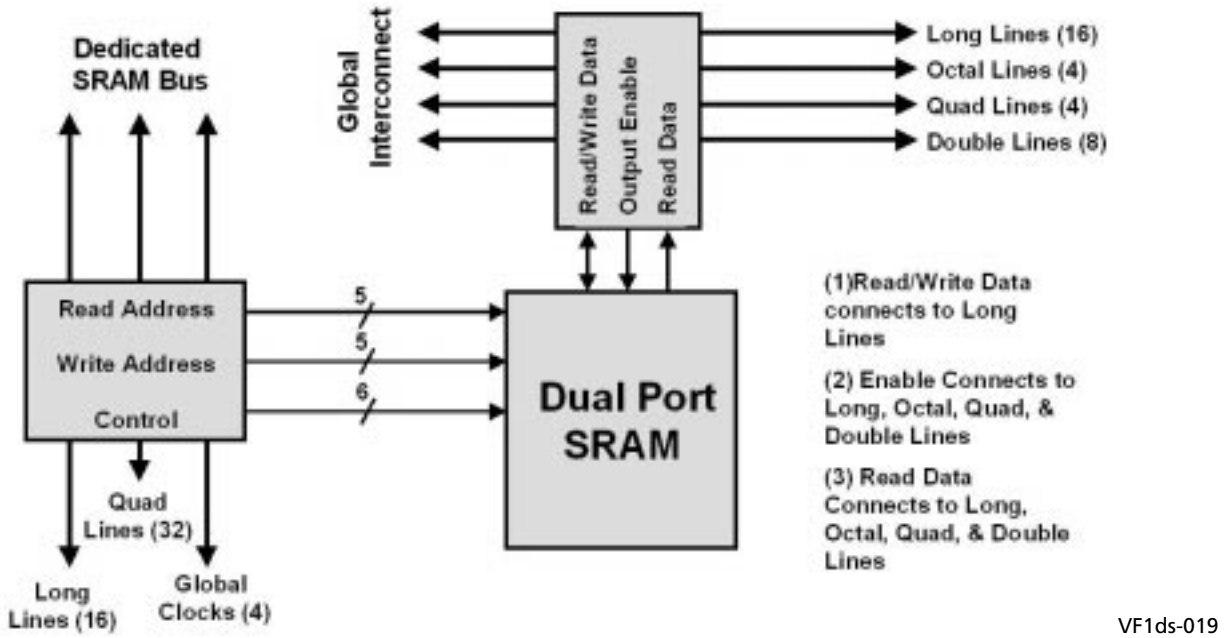


Figure 19. VF1 Dual-port SRAM Routing Resources

Memory read and write addresses come from dedicated SRAM address buses (Figure 19). There are five read address lines, five write address lines, and six control lines (including global clocks) connected to each 32x4 memory block. The SRAM address bus is driven by VLI quad and long lines. Read/write data for the read/write port connect to VLI long lines. Read data from the read port and output enable lines connect to any VLI resources.

Memory Modes

The VF1 embedded memory supports six single- and dual-port synchronous and asynchronous read and synchronous write operations. All single-port operations use the read/write port. The read-only port is used for dual-port operations. All write operations are synchronous. Read operations may be synchronous or asynchronous.

In dual-port operations, it is possible to read from the read port at the same time that the read/write port is performing a read or write. It is also possible to access the same address simultaneously. If the read/write port writes to an address at the same time that the read port reads the address, the read port will read the old contents of the address until the next clock cycle, at which time the contents of the address will change to the new data.

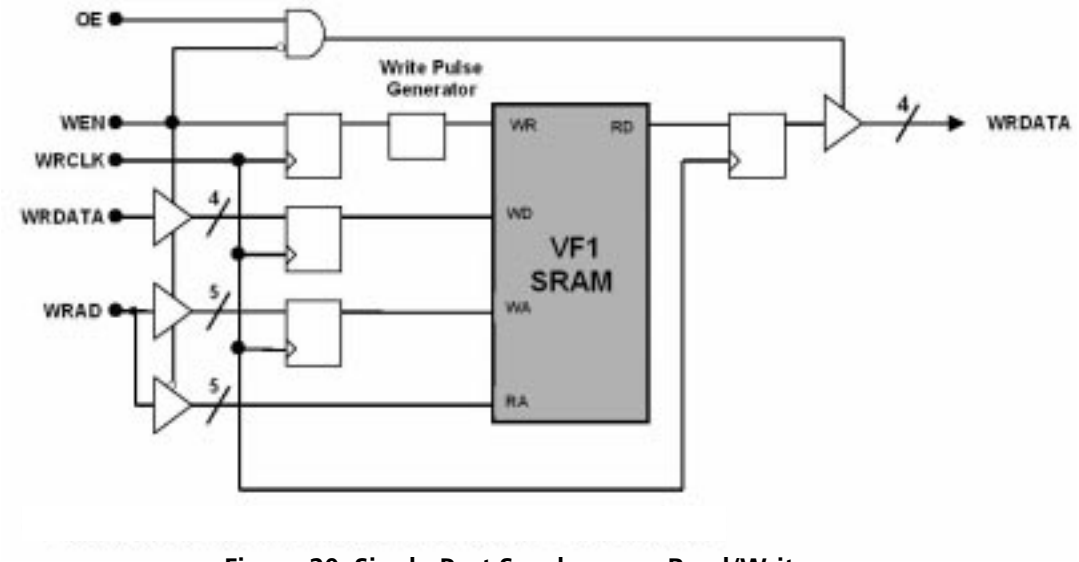
The mode diagrams that follow represent memory behavior and not physical memory implementation. The modes are:

- **Single-port synchronous read/write (Figure 20).** Both read and write operations are synchronized by WRCLK. Synchronous read operations register read data on the output.
- **Single-port synchronous write/asynchronous read (Figure 21).** This operation is identical to the synchronous read/write except that read data is not registered on the output.
- **Single-port synchronous write/asynchronous read, registered read address (Figure 22).** The read address is registered prior to the read/write port using a separate clock (ADDRCLK), rather than the WRCLK that is used for write and synchronous read operations.
- **Dual-port synchronous read/write (Figure 23).** This function adds a second read port to the single-port synchronous read/write operation. The read port functions identically to the read operations in the read/write port.
- **Dual-port synchronous write/asynchronous read (Figure 24).** In this mode the read port performs asynchronous reads while the read/write port performs synchronous writes or asynchronous reads.
- **Dual-port synchronous write/asynchronous read, registered read address (Figure 25).** The read port performs registered address read operations.

The timing diagrams in Figures 26-29 show the timing relationships for each mode. Write timing applies to the read/write port only, and read timing is identical for each port.

Note:

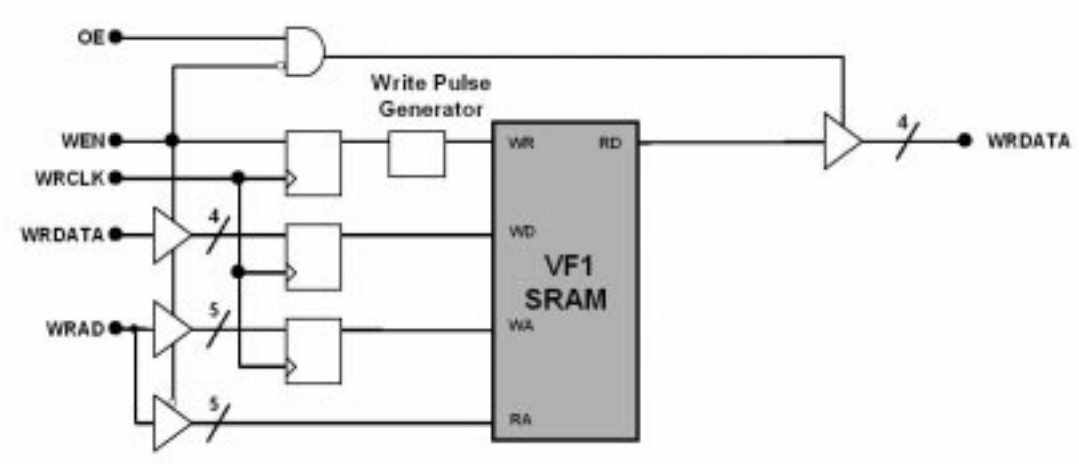
More detailed descriptions of these memory modes, plus detailed timing diagrams of each mode, are found in the "VF1 Dual-Port SRAM Architecture and Timing" Technical Note.



VF1ds-020

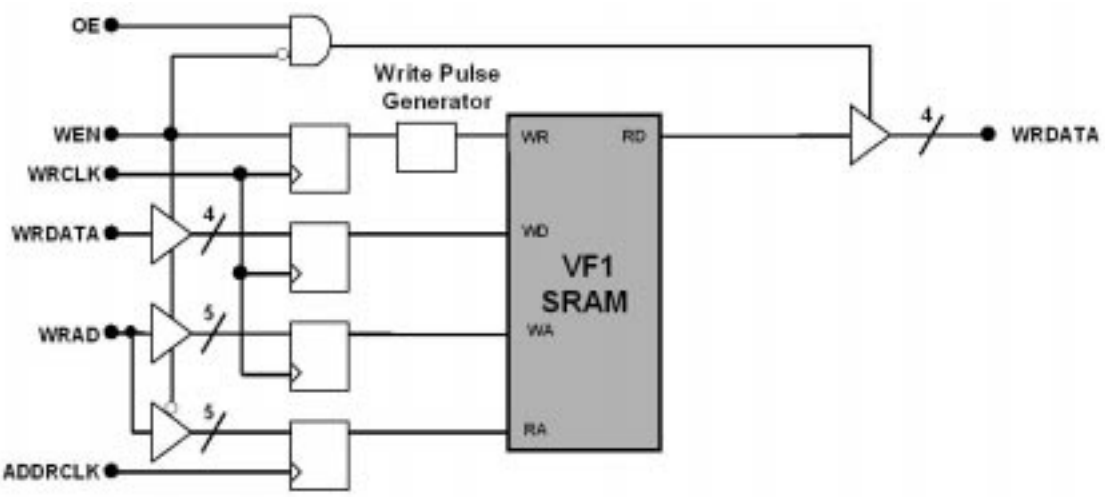
Figure 20. Single-Port Synchronous Read/Write

Note:
Diagram only represents behavior and not physical implementation



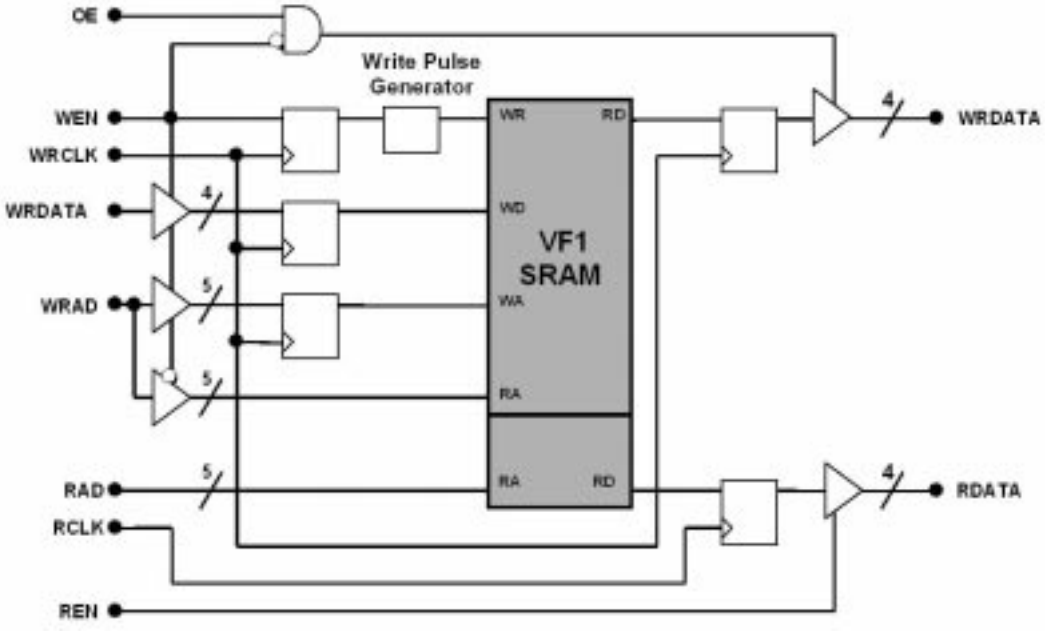
VF1ds-021

Figure 21. Single-Port Synchronous Write/Asynchronous Read



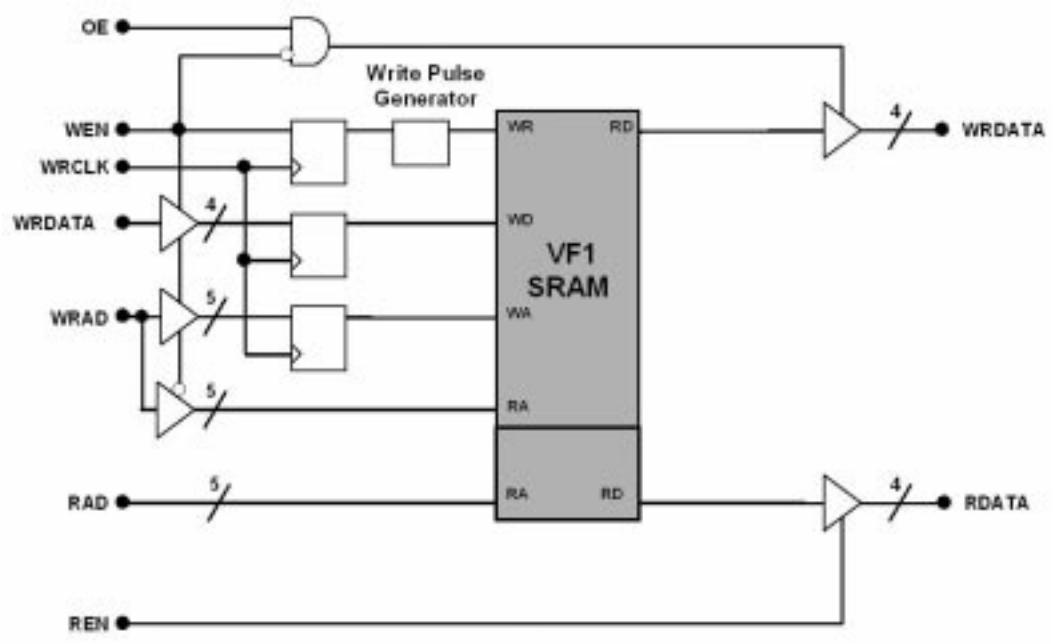
VF1ds-022

Figure 22. Single-Port Synchronous Write/Asynchronous Read, Registered Read Address



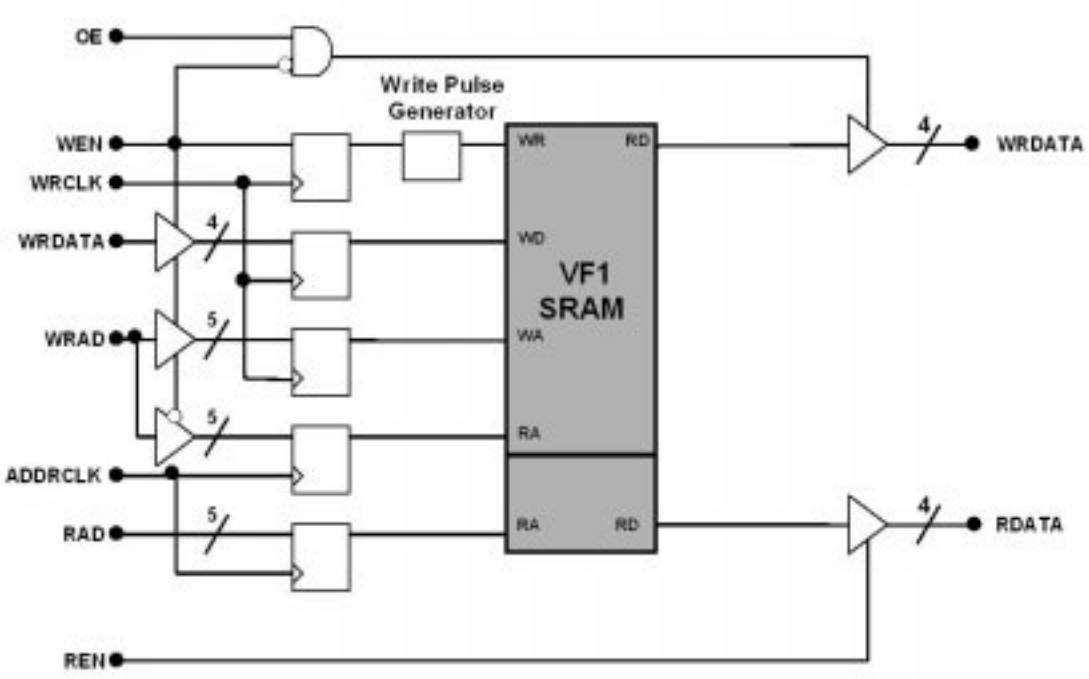
VF1ds-023

Figure 23. Dual-Port Synchronous Read/Write



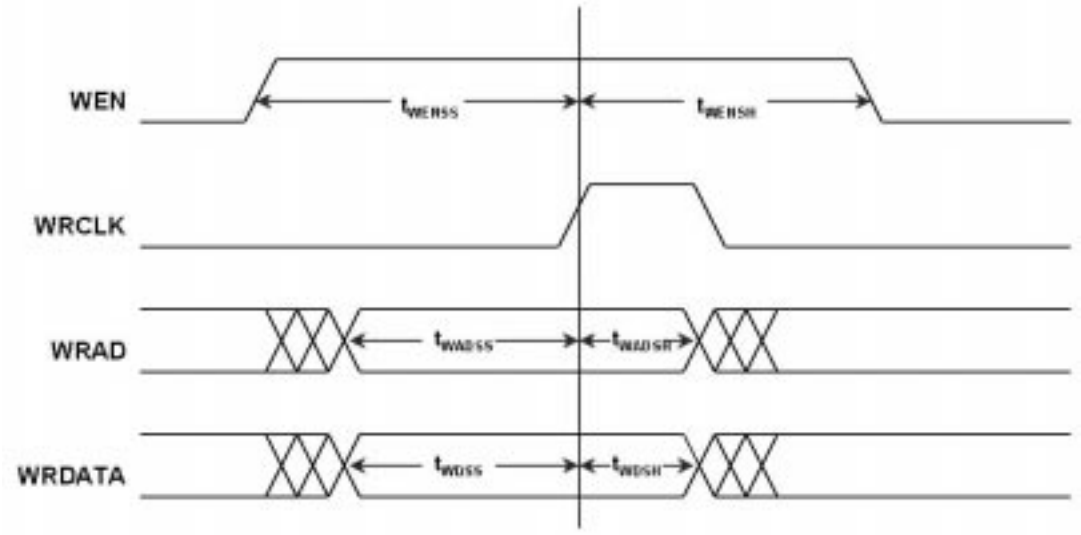
VF1ds-024

Figure 24. Dual-Port Synchronous Write/Asynchronous Read



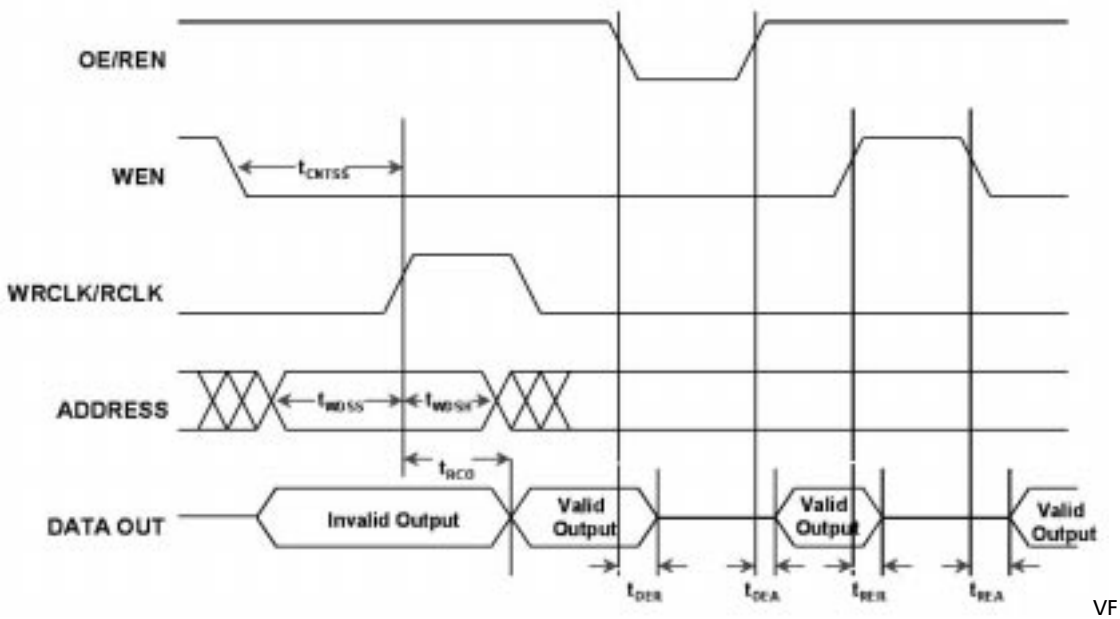
VF1ds-025

Figure 25. Dual-Port Synchronous Write/Asynchronous Read, Registered Read Address



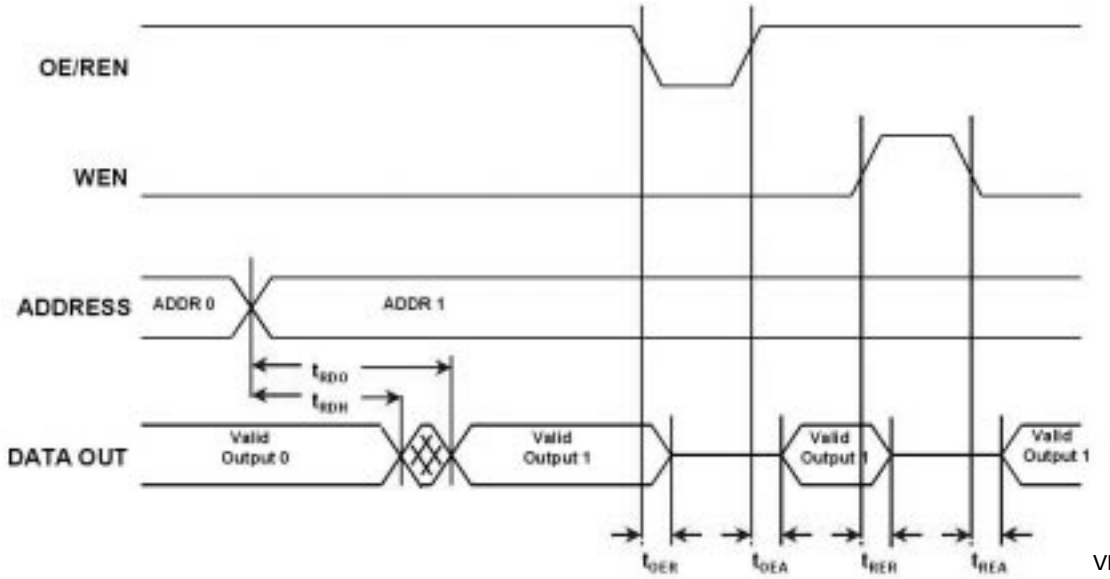
VF1ds-026

Figure 26. Synchronous Write Timing



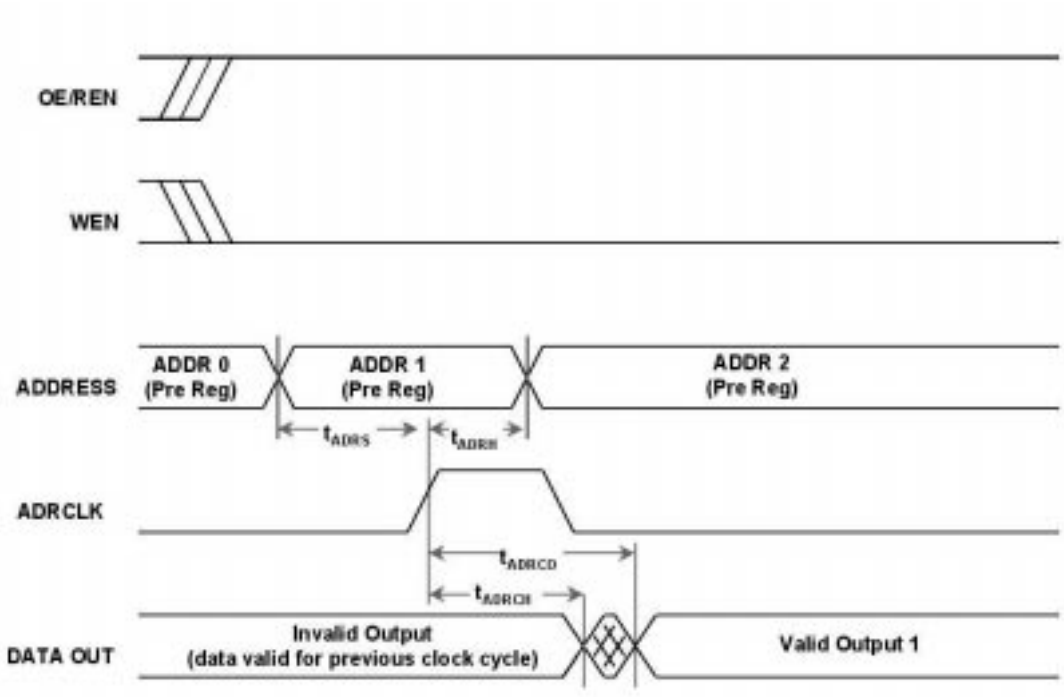
VF1ds-027

Figure 27. Synchronous Read Timing



VF1ds-028

Figure 28. Asynchronous Read Timing



VF1ds-029

Figure 29. Asynchronous Read Timing with Registered Read Address

Input/Output Blocks

Input/output blocks (IOBs) provide an interface between the internal logic functions of the VF1 FPGA and the remainder of the system in which the device is installed. IOBs support input and output functions, and interface the VF1 FPGA to both 3.3V and 5V I/O levels.

IOB regions lie on all four sides of the FPGA (Figure 2). Each programmable IOB includes a pad, input logic, and output logic (Figure 30). The input and output sections function separately from each other, sharing only the I/O pad and common Set/Reset logic. The common Set/Reset signal is either the VF1 Global Set/Reset, or a local set/reset.

Separate input and output enable signals allow an IOB to function as both an input pin and an output pin in a design.

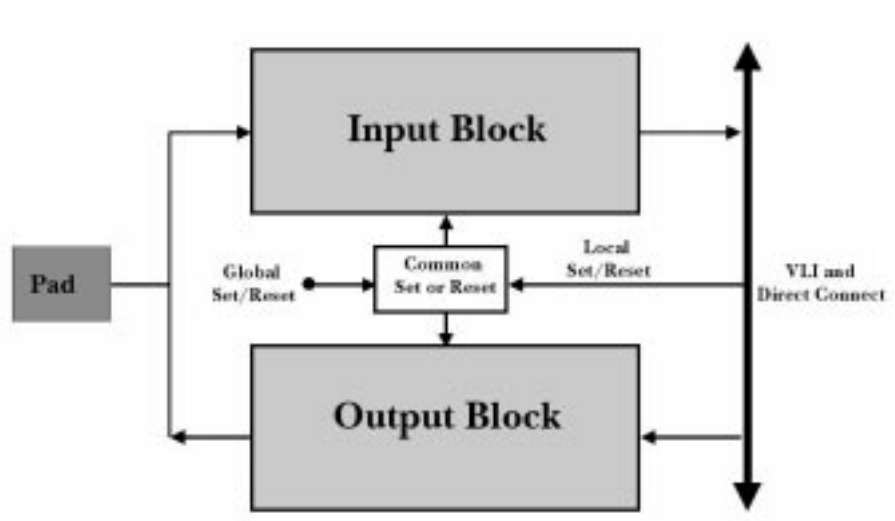


Figure 30. VF1 Input/Output Block (IOB)

Figure 31 gives a more detailed view of the programmable IOB. Both the input and output sections share a common set/reset signal. The set/reset may be locally-generated (LSR), or it may be the VF1 global signal (GSR). The input and output sections use separate clocks and separate clock enables.

The IOB input section includes an input buffer, input register/latch, and programmable logic to connect the input to appropriate interconnect lines. The input signal may either be registered or bypass the register. When the register is used, a delay may be inserted between the input pad and the register (Figure 32) to ensure zero hold time for the register when using an external clock. The delay is not used when an on-chip PLL generates the clock (refer to the PLL description later in this document).

Input signals may be routed to long lines, to shift-connect lines, to edge-connect lines, or directly to VGBs via direct connect lines. The long-line connections may be permanently enabled by tying to V_{CC}, disabled by tying to GND, or dynamically controlled via a locally-generated signal. Other connections are established when the VF1 FPGA is configured. Connections are described in more detail following the IOB output description.

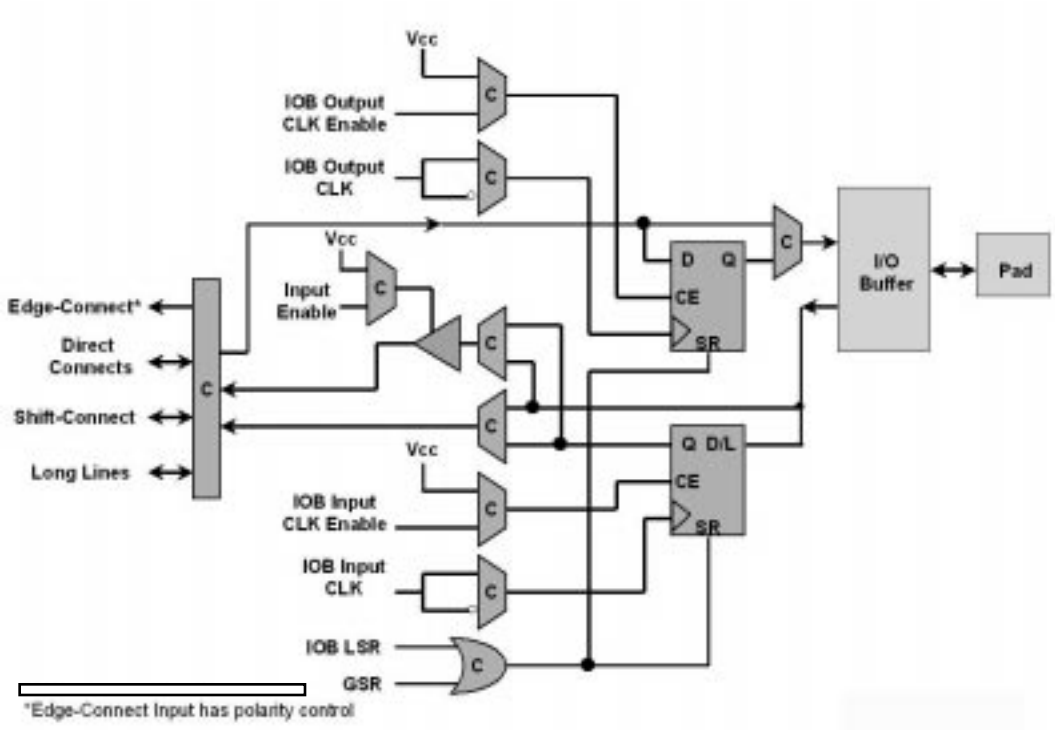
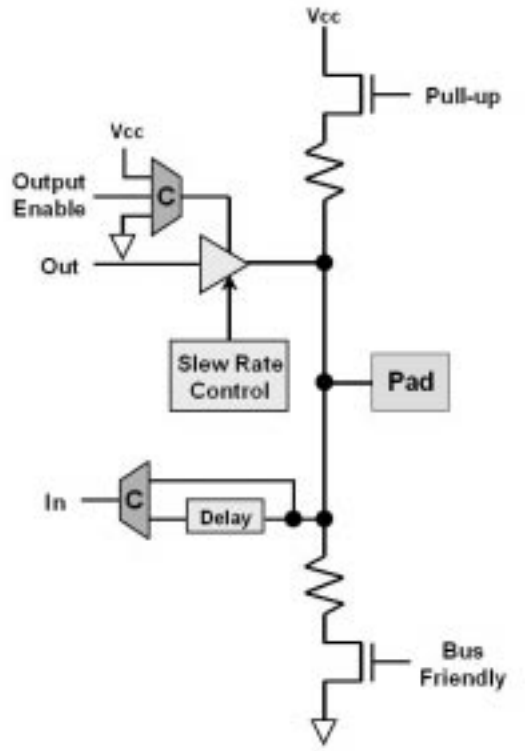


Figure 31. VF1 Input/Output Block

Note:
Edge-Connect input has polarity control

The IOB output section includes programmable interconnections from the VF1 logic, an output register, and an output buffer with programmable slew rate control (Figures 31 and 32). Output data may come from direct connect lines, long lines, or shift-connect lines. The output may be permanently enabled or disabled by tying to V_{cc} or GND, or controlled dynamically by a locally-generated enable signal.

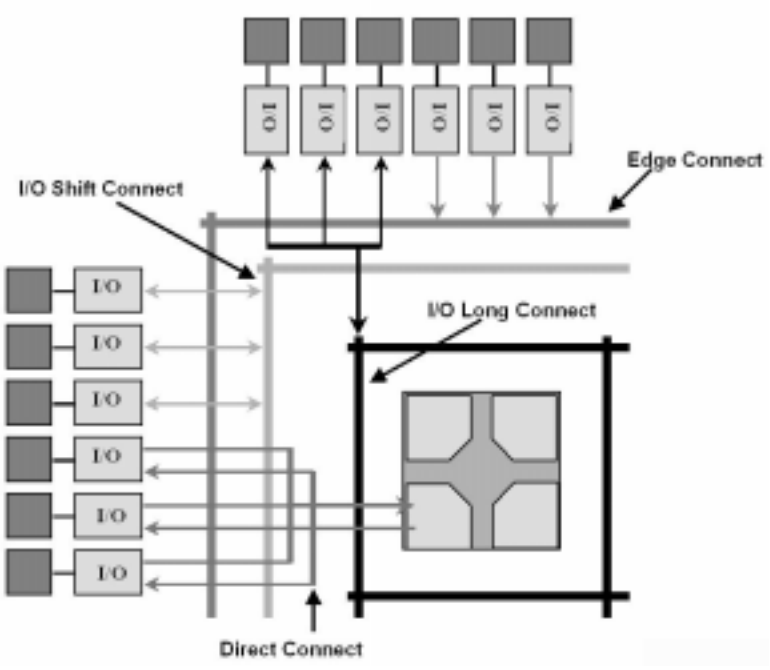


VF1ds-032

Figure 32. VF1 I/O Buffer

The VF1 I/O buffer (Figure 32) offers designers a wide selection of programmable capabilities:

- **Three-state control capability** for interfacing to buses
- **Programmable pull-up resistor** for a weak high bias
- **Programmable Bus-Friendly™ architecture** to hold the last output value when the IOB goes into high-impedance mode
- **Output slew rate control** to reduce ringing
- **Programmable input delay** allows zero hold time from external clock
- **IEEE 1149.1 boundary scan** capability to simplify board testing



VF1ds-033

Figure 33. IOB Interconnect

IOBs may connect to long lines, shift-connect lines, direct-connect lines, and Edge Connect lines (Figure 33). Long-line connections allow any VGB anywhere in the VF1 FPGA to be connected to IOBs. Long-line connections are made to routing resources that are perpendicular to the edge of the device where the IOB is located. Each IOB may connect to two long-line channels.

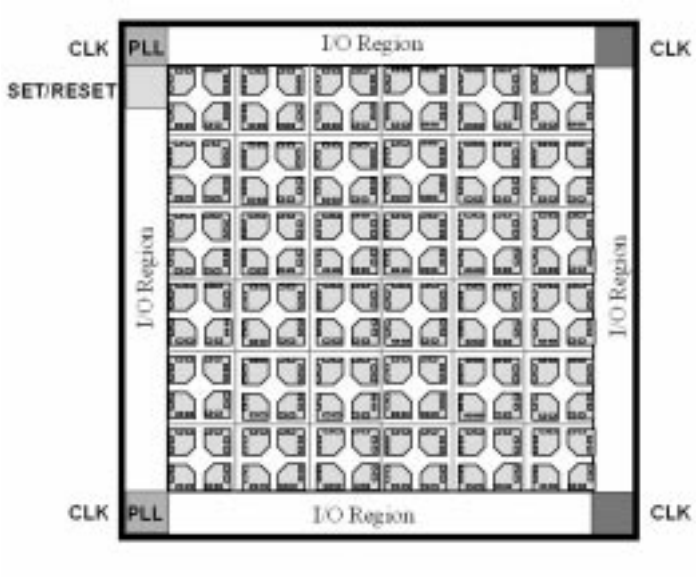
Shift-connect lines give the VF1 FPGA family a very powerful pin-locking capability when a design moves a design to either a higher or lower density VF1 FPGA. Shift-connect lines expand an IOBs long-line connection span from two channels to four, making it much more efficient to lock pin assignments when shifting from one device density to another.

Direct-connect lines connect IOBs directly with VGBs that are near the edge of the VF1 FPGA. These are the fastest connections between logic elements and I/O elements.

Edge Connect lines apply to inputs only. An IOB input section may be configured to connect to an Edge Connect line as well as another data line. The Edge Connect lines (two per side of the VF1 FPGA) are used to implement input NOR functions on IOB inputs.

Global Interconnect and PLL

Global signals in the VF1 family include four global clocks and a global set/reset function (Figure 34). The Set/Reset signal input is at one corner of the VF1 FPGA. The four global clock inputs are distributed with one CLK input at each corner. Two of the global clocks may be applied to embedded phase-locked loop (PLL) circuits for clock deskewing and frequency multiplication.

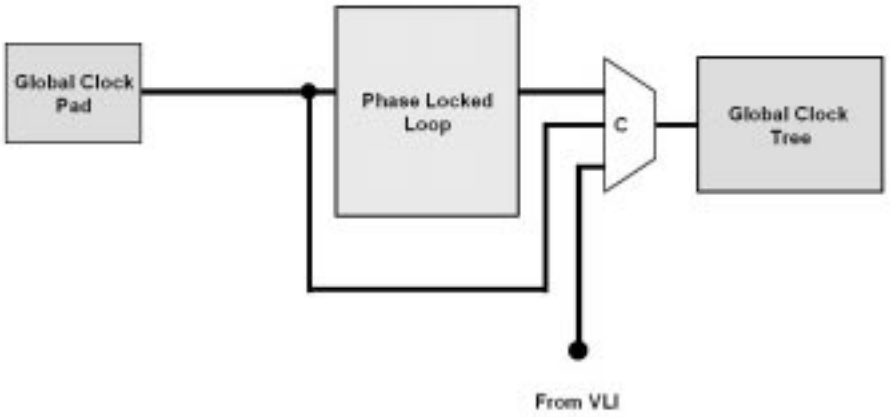


VF1ds-034

Figure 34. VF1 Global Interconnect

All four global clocks have individual clock trees that distribute them throughout the VF1 FPGA (Figure 35). These clock trees cannot be subdivided. Clocks associated with PLLs may either bypass the PLL circuit or may be applied to the PLL with the PLL output applied to the clock tree. In addition, clocks may be generated within the VF1 FPGA and distributed using the global clock tree (the VLI input in Figure 35).

Maximum input frequency on any clock pin is 250 MHz. Operation at the maximum frequency requires certain design considerations. Refer to Vantis applications notes for guidelines on high-frequency designs.



VF1ds-035

Figure 35. Global Clocks and PLL

PLL

The embedded analog PLL circuits can be used to deskew clocks from one chip to another and to synthesize on-chip clocks using an external reference frequency (usually an external clock input).

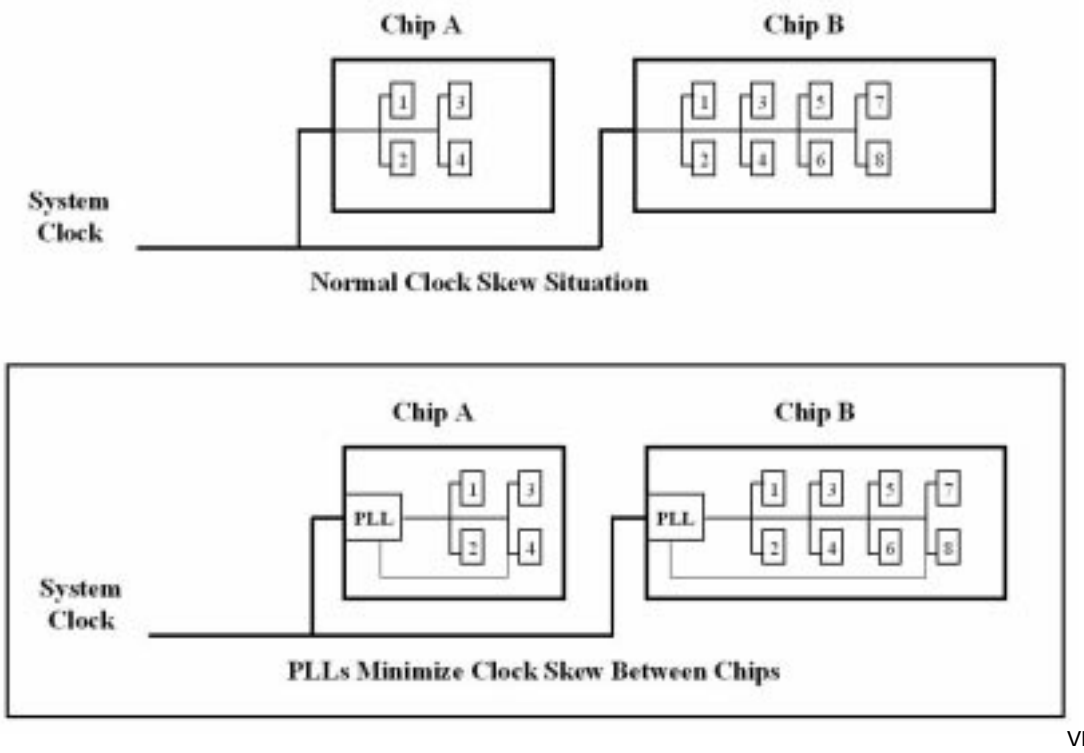
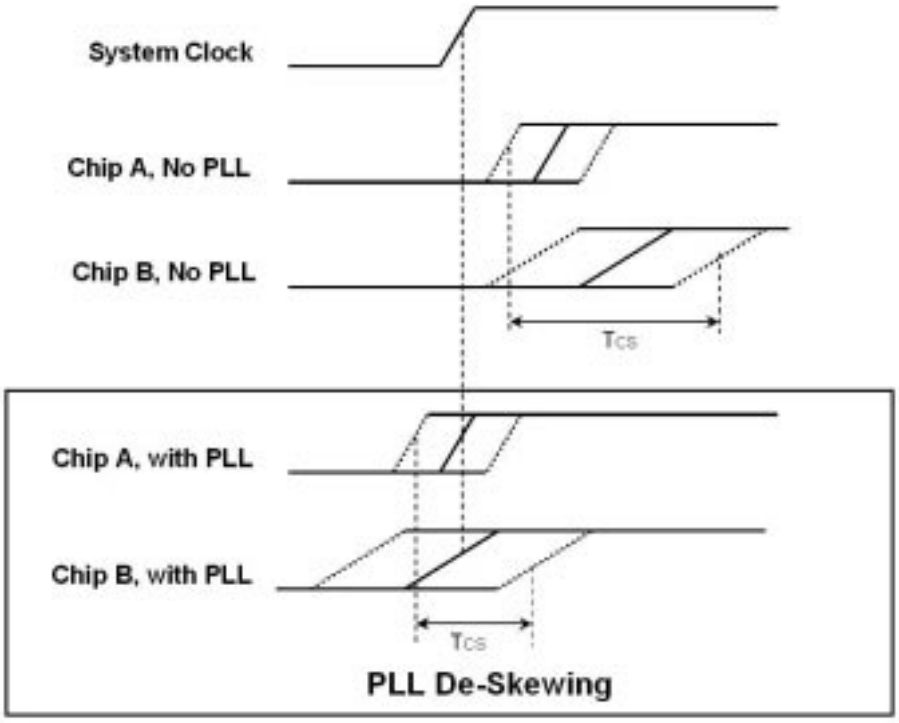


Figure 36. Deskewing Clocks with PLLs

Clock skew from one chip to another robs a system of much of its performance by delaying the generation of reliable outputs from larger chips. When a system clock is applied to two chips of different sizes (Figure 36), the clock will propagate through the chips at different rates. For example, the clock will reach flip-flop 4 in Chip A (Figure 36, upper diagrams) much sooner than it reaches flip-flop 8 in Chip B. Process and environmental variables also contribute to clock skew within a chip.

The waveforms (Figure 37, upper waveforms) show the results of skew in the two chips. The dotted lines in the chip waveforms show when the system clock reaches the first flip-flop in the chip and when it reaches the last. The solid line shows when the clock reaches the mid-point along each chip's clock trunk.

A PLL can "shift" the reference clock within a chip and reduce the time that it takes for the chip to generate its output. The PLL works by monitoring the reference clock and the clock signal at the end of the chip's clock trunk (Figure 36, lower diagrams). It then shifts the clock phase so that the shifted clock pulse reaches the end of each chip at the same time that the system clock reaches the chip input. The PLL effectively synthesizes a new clock at the same frequency as the system clock, but slightly shifted in phase (Figure 37, lower waveforms).



VF1ds-037

Figure 37. PLL Waveforms for Deskewing Clocks

Table 4. PLL operating conditions

Symbol	Parameter	Min	Max	Unit	Output Frequency
t_{RISE}	Input clock rise time		5	ns	
t_{FALL}	Input fall time		5	ns	
t_{INDUTY}		40	60	%	
F_{CLK1}	Input Clock Frequency with multiplication factor of 1	30	150	MHz	30 to 150 MHz
F_{CLK2}	Input Clock Frequency with multiplication factor of 2	16	100	MHz	32 to 200 MHz
F_{CLK3}	Input Clock Frequency with multiplication factor of 3	16	66	MHz	48 to 198 MHz
$t_{INCLKSTB}$	Input Clock Stability (between adjacent clocks)		100	ps	
t_{LOCK}	Time for PLL to acquire lock		30	µs	
$t_{TOTJITTER}$	Total jitter on PLL output (both accumulated and phase-to-phase measures as peak-to-peak)		500	ps	
$t_{OUTDUTY}$	Duty cycle for PLL output	40	60	%	

The PLL can also be used to synthesize on-chip clocks that are multiples of the system clock frequency, up to a maximum of 200MHz. For example, if the system clock operates at 66MHz, the on-chip PLL can double the clock to 132MHz or triple it to 198MHz. If the system clock runs at 100 MHz, the PLL can double it to 200 MHz for use within the VF1 FPGA.

Table 4 lists the PLL operating conditions.

As shown in Table 4 (see t_{LOCK} signal), the PLL will acquire a lock on the reference clock within 30 µs, but it may acquire a lock much sooner. A LOCK status signal goes high when a lock is

acquired, so it is possible either to wait 30 µs or to test the LOCK signal to assure that the PLL has acquired a lock.

Global Set/Reset

The VF1 global set/reset signal (Figure 38) may be generated externally and applied to the VF1 FPGA via the Global Set/Reset input pin, or it may be generated within the VF1 FPGA. In addition, the polarity of the set/reset signal may be selected. Both of these conditions are determined at configuration time.

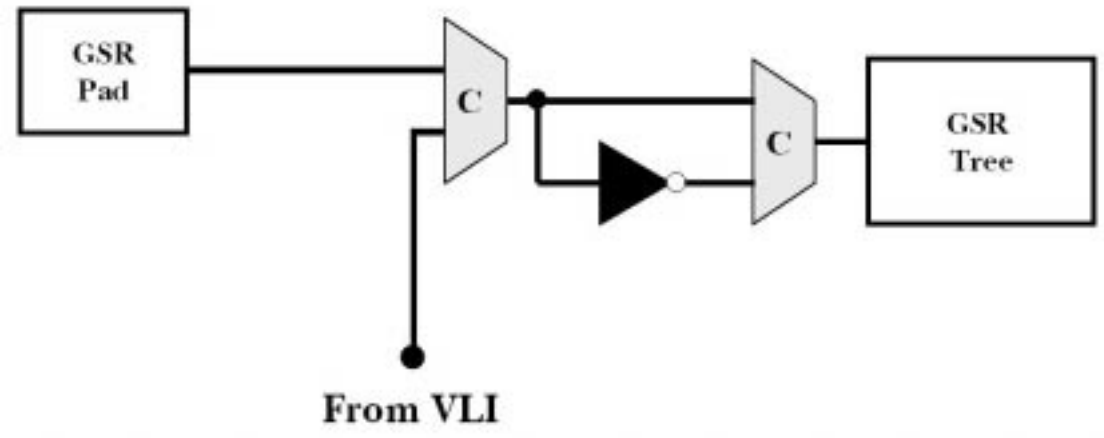


Figure 38. Global Set/Reset

Design Methodology

Complex systems with greater than 10K gates require a sophisticated software-based design methodology. While a schematic-based methodology may be adequate for smaller designs, and sometimes for portions of larger designs, a hardware-description language (HDL) is more appropriate for developing complex designs.

The Vantis design flow consists of two parts (Figure 39):

- **Design development** using third-party front-end development tools. These tools provide design entry, simulation, synthesis, and timing analysis. Designs are transferred from these tools to the Vantis tools in an EDIF file format. Some third-party tools can provide timing constraint files for use by the Vantis tools.
- **Design implementation** using Vantis physical design tools. These technology-specific tools provide optimization, mapping, timing calculation, and device programming. The output is a JEDEC bit-stream file for programming VF1 FPGAs via the JTAG port or the dedicated programming port.

The Vantis tools include a design manager, graphical user interface, and a logic editor and viewer. The logic editor and viewer enable viewing and moving logic elements down to the VGB level.

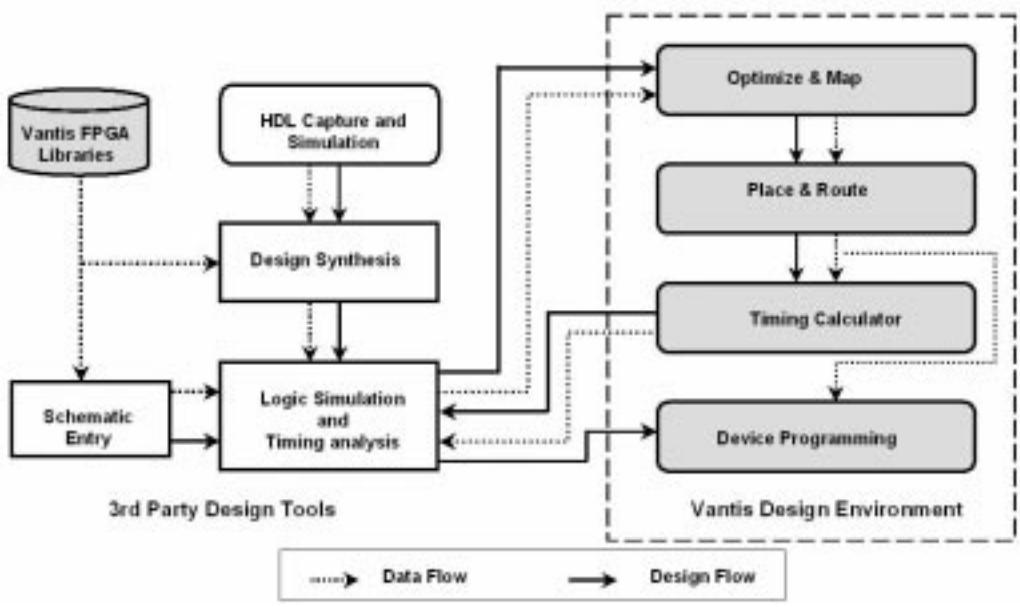
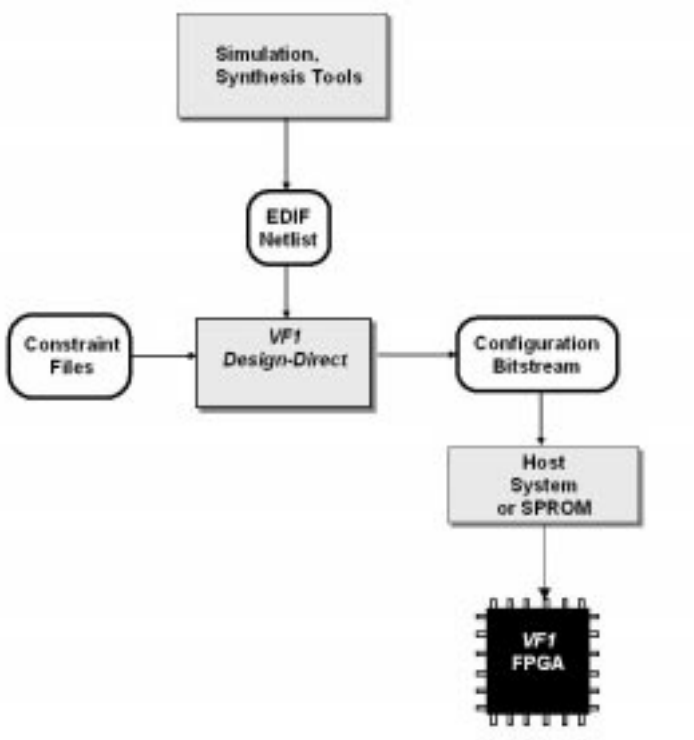


Figure 39. Vantis Design Methodology

Vantis design environment tools are timing driven, using timing constraint files that are provided by the third-party front-end tools (Figure 40). The Vantis tools generate timing files that can be fed back to the front-end tools for further simulation and timing analysis. The output of the design process is a configuration bitstream that is loaded a VF1 FPGA during configuration.



VF1ds-040

Figure 40. DesignDirect Inputs and Outputs

Detailed descriptions of the Vantis design methodology and tools are found in the *Design Methodology Users Manual* on the software CD-ROM.

JTAG Compatibility

VF1 family FPGA products are fully compliant with JTAG 1149.1. They implement the following standard JTAG instructions:

- BYPASS
- SAMPLE/PRELOAD
- EXTEST
- HIGHZ
- USERCODE
- IDCODE
- INTEST

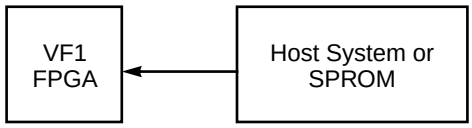
In addition, they implement three non-standard instructions that are used for configuring the VF1 FPGAs through the JTAG port. These instructions are described in the *Configuration modes* section that follows.

Configuration Modes

The VF1 family of devices consists of SRAM-based reprogrammable FPGAs that are configured, or programmed, every time they are powered up. Configuration is the process of loading configuration data into the device from either a companion SPROM or a host system (Figure 41).

The configuration data defines the device's functionality. In addition to power-up configuration, VF1 FPGAs can be reconfigured during operation (in-system programming) if the host system decides to change the device's functionality.

The following is a general description of each configuration mode. Detailed descriptions of all modes and timing are contained in the *VF1 Configuration Guide* Technical Note. The Vantis *VCM SPROM* data sheet describes the companion SPROM.



VF1ds-041

Figure 41. Configuring a VF1 FPGA

The VF1 FPGA family supports five configuration modes, two that use SPROMs and three that depend on a host processor. The modes are:

- **Master serial mode.** The VF1 automatically loads its configuration data from an external serial PROM.
- **Slave serial mode.** When two or more VF1 FPGAs in a system are loaded from the same PROM, the first device loaded is loaded in Master serial mode and subsequent devices are loaded in Slave serial mode. In this mode, the master device provides the CCLK signal to slave devices.
- **Asynchronous peripheral mode.** A host device provides configuration data a byte at a time in parallel to the VF1 FPGA. The VF1 FPGA serializes the data internally for loading.
- **Synchronous peripheral mode.** A host device provides the load clock to the VF1 FPGA and provides byte-wide configuration data on every eighth clock pulse.
- **JTAG mode.** The VF1 FPGA configuration data is loaded via the JTAG boundary scan circuitry. A host, such as a microprocessor, controls loading and provides configuration data.

Configuration modes are selected by the three mode pins, M0-M2, as shown in Table 5.

Table 5. Configuration Mode Selection Pins

Configuration Mode	M2	M1	M0
Master Serial	0	0	0
Slave Serial	1	1	1
Synchronous Peripheral	0	1	1
Asynchronous Peripheral	1	0	1
JTAG	0	0	1

Modes are described briefly below. The Technical Note *VF1 Configuration Guide* provides comprehensive guidelines.

With the exception of the pins directly involved in configuration, all VF1 I/O pins are in three-state mode during configuration. Following configuration the state of the I/O pins is determined by the configuration pattern. Table 5 lists the pins that are used by the various configuration modes.

Table 6. Pins Used in Configuration Modes

Master Serial	Slave Serial	Synchronous Peripheral	Asynchronous Peripheral	JTAG	User Operation
M0 (I)	M0 (I)	M0 (I)	M0 (I)	M0 (I)	(I/O)/RTRIG
M1 (I)	M1 (I)	M1 (I)	M1 (I)	M1 (1)	(I/O)/RDO
M2 (I)	M2 (I)	M2 (I)	M2 (I)	M2 (I)	(I/O)
/PROGRAM (I)	/PROGRAM (I)	/PROGRAM (I)	/PROGRAM (I)	/PROGRAM (I)	/PROGRAM (I)
/INIT (OD)	/INIT (OD)	/INIT (OD)	/INIT (OD)	/INIT (OD)	(I/O)
DONE (OD)	DONE (OD)	DONE (OD)	DONE (OD)	DONE (OD)	DONE (OD)
HDC (O)	HLC (O)	HLC (O)	HLC (O)		(I/O)
/LDC (O)	/LDC (O)	/LDC (O)	/LDC (O)		(I/O)
CCLK (O)	CCLK (I)	CCLK (I)	CCLK (O)		CCLK (I)
TDI (I)	TDI (I)	TDI (I)	TDI (I)	TDI (I)	TDI (I)
TCLK (I)	TCLK (I)	TCLK (I)	TCLK (I)	TCLK (I)	TCLK (I)
TMS (I)	TMS (I)	TMS (I)	TMS (I)	TMS (I)	TMS (I)
TDO (O)	TDO (O)	TDO (O)	TDO (O)	TDO (O)	TDO (O)
DOUT (O)	DOUT (O)	DOUT (O)	DOUT (O)		(I/O)
DIN0 (I)	DIN0 (I)	DIN0 (I)	DIN0 (I)		(I/O)
		DIN1 (I)	DIN1 (I)		(I/O)
		DIN2 (I)	DIN2 (I)		(I/O)
		DIN3 (I)	DIN3 (I)		(I/O)
		DIN4 (I)	DIN4 (I)		(I/O)
		DIN5 (I)	DIN5 (I)		(I/O)
		DIN6 (I)	DIN6 (I)		(I/O)
		DIN7 (I)	DIN7 (I)		(I/O)
		RDY/(/BUSY) (O)	RDY/(/BUSY) (O)		(I/O)
			/CS0 (I)		(I/O)
			CS1 (I)		(I/O)
			/WS (I)		(I/O)
			/RS (I)		(I/O)

Notes:

I = Input
O = Output
OD = Open Drain
I/O = Input/Output

Functions of the configuration mode signals are described below. Refer to the individual mode descriptions that follow for timing relationships of these signals.

M0/RTRIG **M1/RDO** **M2**	**Three multiplexed I/O pins that select the configuration mode.** During configuration, these pins are input pins and are sampled right after initialization to determine the configuration mode. In normal mode, M0 and M1 can be used as RTRIG and RDO for non-JTAG read-back.
/PROGRAM	**A dedicated input pin that initiates configuration.** A low level clears the configuration memory and puts the device into a WAIT state. The MODE pins are sampled. A low-to-high transition clears the configuration memory once more and starts the configuration process. If this pin is high during power up, the device will skip the WAIT state after clearing the configuration memory and will go directly into configuration mode.
/INIT	**A multiplexed I/O pin that indicates initialization status.** During device configuration /INIT is an open-drain status pin that can also be used to reset the serial EPROM for a Master device. A low /INIT when /PROGRAM is high indicates initialization is not complete and the device is not ready to receive data for configuration. Tying all the /INIT pins from different devices together ensures the Master device does not start configuration until all slave devices are initialized. For non-JTAG configuration modes, holding the /INIT pin low externally will delay configuration.
DONE	**A dedicated open drain pin that signals when configuration is done.** A low output indicates the device is in configuration. A high output indicates configuration is done and all the I/Os will be enabled. For non-JTAG configuration modes, enabling of all the I/Os in different devices can be synchronized by tying all the DONE pins together.
HDC	**A multiplexed I/O status pin that is Low During Configuration.**
/LDC	**A multiplexed I/O status pin that is Low During Configuration.**
CCLK	**A dedicated I/O pin for configuration clock input or output.** In the Master mode, this pin is the clock output from an internal oscillator that drives the serial EPROM and Slave VF1 FPGAs. In the Slave mode and Synchronous Peripheral mode, this pin receives a clock from the Master VF1 FPGA or from a host source.
TDI, TCLK, TMS, TDO	**TDI, TCLK, and TMS are dedicated input pins; TDO is a dedicated output pin.** These pins are used for JTAG boundary scan functions and for programming VF1 FPGAs in JTAG mode.
DOUT	**A multiplexed I/O pin to pass configuration data from the first VF1 FPGA in a chain to subsequent devices.** During configuration, this is an output pin for sending DIN data to daisy-chained devices.
DIN0-7	**Seven multiplexed I/O pins for byte-wide data input.** During Synchronous and Asynchronous Peripheral modes, these input pins receive parallel configuration data.
RDY/(/BUSY)	**A multiplexed I/O Ready or Busy status pin.** This pin indicates when it is appropriate to write another byte of data into the VF1 FPGA during Peripheral mode configuration. In Asynchronous peripheral mode, the pin is high (RDY) when the VF1 is ready to receive data, and it is low (/BUSY) when the VF1 is processing the last byte it received. In Synchronous peripheral mode, the signal is normally low and goes high for one CCLK period to acknowledge the receipt of a byte of configuration data.
/CS0, CS1, /WS, /RS	**Multiplexed I/O pins.** These four inputs are used in Asynchronous Peripheral mode. The chip is selected when /CS0 is low and CS1 is high. While the chip is selected, a low on /WS loads the data on DIN [0:7] into the internal data register. A low on /RS changes DIN7 into a status pin that outputs the same signal as the RDY/(/BUSY) pin.

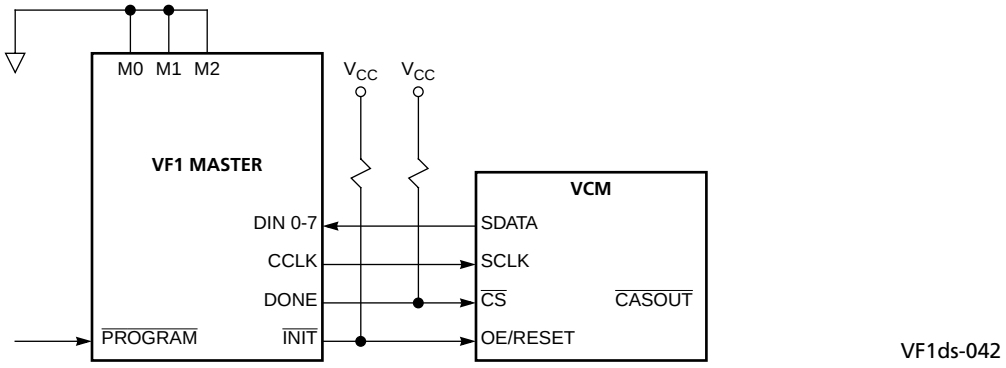


Figure 42. Master Serial Mode

Master Serial Mode

In Master serial mode, configuration data is loaded automatically from a serial PROM into the VF1 FPGA (Figure 42). On power-up, or when a PROGRAM command is received, both the /INIT signal and the DONE signal from the VF1 FPGA go low, generating /CE and /RESET signals to the serial EEPROM.

The /INIT signal goes high, enabling the output of the EEPROM. The VF1 FPGA generates the configuration clock, CCLK, and applies it to the EEPROM. CCLK clocks the configuration data out of the EEPROM and clocks it into the VF1 FPGA.

If two or more EEPROMs are required to hold the configuration data, the first EEPROM pulls its /CASOUT signal low when it has loaded its last data bit, enabling the second EEPROM to provide subsequent configuration data. The loading continues until the VF1 FPGA is fully configured at which time DONE goes high, halting the configuration process.

Configuration can also be initiated by the /PROGRAM command.

Both /INIT and DONE are open-collector drivers that require external pull-up resistors.

Slave Serial Mode

Slave serial mode is normally used when two or more VF1 FPGAs are configured in a daisy chain (Figure 43). In Figure 43 first VF1 FPGA in the chain is configured as a Master and all following devices are slaves. Two SPROMs are shown to illustrate how they may be cascaded to provide adequate storage for multiple configuration bitstreams. The Master VF1 FPGA generates the CCLK configuration clock for all devices in the chain as well as for the SPROMs.

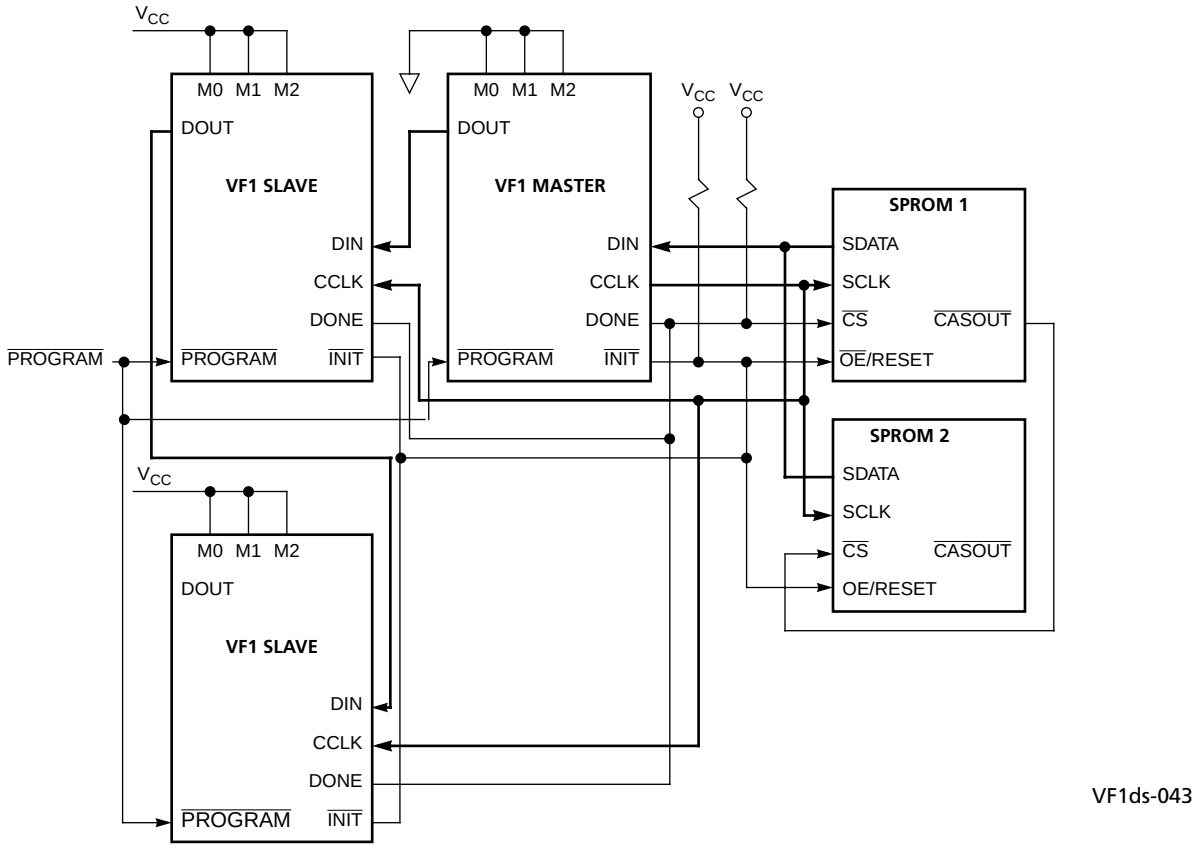


Figure 43. Slave Serial Mode

Configuration starts and proceeds the same as in Master serial mode until the Master device is loaded. At that point, the Master transmits subsequent configuration data out on its DOUT pin. That data goes to the DIN pin of the second device. When that device is loaded, it transmits subsequent data on its DOUT pin to the third device. This process continues until all VF1 FPGAs in the chain have been configured.

Figure 43 shows VF1 slave-mode devices following a master-mode device. This is not the only case in which slave-mode configuration is used. It may also be used following VF1 FPGAs configured in Synchronous or Asynchronous peripheral modes, or when a host system configures a VF1 FPGA directly in serial mode.

Asynchronous Peripheral Mode

Asynchronous Peripheral mode is used to load one or more VF1 FPGAs with byte-wide data from a microprocessor bus (Figure 44). The VF1 FPGA serializes each byte internally, so this mode offers no speed advantage over serial modes. Data transfer is made on the trailing edge of the logical AND of signals /WS and /CS0 being low and /RS and /CS1 being high. Chip select signals can be cycled or maintained at a static level during the configuration process. Each byte of data is written into the VF1 FPGA's DIN [7:0] input pins.

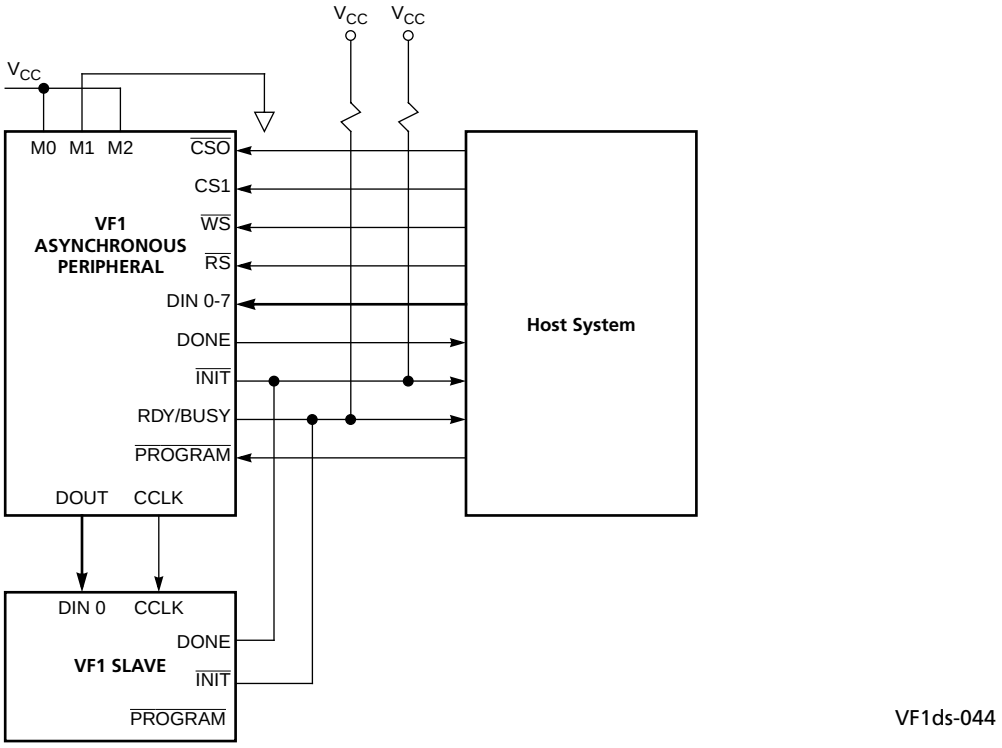


Figure 44. Asynchronous Peripheral Mode

When two or more VF1 FPGAs are daisy-chained for configuration, the lead device loads itself first and then it presents serial configuration data on its DOUT pin. It also generates the CCLK clock signal to control shifting of data into subsequent slave-mode devices in the daisy chain.

The RDY/(/BUSY) status output indicates when another byte can be loaded from the host system. A high indicates that the VF1 FPGA is ready to receive another byte, while a low indicates that it cannot accept a byte. The length of the low signal will vary depending on the shifting status of previously loaded bytes. In addition to appearing on its status pin, the RDY/(/BUSY) signal can be multiplexed on the DIN7 pin by setting chip select pin /WR high and setting pin /RD low.

Synchronous Peripheral Mode

In Synchronous Peripheral mode, a host system presents byte-wide data over a microprocessor bus and controls shifting of that data by inputting a clock signal to the VF1 FPGA's CCLK pin (Figure 45). The first data byte is clocked into the VF1 FPGA on the rising edge of the second CCLK pulse after /INIT goes high. Bytes are then clocked in on every eighth CCLK pulse. In this mode, the RDY/(/BUSY) signal acknowledges the loading of the byte by going high for one CCLK period on the same clock that loaded the byte. CCLK must remain active after the last byte is loaded to complete the shifting.

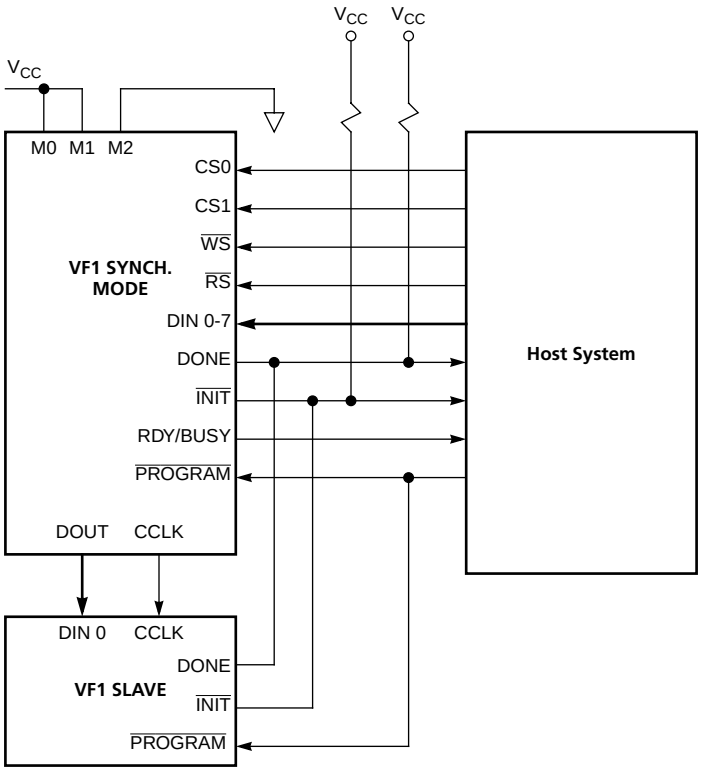


Figure 45. Synchronous Peripheral Mode

Synchronous Peripheral mode can be used in daisy-chain configurations. The first VF1 FPGA in the chain loads itself, and then presents serial data on its DOUT pin for loading into the following devices in the chain. CCLK is applied in parallel to all devices from the host system. The data appears on DOUT 1.5 cycles after it is loaded in parallel, which means that DOUT changes on a falling CCLK edge and the next VF1 FPGA loads data on the next rising edge.

JTAG Mode

In JTAG mode, VF1 FPGAs are configured using the JTAG pins TCLK, TMS TDI, and TDO. Three additional JTAG instructions support JTAG configuration mode:

- **PROG_MODE.** This instruction places the VF1 FPGA in programming mode.
- **PROGRAM.** Once the VF1 FPGA is in programming mode, this instruction shifts configuration data into the VF1 FPGA.
- **VERIFY.** After configuration this instruction is used to read back all configuration, VGB and I/O flip-flops, and embedded SRAM bits in the device.

A host system such as a microprocessor controls the configuration of the VF1 FPGA or devices and supplies configuration data. The host also provides the configuration clock.

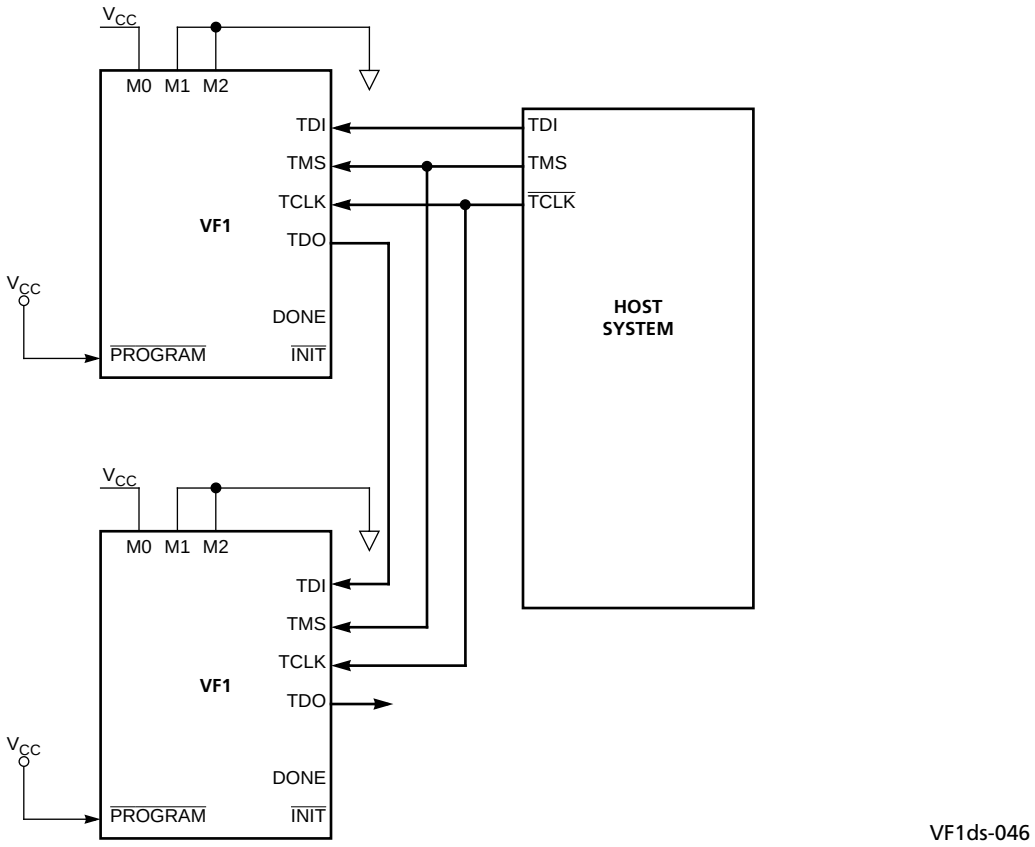


Figure 46. JTAG Mode

If two or more VF1 FPGAs are to be configured, they are arranged in a daisy chain with all devices selected for JTAG mode configuration (Figure 46). Data is applied to the TDI pin of the first device and the TDO pin of that device is connected to the TDI pin of the next device. The TMS and TCLK signals from the host are applied to all VF1 FPGAs in parallel.

In-System Programming

A VF1 FPGA is normally loaded with a configuration program when its host system is powered up. As described in the section above, this is often accomplished by loading the program from a separate SPROM. In the case of the Vantis VF1 family, the program may also be loaded through the JTAG port or the dedicated programming port.

The typical FPGA, however, is part of a larger system that includes a microprocessor. The system design can often be simplified by having the microprocessor, rather than a separate serial PROM, configure the VF1 FPGA. The microprocessor can configure the VF1 FPGA using host-driven Slave mode, Asynchronous Peripheral mode, Synchronous Peripheral mode, or JTAG mode. In most applications, JTAG mode will be used.

Using a host microprocessor to load the VF1 FPGA simplifies making design changes or installing ECOs after the device has been installed in a system. The new configuration program can simply be loaded into the microprocessor and then loaded into the VF1 FPGA, eliminating the need to swap PROMs or any other physical part of the system. It also allows dynamic changing of system

functionality by allowing multiple configuration programs to reside in the host system and be loaded into the VF1 FPGAs as needed.

Core Program

Vantis plans to offer high-value, reusable cores as part of its VF1 family. The first cores in this program are PCI cores that support both the 33MHz and 66MHz standards. Detailed information will be published later.

ORDERING INFORMATION

Vantis VF1 Series FPGAs

VF 1 036 A M AH C 1

Vantis FPGA

FAMILY
1 = 1000 sereis family

Gate Count
012 = 12K
020 = 20K
025 = 25K
036 = 36K

Supply Voltage
A = 3.3V

Embedded function
M = Memory

Speed
1 = Speed grade 1 (Slowest)
2 = Speed grade 2

OPERATING CONDITIONS
C = Commercial (0°C to +70°C)
I = Industrial (-40 °C to +85 °C)

PACKAGE TYPE
Ball Grid Array (BGA)
AH = 256, AM= 352
Plastic Quad Flat Pack (PQFP)
YO = 160, YS=208, YT=240
Thin Quad Flat Pack (TQFP)
VN = 144

TECHNICAL SPECIFICATIONS

The following pages contain preliminary technical specifications for the VF1 family.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . .-65°C to +150°C

Device Junction Temperature . . . . . +120°C

Supply Voltage with Respect to Ground . . . . . .-0.5 V to +4.0 V

DC Input Voltage . . . . . -0.5 to 5.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (0°C to +70°C) . . . . . .200 mA

Note:

Stresses above those listed under Absolute Maximum Ratings may cause permantent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC}) with Respect to Ground. . . . . +3.0 V to +3.6 V

Note:

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

Parameter	Parameter Description	Min	Max	Unit
V_{IH}	Input High Voltage	2.0		V
V_{IL}	Input Low Voltage		0.8	V
I_{IH1}	Input High Leakage Current (Vin = Max V_{CC} = 3.6V)		10.0	µA
I_{IL1}	Input Low Leakage Current (Vin = 0V)		-10.0	µA
I_{IH2}	Input High Leakage Current with Pull Up (Vin = Max V_{CC}=3.6V)		10.0	µA
I_{IL2}	Input Low Leakage Current with Pull Up (Vin = 0V)		-100.0	µA
I_{IH3}	Input High Leakage Current with Bus Friendly (Vin = Max V_{CC}=3.6V)		10.0	µA
I_{IL3}	Input Low Leakage Current with Bus Friendly (Vin = 0V)		-10.0	µA
V_{OH}	Output High Voltage @ I_{OH} = -4.0mA (LVTTL) (V_{CC} = 3.0V)	2.4		V
	Output High Voltage @ I_{OH} = -500uA (LVCMOS) (V_{CC} = 3.0V)	$0.9V_{CC}$		V
V_{OL}	Output Low Voltage @ I_{OL} = 12.0mA (LVTTL) (V_{CC} = 3.0V)		0.4	V
	Output Low Voltage @ I_{OL} = 1.5mA (LVCMOS) (V_{CC} = 3.0V)		$0.1V_{CC}$	V
I_{OZH1}	Off State Output Leakage with Bus High		10.0	µA
I_{OZL1}	Off State Output Leakage with Bus Low		-10.0	µA
I_{OZH2}	Off State Output Leakage with Bus High (Pull Up) (Note 1)		10.0	µA
I_{OZL2}	Off State Output Leakage with Bus Low (Pull Up) (Note 1)		-100.0	µA
I_{OZH3}	Off State Output Leakage with Bus High (Bus Friendly)		10.0	µA
I_{OZL3}	Off State Output Leakage with Bus Low (Bus Friendly)		-10.0	µA
I_{SC}	Output Short Circuit Current (Vout = 0.5V) (V_{CC} = Max V_{CC} = 3.6V)		300.0	mA
SI_{CC}	Standby Supply Current (Nominal V_{CC})		6.0	mA

Notes:

1. *JTAG and dedicated configuration pins have only Pull Up option.*
2. *Usage of PLL adds 20mA per PLL to the dynamic I_{CC}.*

AC CHARACTERISTICS

The following tables contain preliminary AC timing parameters for the VF1 FPGA family. It is recommended that the timing analysis tools in Vantis' DesignDirect software be used to calculate timing for a design. However, the following tables can be used to develop approximate delays for small circuits. Interconnect delays and interconnect driver delays are not included in these tables. Timing information will be updated as final characterization is done. The latest timing information is published on the Vantis Web site (www.vantis.com).

Input AC Parameters

IOB General Input Delays

Parameter	Parameter Description	Test Conditions	-1	-2	Unit
t_{IN}	IOB Standard Input Delay	IOB to Direct Connect to CBB 4LUT	0.9	0.7	ns
t_{INXL}	IOB Transparent Input Latch Delay without Delay		1.5	1.2	ns
t_{INXLD}	IOB Transparent Input Latch Delay with Delay		6.4	5.3	ns
t_{ILLEA}	Input Long Line Enable Time		1.8	1.5	ns
t_{ILLER}	Input Long Line Disable Time		2.4	2.0	ns

IOB Input Set/Reset Delays

Parameter	Parameter Description	-1	-2	Unit
t_{ISRGO}	IOB Input Register (Latch) Global Set/Reset → Interconnect Lines	1.5	1.2	ns
t_{ISRLO}	IOB Input Register (Latch) Local Set/Reset → Interconnect Lines	2.4	2.0	ns
$t_{ISRGREC}$	IOB Input Register (Latch) Global Set/Reset Recovery Time	0.5	0.4	ns
$t_{ISRLREC}$	IOB Input Register (Latch) Local Set/Reset Recovery Time	1.0	0.8	ns

IOB Input Register (Latch) Global Clock (Gate) Delays

Parameter	Parameter Description	-1	-2	Unit
t_{IRLGS}	IOB Input Register (Latch) Global Clock (Gate) Setup Time Without Delay	0.0	0.0	ns
t_{IRLGH}	IOB Input Register (Latch) Global Clock (Gate) Hold Time Without Delay	0.8	0.6	ns
t_{IRLGSD}	IOB Input Register (Latch) Global Clock (Gate) Setup Time With Delay	5.0	4.1	ns
t_{IRLGHD}	IOB Input Register (Latch) Global Clock (Gate) Hold Time With Delay	0.0	0.0	ns
t_{IRLGCO}	IOB Input Register (Latch) Global Clock (Gate) → Interconnect Lines	1.8	1.5	ns
$t_{IRLGCES}$	IOB Input Register (Latch) Global Clock Enable Setup Time	0.9	0.7	ns
$t_{IRLGCEH}$	IOB Input Register (Latch) Global Clock Enable Hold Time	0.0	0.0	ns

IOB Input Register (Latch) Local Clock (Gate) Delays

Parameter	Parameter Description	-1	-2	Unit
t_{IRLLS}	IOB Input Register (Latch) Local Clock (Gate) Setup Time Without Delay	0.0	0.0	ns
t_{IRLLH}	IOB Input Register (Latch) Local Clock (Gate) Hold Time Without Delay	1.8	1.5	ns
t_{IRLLSD}	IOB Input Register (Latch) Local Clock (Gate) Setup Time With Delay	4.0	3.3	ns
t_{IRLLHD}	IOB Input Register (Latch) Local Clock (Gate) Hold Time With Delay	0.0	0.0	ns
t_{IRLLCO}	IOB Input Register (Latch) Local Clock (Gate) → Interconnect Lines	2.8	2.3	ns

IOB Input Register (Latch) Local Clock (Gate) Delays (Continued)

Parameter	Parameter Description	-1	-2	Unit
$t_{IRLLCES}$	IOB Input Register (Latch) Local Clock Enable Setup Time	0.0	0.0	ns
$t_{IRLLCEH}$	IOB Input Register (Latch) Local Clock Enable Hold Time	0.8	0.6	ns

Output AC Parameters

IOB General Output Delays

Parameter	Parameter Description	Test Conditions	-1	-2	Unit
t_{OUT}	IOB Standard Output Delay to Pad	CBB 4LUT Direct Connect to IOB	4.0	3.3	ns
t_{OEA}	Output Buffer Enable Time		4.5	3.7	ns
t_{OER}	Output Buffer Disable Time		6.2	5.1	ns
t_{SLW}	Output Buffer Slow Slew Rate Adder		1.8	1.5	ns

IOB Output Set/Reset Delays

Parameter	Parameter Description	-1	-2	Unit
t_{ORSRGO}	IOB Output Register Global Set/Reset → Pad	4.1	3.4	ns
t_{ORSRLO}	IOB Output Register Local Set/Reset → Pad	5.1	4.2	ns
t_{ORGREC}	IOB Output Register Global Set/Reset Recovery Time	0.5	0.4	ns
t_{ORLREC}	IOB Output Register Local Set/Reset Recovery Time	1.0	0.8	ns

IOB Output Register Global Clock Delays

Parameter	Parameter Description	-1	-2	Unit
t_{ORGS}	IOB Output Register Global Clock Setup Time	0.4	0.3	ns
t_{ORGH}	IOB Output Register Global Clock Hold Time	0.4	0.3	ns
t_{ORGCO}	IOB Output Register Global Clock → Pad	4.5	3.7	ns
t_{ORGCES}	IOB Output Register Global Clock Enable Setup Time	1.0	0.8	ns
t_{ORGCEH}	IOB Output Register Global Clock Enable Hold Time	0.0	0.0	ns

IOB Output Register Local Clock Delays

Parameter	Parameter Description	-1	-2	Unit
t_{ORLS}	IOB Output Register Local Clock Setup Time	0.0	0.0	ns
t_{ORLH}	IOB Output Register Local Clock Hold Time	1.4	1.1	ns
t_{ORLCO}	IOB Output Register Local Clock → Pad	5.4	4.5	ns
t_{ORLCES}	IOB Output Register Local Clock Enable Setup Time	0.0	0.0	ns
t_{ORLCEH}	IOB Output Register Local Clock Enable Hold Time	0.8	0.6	ns

CBB AC Parameters

Combinatorial Configurable Building Block (CBB) Delays

Parameter	Parameter Description	Test Conditions	-1	-2	Unit
t_{3LUT}	CBB Input → LUT → CBB Output (3-LUT)	IOB to Direct Connect to CBB to Direct Connect to IOB	2.2	1.8	ns
t_{4LUT}	CBB Input → LUT → CBB Output (4-LUT)		3.2	2.6	ns
t_{5LUT}	CBB Input → LUT → CBB Output (5-LUT)		3.6	3.0	ns
t_{6LUT}	CBB Input → LUT → CBB Output (6-LUT)		5.8	4.8	ns
t_{WG}	CBB Input → LUT → CBB Output (Wide Gate)		4.1	3.4	ns
t_{VFP}	CBB 3LUT Feedthrough		2.1	1.7	ns

Registered Configurable Building Block (CBB) VGB Global Clock Delays

Parameter	Parameter Description	-1	-2	Unit
t_{3LUTGS}	CBB Input → VGB Global Clock Setup Time (3-LUT)	1.2	1.0	ns
t_{4LUTGS}	CBB Input → VGB Global Clock Setup Time (4-LUT)	2.2	1.8	ns
t_{5LUTGS}	CBB Input → VGB Global Clock Setup Time (5-LUT)	2.6	2.1	ns
t_{6LUTGS}	CBB Input → VGB Global Clock Setup Time (6-LUT)	4.7	3.9	ns
t_{WGGS}	CBB Input → VGB Global Clock Setup Time (Wide Gate)	3.0	2.5	ns
t_{3LUTGH}	CBB Input → VGB Global Clock Hold Time (3-LUT)	0.0	0.0	ns
t_{4LUTGH}	CBB Input → VGB Global Clock Hold Time (4-LUT)	0.0	0.0	ns
t_{5LUTGH}	CBB Input → VGB Global Clock Hold Time (5-LUT)	0.0	0.0	ns
t_{6LUTGH}	CBB Input → VGB Global Clock Hold Time (6-LUT)	0.0	0.0	ns
t_{WGGH}	CBB Input → VGB Global Clock Hold Time (Wide Gate)	0.0	0.0	ns
t_{VGCO}	VGB Global Clock → CBB Output	1.8	1.5	ns
t_{VGCES}	VGB Global Clock Enable Setup Time	0.5	0.4	ns
t_{VGCEH}	VGB Global Clock Enable Hold Time	0.4	0.3	ns
t_{VGSR}	VGB Global Set/Reset → CBB Output	1.4	1.1	ns
t_{VGREC}	VGB Global Set/Reset Recovery Time	0.3	0.2	ns

Super VGB Control Signals

Parameter	Parameter Description	-1	-2	Unit
t_{VFF}	VGB Feedthrough	1.1	0.9	ns
t_{SDEA}	Shared Driver Enable Time	2.4	2.0	ns
t_{SDER}	Shared Driver Disable Time	2.8	2.3	ns

Registered Configurable Building Block (CBB) VGB Local Clock Delays

Parameter	Parameter Description	-1	-2	Unit
t_{3LUTLS}	CBB Input → VGB Local Clock Setup Time (3-LUT)	0.5	0.4	ns
t_{4LUTLS}	CBB Input → VGB Local Clock Setup Time (4-LUT)	1.4	1.1	ns
t_{5LUTLS}	CBB Input → VGB Local Clock Setup Time (5-LUT)	1.8	1.5	ns
t_{6LUTLS}	CBB Input → VGB Local Clock Setup Time (6-LUT)	4.0	3.3	ns
t_{WGLS}	CBB Input → VGB Local Clock Setup Time (Wide Gate)	2.3	1.9	ns
t_{3LUTLH}	CBB Input → VGB Local Clock Hold Time (3-LUT)	0.0	0.0	ns
t_{4LUTLH}	CBB Input → VGB Local Clock Hold Time (4-LUT)	0.0	0.0	ns
t_{5LUTLH}	CBB Input → VGB Local Clock Hold Time (5-LUT)	0.0	0.0	ns
t_{6LUTLH}	CBB Input → VGB Local Clock Hold Time (6-LUT)	0.0	0.0	ns
t_{WGLH}	CBB Input → VGB Local Clock Hold Time (Wide Gate)	0.0	0.0	ns
t_{VLCO}	VGB Local Clock → CBB Output	2.4	2.0	ns
t_{VLCES}	VGB Local Clock Enable Setup Time	0.0	0.0	ns
t_{VLCEH}	VGB Local Clock Enable Hold Time	1.0	0.8	ns
t_{VLSR}	VGB Local Set/Reset → CBB Output	2.0	1.6	ns
t_{VLREC}	VGB Local Set/Reset Recovery Time	0.0	0.0	ns

VGB Carry Logic AC Parameters

VGB Combinatorial High Speed Carry Logic

Parameter	Parameter Description	Test Conditions	-1	-2	Unit
t_{OPSUM}	Operand/Control Input → Sum Logic Output → CBB Output	Direct Connect to CBB 3LUT Carry Logic	2.6	2.1	ns
$t_{OPCARRY}$	Operand/Control Input → Carry Logic Output		2.1	1.7	ns
t_{CSUM}	Carry Logic Input → Sum Logic Output → CBB Output		1.0	0.8	ns
t_{CCARRY}	Carry Logic Input → Carry Logic Output		0.4	0.3	ns

VGB Registered Global Clock High Speed Carry Logic

Parameter	Parameter Description	-1	-2	Unit
t_{OPGS}	Operand/Control Input → Sum Logic → VGB Global Clock Setup Time	1.6	1.3	ns
t_{OPGH}	Operand/Control Input → Sum Logic → VGB Global Clock Hold Time	0.0	0.0	ns
t_{CGS}	Carry Logic Input → Sum Logic → VGB Global Clock Setup Time	0.0	0.0	ns
t_{CGH}	Carry Logic Input → Sum Logic → VGB Global Clock Hold Time	0.6	0.5	ns

VGB Registered Local Clock High Speed Carry Logic

Parameter	Parameter Description	-1	-2	Unit
t_{OPLS}	Operand/Control Input → Sum Logic → VGB Local Clock Setup Time	0.9	0.7	ns
t_{OPLH}	Operand/Control Input → Sum Logic → VGB Local Clock Hold Time	0.0	0.0	ns
t_{CLS}	Carry Logic Input → Sum Logic → VGB Local Clock Setup Time	0.0	0.0	ns
t_{CLH}	Carry Logic Input → Sum Logic → VGB Local Clock Hold Time	1.2	1.0	ns

VF1 FAMILY PACKAGE PIN LISTS

VF1 family FPGA devices are available in five package types as listed in the table below. Pin lists for each package type and VF1 family device follow the table. The pin lists are arranged by package type and are sorted by signal type and name.

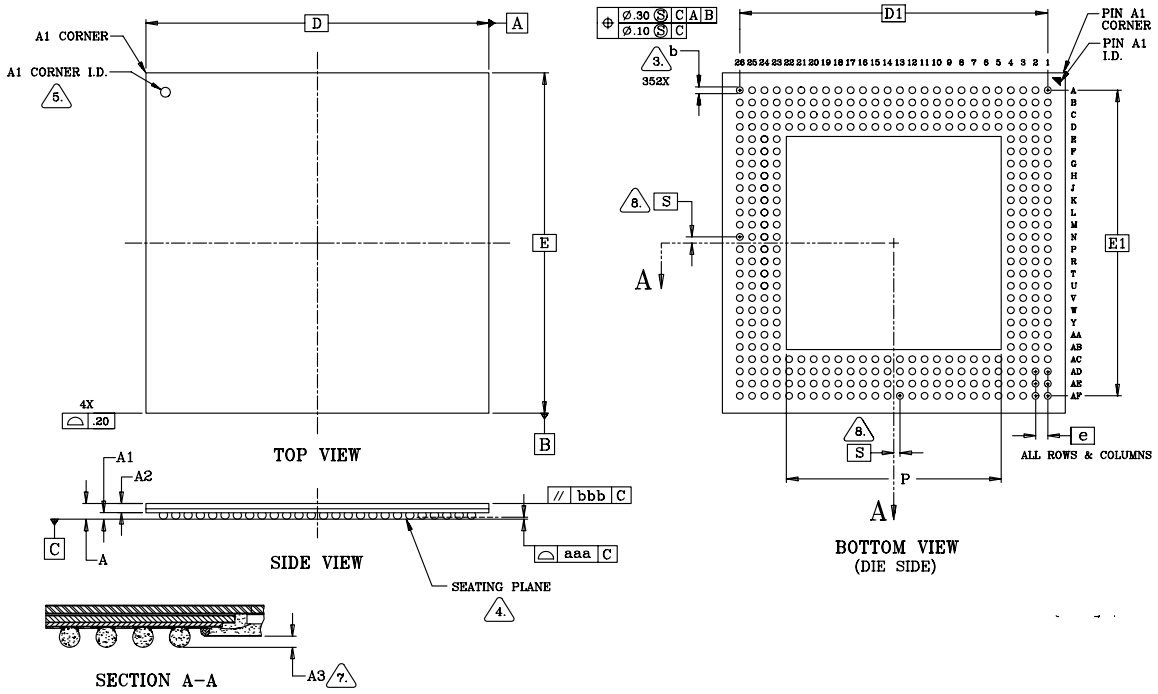
Within a given package, certain common signals appear on the same pins regardless of the VF1 FPGA in the package. For example, the VF1012, VF1020, VF1025, and VF1036 devices are available in the 256 BGA package. The SET/RESET signal, all CLKx inputs, JTAG interface signals, and all configuration signals appear on the same pins in the 256 BGA package for every member of the family. These common signals are listed at the beginning of each package type. These are followed by IOB (Input/Output Block) pin lists. IOB placement varies by family member within a single package type.

Each pin list includes a specification drawing of the package.

VF1 Family Package Options/Total Pins

Package	VF1012	VF1020	VF1025	VF1036
352 BGA			244	292
256 BGA	172	208	208	208
208 PQFP	168	168	168	168
160 PQFP	128	128		
144 TQFP	112			

352 BGA PACKAGE



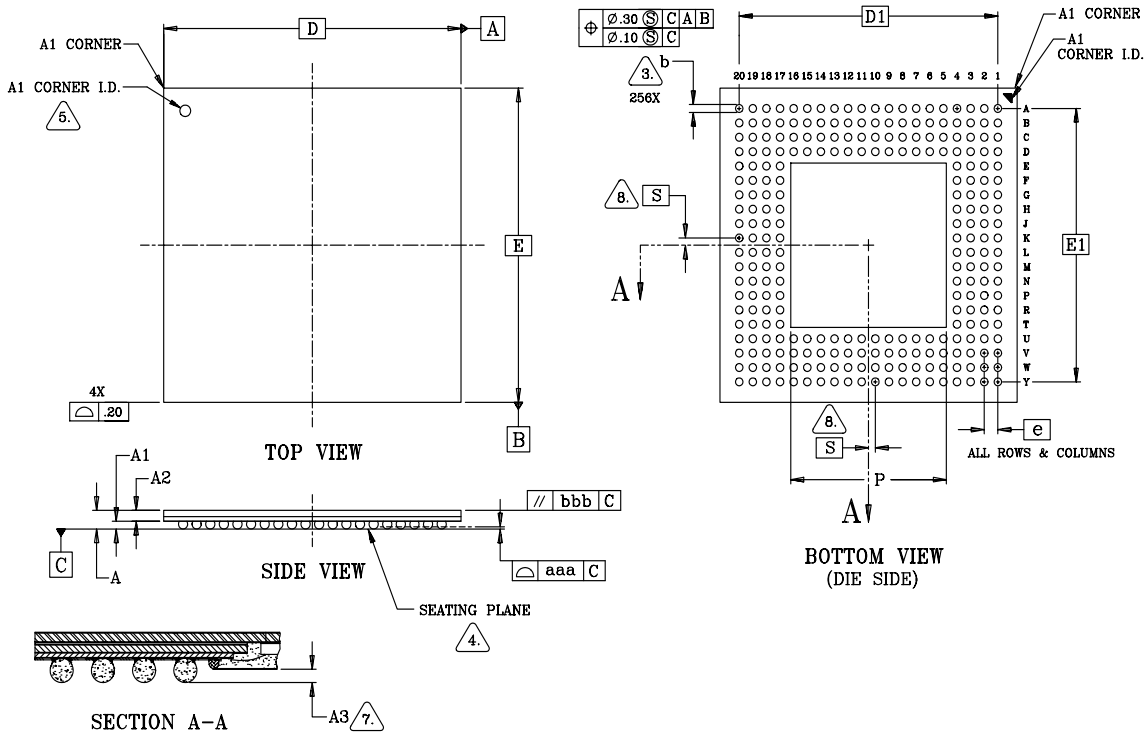
352 BGA Common Signals (VF1025, VF1036)

Group	Signal	Pin
Clock Inputs	SET/RESET	D1
	CLK0	B4
	CLK1	D25
	CLK2	AF23
	CLK3	AC1
JTAG Interface	TDI	D26
	TMS	D2
	TDO	AE4
	TCLK	A4
Configuration, Dedicated	PROGRAM	B23
	DONE	AC25
	CCLK	AF4
Configuration, Multiplexed	HDC	E26
	/LDC	E23
	/INIT	E24
	M0	E25
	M1	F26
	M2	AB26
	/CSO	AB25
	CS1	AB24
	/RS	AB23
	/WS	AC26
	RDY/(/BUSY)	AC2
	DOUT	AB1
	D7	AB4
	D6	AB3
	D5	AB2
	D4	F4
	D3	E1
	D2	E2
	D1	E3
	D0	E4
Power Pins	V_{CC} (17)	C3, AC3, C4, AC4, C23, AC23, C24, AC24, D3, AD3, D4, AD4, D13, AD23, D23, AD24, D24
	GND (35)	A1, B26, AE1, A2, C1, AE2, A3, C2, AE3, A24, C25, AE24, A25, C26, AE25, A26, N1, AE26, B1, P26, AF1, B2, AD1, AF2, B3, AD2, AF3, B24, AD25, AF13, B25, AD26, AF24, AF25, AF26

352 BGA INPUT/OUTPUT BLOCKS (VF1025, VF1036)

Signal	VF1025	VF1036	Signal	VF1025	VF1036	Signal	VF1025	VF1036	Signal	VF1025	VF1036	Signal	VF1025	VF1036	Signal	VF1025	VF1036
IOB1	A5	A5	IOB51	D20	D17	IOB101	V25	M26	IOB151	AE15	AE21	IOB201	V4	AF8	IOB251		P2
IOB2	D5	D5	IOB52	A21	A18	IOB102	V24	M25	IOB152	AD15	AC21	IOB202	U1	AE8	IOB252		P3
IOB3	C5	C5	IOB53	B21	B18	IOB103	V23	M24	IOB153	AC15	AD21	IOB203	U2	AD8	IOB253		P4
IOB4	B5	B5	IOB54	C21	C18	IOB104	W26	M23	IOB154	AF14	AF20	IOB204	U3	AC8	IOB254		N2
IOB5	A6	A6	IOB55	D21	D18	IOB105	W25	N26	IOB155	AE14	AE20	IOB205	U4	AF7	IOB255		N3
IOB6	B6	B6	IOB56	A22	A19	IOB106	W24	N25	IOB156	AD14	AD20	IOB206	T1	AE7	IOB256		N4
IOB7	D6	D6	IOB57	B22	B19	IOB107	W23	N24	IOB157	AC14	AC20	IOB207	T2	AD7	IOB257		M1
IOB8	C6	C6	IOB58	C22	C19	IOB108	Y26	N23	IOB158	AE13	AF19	IOB208	T3	AC7	IOB258		M2
IOB9	A7	A7	IOB59	D22	D19	IOB109	Y25	P25	IOB159	AD13	AE19	IOB209	T4	AF6	IOB259		M3
IOB10	B7	B7	IOB60	A23	A20	IOB110	Y24	P24	IOB160	AC13	AD19	IOB210	R1	AE6	IOB260		M4
IOB11	C7	C7	IOB61	E26	B20	IOB111	Y23	P23	IOB161	AF12	AC19	IOB211	R2	AD6	IOB261		L1
IOB12	D7	D7	IOB62	E23	C20	IOB112	AA26	R26	IOB162	AE12	AF18	IOB212	R3	AC6	IOB262		L2
IOB13	A8	A8	IOB63	E24	D20	IOB113	AA25	R25	IOB163	AD12	AE18	IOB213	R4	AF5	IOB263		L3
IOB14	B8	B8	IOB64	E25	A21	IOB114	AA24	R24	IOB164	AC12	AD18	IOB214	P1	AE5	IOB264		L4
1OB15	C8	C8	IOB65	F26	B21	IOB115	AA23	R23	IOB165	AF11	AC18	IOB215	P2	AD5	IOB265		K1
IOB16	D11	D8	IOB66	F25	C21	IOB116	AB26	T26	IOB166	AE8	AF17	IOB216	P3	AC5	IOB266		K2
IOB17	A12	A9	IOB67	F23	D21	IOB117	AB25	T25	IOB167	AD8	AE17	IOB217	P4	AC2	IOB267		K3
IOB18	B12	B9	IOB68	F24	A22	IOB118	AB24	T24	IOB168	AC8	AD17	IOB218	N2	AB1	IOB268		K4
IOB19	C12	C9	IOB69	G26	B22	IOB119	AB23	T23	IOB169	AF7	AC17	IOB219	N3	AB4	IOB269		J1
IOB20	D12	D9	IOB70	G25	C22	IOB120	AC26	U26	IOB170	AE7	AF16	IOB220	N4	AB3	IOB270		J2
IOB21	A13	A10	IOB71	G24	D22	IOB121	AE23	U25	IOB171	AD7	AE16	IOB221	M1	AB2	IOB271		J3
IOB22	B13	B10	IOB72	G23	A23	IOB122	AF22	U24	IOB172	AC7	AD16	IOB222	M2	AA1	IOB272		J4
IOB23	C13	C10	IOB73	H26	E26	IOB123	AC22	U23	IOB173	AF6	AC16	IOB223	M3	AA2	IOB273		H1
IOB24	A14	D10	IOB74	H25	E23	IOB124	AD22	V26	IOB174	AE6	AF15	IOB224	M4	AA4	IOB274		H2
IOB25	B14	A11	IOB75	H24	E24	IOB125	AE22	V25	IOB175	AD6	AE15	IOB225	L1	AA3	IOB275		H3
IOB26	C14	B11	IOB76	L23	E25	IOB126	AF21	V24	IOB176	AC6	AD15	IOB226	H2	Y1	IOB276		H4
IOB27	D14	C11	IOB77	M26	F26	IOB127	AE21	V23	IOB177	AF5	AC15	IOB227	H3	Y2	IOB277		G1
IOB28	A15	D11	IOB78	M25	F25	IOB128	AC21	W26	IOB178	AE5	AF14	IOB228	H4	Y3	IOB278		G2
IOB29	B15	A12	IOB79	M24	F23	IOB129	AD21	W25	IOB179	AD5	AE14	IOB229	G1	Y4	IOB279		G3
IOB30	C15	B12	IOB80	M23	F24	IOB130	AF20	W24	IOB180	AC5	AD14	IOB230	G2	W1	IOB280		G4
IOB31	D15	C12	IOB81	N26	G26	IOB131	AE20	W23	IOB181	AC2	AC14	IOB231	G3	W2	IOB281		F1
IOB32	A16	D12	IOB82	N25	G25	IOB132	AD20	Y26	IOB182	AB1	AE13	IOB232	G4	W3	IOB282		F2
IOB33	B16	A13	IOB83	N24	G24	IOB133	AC20	Y25	IOB183	AB4	AD13	IOB233	F1	W4	IOB283		F3
IOB34	C16	B13	IOB84	N23	G23	IOB134	AF19	Y24	IOB184	AB3	AC13	IOB234	F2	V1	IOB284		F4
IOB35	D16	C13	IOB85	P25	H26	IOB135	AE19	Y23	IOB185	AB2	AF12	IOB235	F3	V2	IOB285		E1
IOB36	A17	A14	IOB86	P24	H25	IOB136	AD19	AA26	IOB186	AA1	AE12	IOB236	F4	V3	IOB286		E2
IOB37	B17	B14	IOB87	P23	H24	IOB137	AC19	AA25	IOB187	AA2	AD12	IOB237	E1	V4	IOB287		E3
IOB38	C17	C14	IOB88	R26	H23	IOB138	AF18	AA24	IOB188	AA4	AC12	IOB238	E2	U1	IOB288		E4
IOB39	D17	D14	IOB89	R25	J26	IOB139	AE18	AA23	IOB189	AA3	AF11	IOB239	E3	U2			
IOB40	A18	A15	IOB90	R24	J25	IOB140	AD18	AB26	IOB190	Y1	AE11	IOB240	E4	U3			
IOB41	B18	B15	IOB91	R23	J24	IOB141	AC18	AB25	IOB191	Y2	AD11	IOB241		U4			
IOB42	C18	C15	IOB92	T26	J23	IOB142	AF17	AB24	IOB192	Y3	AC11	IOB242		T1			
IOB43	D18	D15	IOB93	T25	K26	IOB143	AE17	AB23	IOB193	Y4	AF10	IOB243		T2			
IOB44	A19	A16	IOB94	T24	K25	IOB144	AD17	AC26	IOB194	W1	AE10	IOB244		T3			
IOB45	B19	B16	IOB95	T23	K24	IOB145	AC17	AE23	IOB195	W2	AD10	IOB245		T4			
IOB46	C19	C16	IOB96	U26	K23	IOB146	AF16	AF22	IOB196	W3	AC10	IOB246		R1			
IOB47	D19	D16	IOB97	U25	L26	IOB147	AE16	AC22	IOB197	W4	AF9	IOB247		R2			
IOB48	A20	A17	IOB98	U24	L25	IOB148	AD16	AD22	IOB198	V1	AE9	IOB248		R3			
IOB49	B20	B17	IOB99	U23	L24	IOB149	AC16	AE22	IOB199	V2	AD9	IOB249		R4			
IOB50	C20	C17	IOB100	V26	L23	IOB150	AF15	AF21	IOB200	V3	AC9	IOB250		P1			

256 BGA PACKAGE



256 BGA COMMON SIGNALS (VF1012, VF1020, VF1025, VF1036)

Group	Signal	Pin
Clock Inputs	SET/RESET	D2
	CLK0	B4
	CLK1	D19
	CLK2	V17
	CLK3	U3
JTAG Interface	TDI	D18
	TMS	D3
	TDO	V4
	TCLK	C4
Configuration, Dedicated	/PROGRAM	C17
	DONE	U18
	CCLK	W4
Configuration, Multiplexed	HDC	D20
	/LDC	E17
	/INIT	E18
	M0	E19
	M1	E20
	M2	T19
	/CSO	T18
	CS1	T17
	/RS	U20
	/WS	U19
	RDY/(/BUSY)	U2
	DOUT	U1
	D7	T4
	D6	T3
	D5	T2
	D4	E1
	D3	E2
	D2	E3
	D1	E4
	DO	D1
Power Pins	VCC (20)	B2, B3, B18, B19, C2, C3, C18, C19,D4, D17, U4, U17, V2, V3, V18, V19, W2, W3, W18, W19.
	GND (20)	A1, A2, A3, A18, A19, A20, B1, B20, C1, C20, V1, V20, W1, W20, Y1, Y2, Y3, Y18, Y19, Y20.

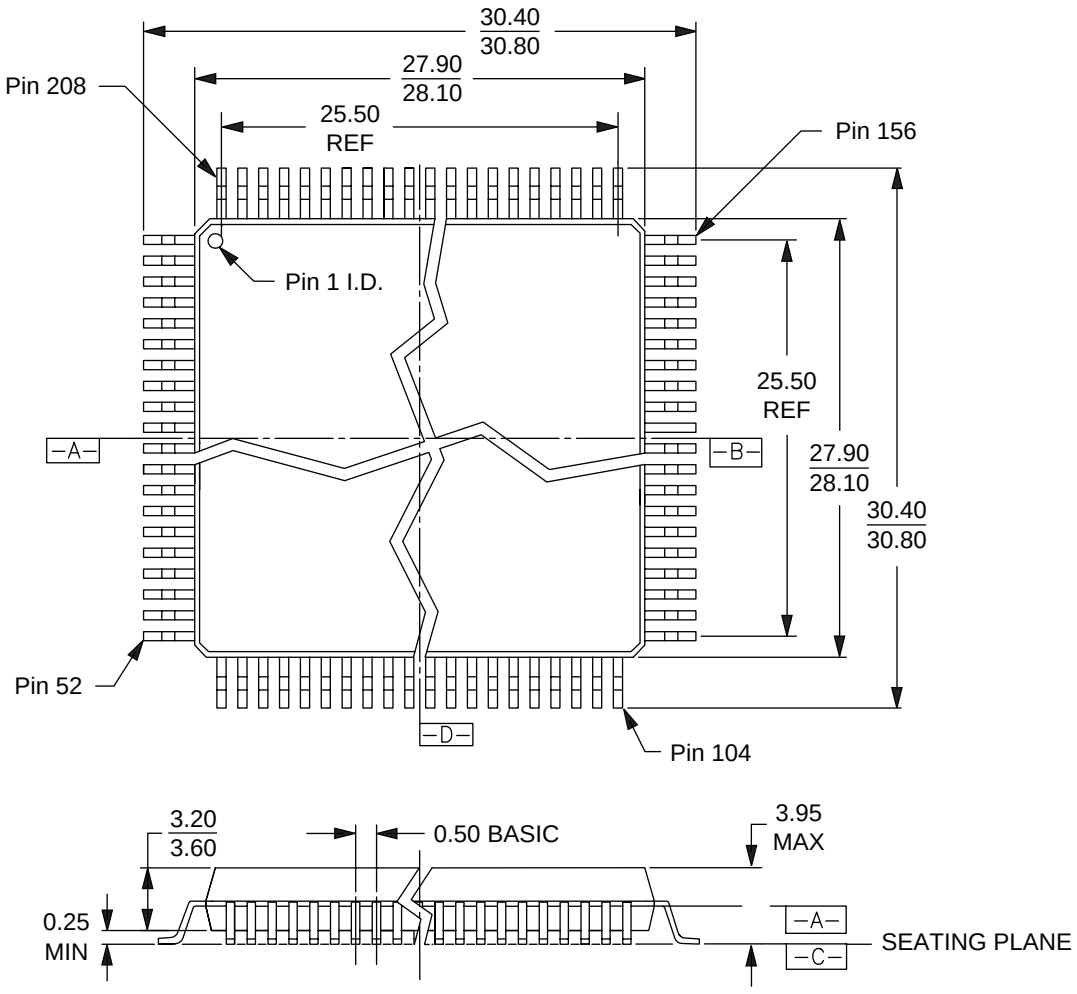
256 BGA INPUT/OUTPUT BLOCKS (VF1012, VF1020, VF1025, VF1036)

Signal	VF1012	VF1020	VF1025	VF1036	Signal	VF1012	VF1020	VF1025	VF1036	Signal	VF1012	VF1020	VF1025	VF1036
IOB1	A4	A4	A4	A4	IOB51	G19	C16	A15	B14	IOB101	V12	R18		H20
IOB2	D5	D5	D5	D5	IOB52	G20	D16	B15		IOB102	W12	R17		J17
IOB3	C5	C5	C5	C5	IOB53	H17	A17	C15		IOB103	Y12	T20	N20	J18
IOB4	B5	B5	B5	B5	IOB54	H18	B17	D15		IOB104	V11	T19	N19	J19
IOB5	A5	A5	A5	A5	IOB55	H19	D20	A16	C14	IOB105	U11	T18	N18	J20
IOB6	D6	D6	D6	D6	IOB56	H20	E17	B16	D14	IOB106	W11	T17	N17	K20
IOB7	D7	C6	C6		IOB57	J17	E18	C16	A15	IOB107	Y11	U20	P20	K17
IOB8	C7	B6	B6		IOB58	K20	E19	D16		IOB108	W10	U19	P19	K18
IOB9	B7	A6	A6		IOB59	K17	E20	A17		IOB109	V10	W17	P18	K19
IOB10	A7	D7	D7	C6	IOB60	K18	F17	B17		IOB110	U10	Y17	P17	L20
IOB11	D8	C7	C7	B6	IOB61	K19	F18	D20	B15	IOB111	Y10	U16	R20	L19
IOB12	C8	B7	B7	A6	IOB62	L20	F19	E17	C15	IOB112	U9	V16	R19	L17
IOB13	B8	A7	A7		IOB63	L19	F20	E18	D15	IOB113	Y8	W16	R18	L18
IOB14	A8	D8	D8		IOB64	L17	G17	E19		IOB114	W8	Y16	R17	M20
1OB15	D9	C8	C8		IOB65	L18	G18	E20		IOB115	V8	U15	T20	M19
IOB16	A10	B8	B8	D7	IOB66	M20	G19	F17		IOB116	U8	V15	T19	M18
IOB17	D10	A8	A8	C7	IOB67	M19	G20	F18	A16	IOB117	Y7	W15	T18	M17
IOB18	C10	D9	D9	B7	IOB68	M18	H17	F19	B16	IOB118	W7	Y15	T17	N20
IOB19	B10	C9	C9		IOB69	M17	H18	F20	C16	IOB119	V7	U14	U20	N19
IOB20	A11	B9	B9		IOB70	N17	H19	G17	D16	IOB120	U7	V14	U19	N18
IOB21	B11	A9	A9		IOB71	P20	H20	G18	A17	IOB121	U6	W14	W17	N17
IOB22	D11	A10	A10	A7	IOB72	P19	J17	G19	B17	IOB122	Y5	Y14	Y17	P20
IOB23	C11	D10	D10	D8	IOB73	P18	J18	G20	D20	IOB123	W5	U13	U16	P19
IOB24	A12	C10	C10	C8	IOB74	P17	J19	H17	E17	IOB124	V5		V16	
IOB25	B12	B10	B10		IOB75	R20	J20	H18	E18	IOB125	U5		W16	
IOB26	C12	A11	A11		IOB76	R19	K20	H19	E19	IOB126	Y4		Y16	
IOB27	D12	B11	B11		IOB77	R18	K17	H20	E20	IOB127	U2	V13	U15	P18
IOB28	D13	D11		B8	IOB78	R17	K18	J17	F17	IOB128	U1	W13	V15	P17
IOB29	A14	C11		A8	IOB79	T20	K19	J18		IOB129	T4	Y13	W15	R20
IOB30	B14	A12		D9	IOB80	T19	L20	J19		IOB130	T3	U12	Y15	
IOB31	C14	B12	D11	C9	IOB81	T18	L19	J20		IOB131	T2	V12	U14	
IOB32	D14	C12	C11	B9	IOB82	T17	L17	K20	F18	IOB132	T1	W12	V14	
IOB33	A15	D12	A12	A9	IOB83	U20	L18	K17	F19	IOB133	R4	Y12	W14	R19
IOB34	B15	A13	B12	A10	IOB84	U19	M20	K18	F20	IOB134	R3	V11	Y14	R18
IOB35	C15	B13	C12	D10	IOB85	W17	M19	K19		IOB135	R2	U11	U13	R17
IOB36	D15	C13	D12	C10	IOB86	Y17	M18	L20		IOB136	R1	W11	V13	
IOB37	A16			B10	IOB87	U16	M17	L19		IOB137	P4	Y11	W13	
IOB38	B16			A11	IOB88	V16	N20		G17	IOB138	P3	W10	Y13	
IOB39	C16			B11	IOB89	W16	N19		G18	IOB139	P2	V10		T20
IOB40	D16	D13		D11	IOB90	Y16	N18		G19	IOB140	P1	U10		T19
IOB41	A17	A14		C11	IOB91	U15		L17		IOB141	N4	Y10		T18
IOB42	B17	B14		A12	IOB92	V15		L18		IOB142	M4	Y9		T17
IOB43	D20	C14	A13	B12	IOB93	W15		M20		IOB143	M3	W9		U20
IOB44	E17	D14	B13	C12	IOB94	Y15	N17	M19	G20	IOB144	M2	V9		U19
IOB45	E18	A15	C13	D12	IOB95	U14	P20	M18	H17	IOB145	M1	U9	U12	W17
IOB46	E19	B15	D13	A13	IOB96	V14	P19	M17	H18	IOB146	L3	Y8	V12	Y17
IOB47	E20	C15	A14	B13	IOB97	W14	P18			IOB147	L4	W8	W12	U16
IOB48	F17	D15	B14	C13	IOB98	Y14	P17			IOB148	L2	V8	Y12	V16
IOB49	G17	A16	C14	D13	IOB99	U13	R20			IOB149	L1	U8	V11	W16
IOB50	G18	B16	D14	A14	IOB100	U12	R19		H19	IOB150	K2	Y7	U11	Y16

256 BGA INPUT/OUTPUT BLOCKS (VF1012, VF1020, VF1025, VF1036)

Signal	VF1012	VF1020	VF1025	VF1036	Signal	VF1012	VF1020	VF1025	VF1036	Signal	VF1012	VF1020	VF1025	VF1036
IOB151	K3	W7			IOB201		H2		U7	IOB251				L1
IOB152	K4	V7			IOB202		H3			IOB252				K2
IOB153	K1	U7			IOB203		H4			IOB253				K3
IOB154	J4	Y6	W11	U15	IOB204		G1			IOB254				K4
IOB155	H1	W6	Y11	V15	IOB205		G2	M4	Y6	IOB255				K1
IOB156	H2	V6	W10	W15	IOB206		G3	M3	W6	IOB256				J1
IOB157	H3	U6	V10		IOB207		G4	M2	V6	IOB257				J2
IOB158	H4	Y5	U10		IOB208		F1	M1		IOB258				J3
IOB159	G1	W5	Y10		IOB209		F2	L3		IOB259				J4
IOB160	G2	V5	Y9	Y15	IOB210		F3	L4		IOB260				H1
IOB161	G3	U5	W9	U14	IOB211		F4		U6	IOB261				H2
IOB162	G4	Y4	V9	V14	IOB212		E1		Y5	IOB262				
IOB163	F4	U2	U9		IOB213		E2		W5	IOB263				
IOB164	E1	U1	Y8		IOB214		E3	L2	V5	IOB264				
IOB165	E2	T4	W8		IOB215		E4	L1	U5	IOB265				H3
IOB166	E3	T3	V8	W14	IOB216		D1	K2	Y4	IOB266				H4
IOB167	E4	T2	U8	Y14	IOB217			K3	U2	IOB267				G1
IOB168	D1	T1	Y7	U13	IOB218			K4	U1	IOB268				
IOB169		R4	W7	V13	IOB219			K1	T4	IOB269				
IOB170		R3	V7	W13	IOB220			J1	T3	IOB270				
IOB171		R2	U7	Y13	IOB221			J2	T2	IOB271				G2
IOB172		R1	Y6	U12	IOB222			J3	T1	IOB272				G3
IOB173		P4	W6	V12	IOB223			J4		IOB273				G4
IOB174		P3	V6	W12	IOB224			H1		IOB274				
IOB175		P2	U6	Y12	IOB225			H2		IOB275				
IOB176		P1	Y5	V11	IOB226			H3	R4	IOB276				
IOB177		N4	W5	U11	IOB227			H4	R3	IOB277				F1
IOB178			V5	W11	IOB228			G1	R2	IOB278				F2
IOB179			U5	Y11	IOB229			G2		IOB279				F3
IOB180			Y4	W10	IOB230			G3		IOB280				
IOB181		N3	U2	V10	IOB231			G4		IOB281				
IOB182		N2	U1	U10	IOB232			F1	R1	IOB282				
IOB183		N1	T4	Y10	IOB233			F2	P4	IOB283				F4
IOB184		M4	T3	Y9	IOB234			F3	P3	IOB284				E1
IOB185		M3	T2	W9	IOB235			F4		IOB285				E2
IOB186		M2	T1	V9	IOB236			E1		IOB286				E3
IOB187		M1	R4	U9	IOB237			E2		IOB287				E4
IOB188		L3	R3	Y8	IOB238			E3	P2	IOB288				D1
IOB189		L4	R2	W8	IOB239			E4	P1					
IOB190		L2	R1		IOB240			D1	N4					
IOB191		L1	P4		IOB241				N3					
IOB192		K2	P3		IOB242				N2					
IOB193		K3	P2	V8	IOB243				N1					
IOB194		K4	P1	U8	IOB244				M4					
IOB195		K1	N4	Y7	IOB245				M3					
IOB196		J1	N3		IOB246				M2					
IOB197		J2	N2		IOB247				M1					
IOB198		J3	N1		IOB248				L3					
IOB199		J4		W7	IOB249				L4					
IOB200		H1		V7	IOB250				L2					

208 PQFP PACKAGE



16-038-PQR-1_AH
PRH208
EC95
8-13-97 lv

208 PQFP Common Signals (VF1012, VF1020, VF1025, VF1036)

Group	Signal	Pin
Clock Inputs	SET/RESET	207
	CLK0	2
	CLK1	54
	CLK2	105
	CLK3	157
JTAG Interface	TDI	53
	TMS	208
	TDO	156
	TCLK	1
Configuration, Dedicated	/PROGRAM	52
	DONE	104
	CCLK	155
Configuration, Multiplexed	HDC	55
	/LDC	56
	/INIT	57
	M0	58
	M1	59
	M2	99
	/CSO	100
	CS1	101
	/RS	102
	/WS	103
	RDY/(/BUSY)	158
	DOUT	159
	D7	160
	D6	161
	D5	162
	D4	202
	D3	203
	D2	204
	D1	205
	D0	206
Power Pins	VCC (16)	8, 112, 20, 125, 32, 137, 45, 149, 60, 164, 72, 177, 84, 189, 97, 201
	GND (16)	9, 21, 33, 46, 61, 73, 85, 98, 111, 124, 136, 148, 163, 176, 188, 200

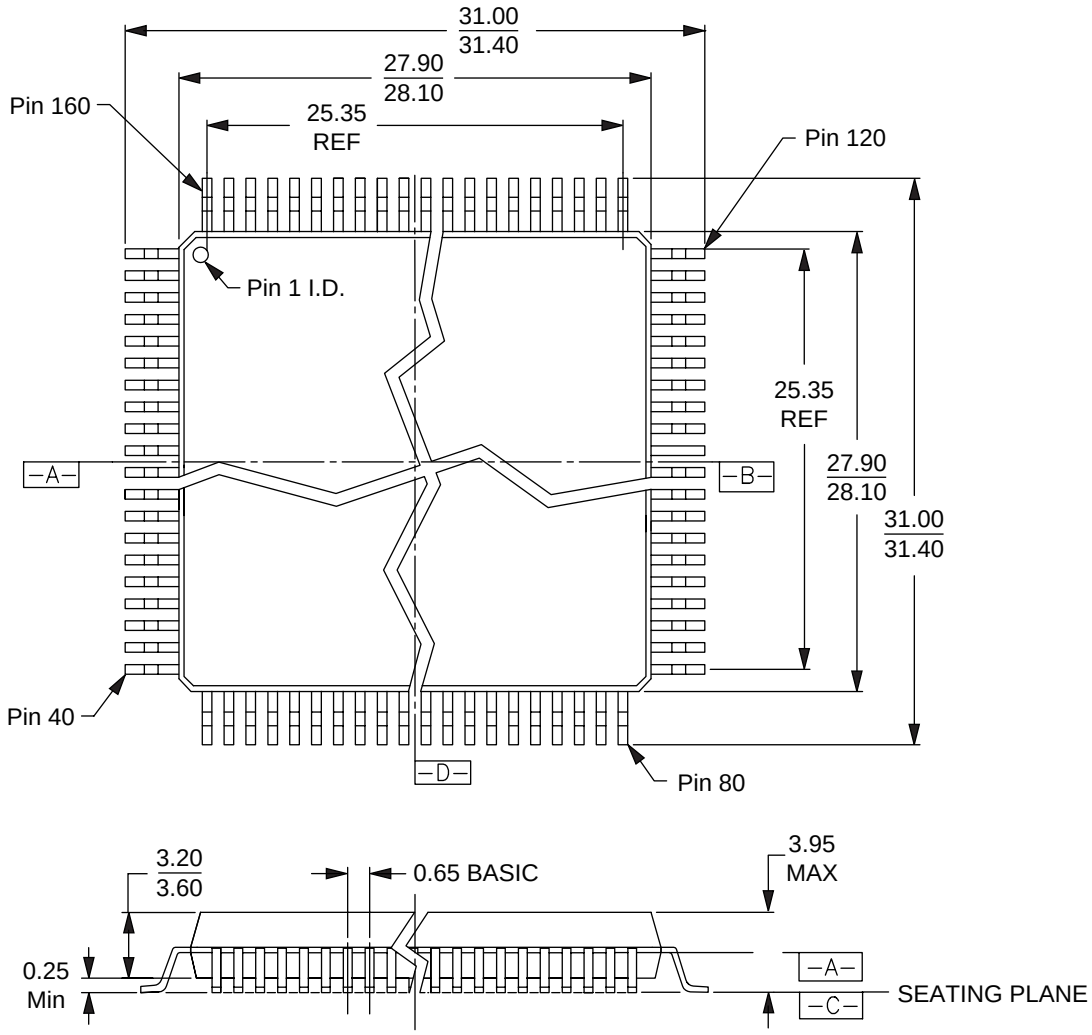
256 PQFP INPUT/OUTPUT BLOCKS (VF1012, VF1020, VF1025, VF1036)

Signal	VF1012	VF1020	VF1025	VF1036	Signal	VF1012	VF1020	VF1025	VF1036	Signal	VF1012	VF1020	VF1025	VF1036
IOB1	3	3	3	3	IOB51	65	48	40	37	IOB101	126	94		75
IOB2	4	4	4	4	IOB52	66	49	41		IOB102	127	95		76
IOB3	5	5	5	5	IOB53	67	50	42		IOB103	128	96	82	
IOB4	6	6	6	6	IOB54	68	51	43		IOB104	129	99	83	
IOB5	7	7	7	7	IOB55	69	55	44	38	IOB105	130	100	86	
IOB6	10	10	10	10	IOB56	70	56	47	39	IOB106	131	101	87	77
IOB7	11	11	11		IOB57	71	57	48	40	IOB107	132	102	88	78
IOB8	12	12	12		IOB58		58	49		IOB108	133	103	89	
IOB9	13	13	13		IOB59	74	59	50		IOB109	134	106	90	
IOB10	14	14	14	11	IOB60	75	62	51		IOB110	135	107	91	
IOB11	15	15	15	12	IOB61	76	63	55	41	IOB111		108	92	
IOB12	16	16	16	13	IOB62	77	64	56	42	IOB112	138	109	93	79
IOB13	17	17	17		IOB63	78	65	57	43	IOB113	139	110	94	80
IOB14	18	18	18		IOB64	79	66	58		IOB114	140	113	95	81
1OB15	19	19	19		IOB65	80	67	59		IOB115	141	114	96	
IOB16				14	IOB66	81	68	62		IOB116	142	115	99	
IOB17	22	22	22	15	IOB67	82	69	63	44	IOB117	143	116	100	
IOB18	23	23	23	16	IOB68	83	70	64	47	IOB118	144	117	101	82
IOB19	24				IOB69	86	71	65	48	IOB119	145	118	102	83
IOB20	25				IOB70	87		66	49	IOB120	146	119	103	86
IOB21	26				IOB71	88	74	67	50	IOB121	147	120	106	87
IOB22	27			17	IOB72	89	75	68	51	IOB122	150	121	107	88
IOB23	28			18	IOB73	90		69	55	IOB123	151	122	108	89
IOB24	29			19	IOB74	91		70	56	IOB124	152		109	
IOB25	30	24	24		IOB75	92		71	57	IOB125	153		110	
IOB26	31	25	25		IOB76	93			58	IOB126	154		113	
IOB27	34	26	26		IOB77	94		74	59	IOB127	158	123	114	90
IOB28	35	27		22	IOB78	95		75	62	IOB128	159	126	115	91
IOB29	36	28		23	IOB79	96	76			IOB129	160	127	116	92
IOB30	37	29		24	IOB80	99	77			IOB130	161		117	
IOB31	38				IOB81	100	78			IOB131	162		118	
IOB32	39				IOB82	101	79		63	IOB132	165		119	
IOB33	40				IOB83	102	80		64	IOB133	166	128	120	93
IOB34	41	30	27	25	IOB84	103	81		65	IOB134	167	129	121	94
IOB35	42	31	28	26	IOB85	106		76		IOB135	168	130	122	95
IOB36	43	34	29		IOB86	107		77		IOB136	169	131	123	
IOB37	44				IOB87	108		78		IOB137	170	132	126	
IOB38	47				IOB88	109	82		66	IOB138	171	133	127	
IOB39	48				IOB89	110	83		67	IOB139	172			96
IOB40	49	35		27	IOB90	113	86		68	IOB140	173			99
IOB41	50	36		28	IOB91	114				IOB141	174			100
IOB42	51	37		29	IOB92	115				IOB142	175			101
IOB43	55	38	30		IOB93	116				IOB143	178			102
IOB44	56	39	31		IOB94	117	87	79	69	IOB144	179			103
IOB45	57	40	34		IOB95	118	88	80	70	IOB145	180	134	128	106
IOB46	58	41	35	30	IOB96	119	89	81	71	IOB146	181	135	129	107
IOB47	59	42	36	31	IOB97	120	90			IOB147	182		130	108
IOB48	62	43	37	34	IOB98	121	91			IOB148	183	138		109
IOB49	63	44	38	35	IOB99	122	92			IOB149	184	139		110
IOB50	64	47	39	36	IOB100	123	93		74	IOB150	185	140		113

256 PQFP INPUT/OUTPUT BLOCKS (VF1012, VF1020, VF1025, VF1036)

Signal	VF1012	VF1020	VF1025	VF1036	Signal	VF1012	VF1020	VF1025	VF1036	Signal	VF1012	VF1020	VF1025	VF1036
IOB151	186	141			IOB201				143	IOB251				
IOB152	187	142			IOB202		190			IOB252				
IOB153		143			IOB203		191			IOB253				
IOB154	190	144	131	114	IOB204		192			IOB254				183
IOB155	191	145	132	115	IOB205		193	180	144	IOB255				184
IOB156	192	146	133	116	IOB206		194	181	145	IOB256				
IOB157	193	147			IOB207		195	182	146	IOB257				
IOB158	194	150			IOB208		196			IOB258				
IOB159	195	151			IOB209		197			IOB259				185
IOB160	196	152		117	IOB210		198			IOB260				186
IOB161	197	153		118	IOB211		199		147	IOB261				187
IOB162	198	154		119	IOB212		202		150	IOB262				
IOB163	199	158	134		IOB213		203		151	IOB263				
IOB164	202	159	135		IOB214		204	183	152	IOB264				
IOB165	203	160			IOB215		205	184	153	IOB265				190
IOB166	204	161	138	120	IOB216		206	185	154	IOB266				191
IOB167	205	162	139	121	IOB217				158	IOB267				192
IOB168	206	165	140	122	IOB218				159	IOB268				
IOB169		166	141	123	IOB219				160	IOB269				
IOB170		167	142	126	IOB220				161	IOB270				
IOB171		168	143	127	IOB221				162	IOB271				193
IOB172		169	144		IOB222				165	IOB272				194
IOB173		170	145		IOB223			186		IOB273				195
IOB174		171	146		IOB224			187		IOB274				
IOB175		172	147	128	IOB225					IOB275				
IOB176		173	150	129	IOB226			190	166	IOB276				
IOB177		174	151	130	IOB227			191	167	IOB277				196
IOB178			152		IOB228			192	168	IOB278				197
IOB179			153		IOB229			193		IOB279				198
IOB180			154		IOB230			194		IOB280				
IOB181		175	158		IOB231			195		IOB281				
IOB182		178	159	131	IOB232			196	169	IOB282				
IOB183		179	160	132	IOB233			197	170	IOB283				199
IOB184			161		IOB234			198	171	IOB284				202
IOB185			162		IOB235			199		IOB285				203
IOB186			165		IOB236			202		IOB286				204
IOB187		180	166	133	IOB237			203		IOB287				205
IOB188		181	167	134	IOB238			204	172	IOB288				206
IOB189		182	168	135	IOB239			205	173					
IOB190		183	169		IOB240			206	174					
IOB191		184	170		IOB241				175					
IOB192		185	171		IOB242				178					
IOB193			172	138	IOB243				179					
IOB194			173	139	IOB244									
IOB195			174	140	IOB245									
IOB196			175		IOB246									
IOB197			178		IOB247				180					
IOB198			179		IOB248				181					
IOB199		186		141	IOB249				182					
IOB200		187		142	IOB250									

160 PQFP PACKAGE



16-038-PQR-1
PQR160
12-22-95 lv

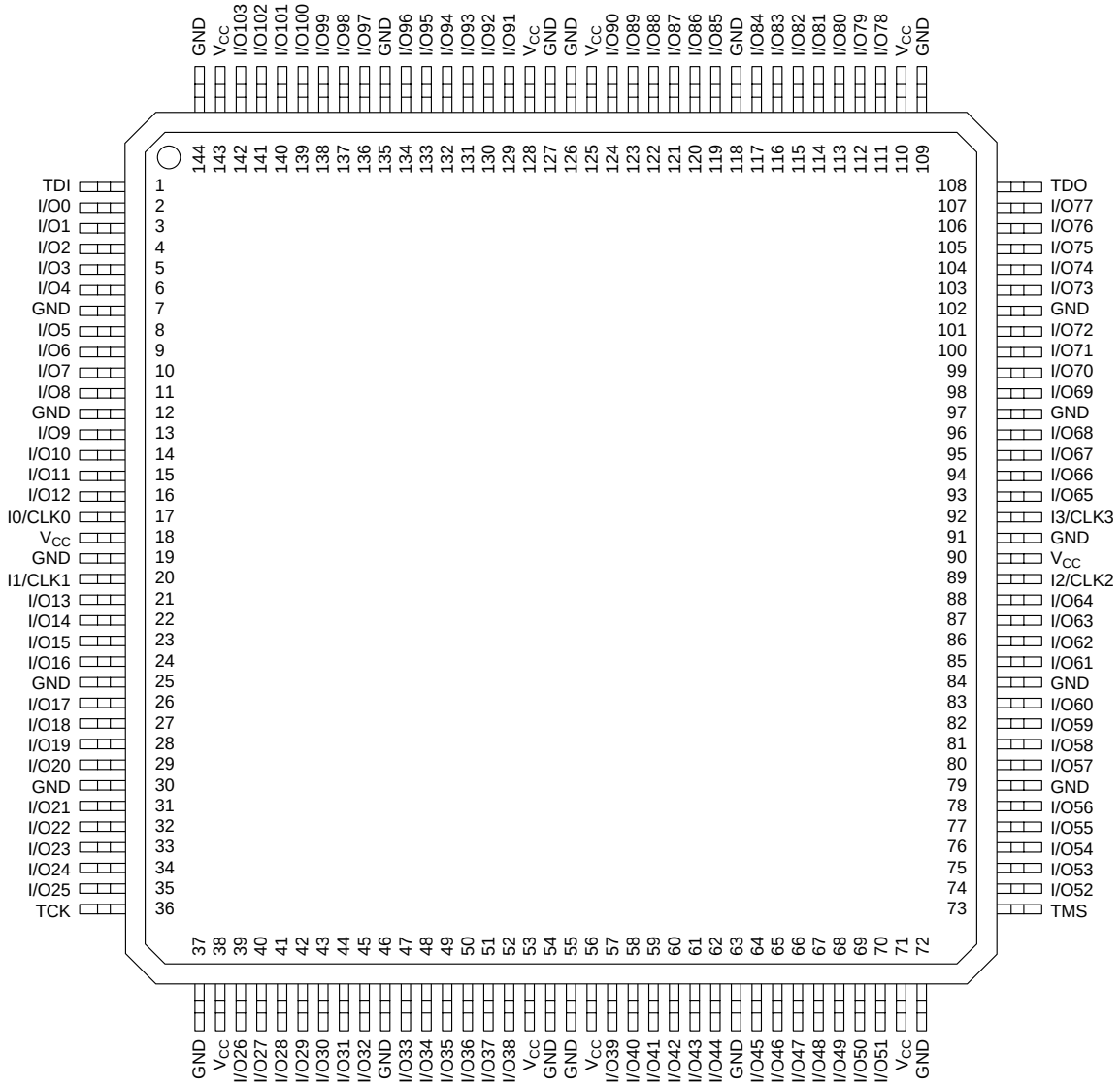
160 PQFP Common Signals (VF1012, VF1020)

Group	Signal	Pin
Clock Inputs	SET/RESET	159
	CLK0	2
	CLK1	42
	CLK2	81
	CLK3	121
JTAG Interface	TDI	41
	TMS	160
	TDO	120
	TCLK	1
Configuration, Dedicated	/PROGRAM	40
	DONE	80
	CCLK	119
Configuration, Multiplexed	HDC	43
	/LDC	44
	/INIT	45
	M0	46
	M1	47
	M2	75
	/CSO	76
	CS1	77
	/RS	78
	/WS	79
	RDY/(/BUSY)	122
	DOUT	123
	D7	124
	D6	125
	D5	126
	D4	154
	D3	155
	D2	156
	D1	157
	D0	158
Power Pins	VCC (12)	8, 20, 33, 48, 60, 73, 88, 101, 113, 128, 141, 153
	GND (12)	9, 21, 34, 49, 61, 74, 87, 100, 112, 127, 140, 152

160 PQFP INPUT/OUTPUT BLOCKS (VF1012, VF1020)

Signal	VF1012	VF1020	Signal	VF1012	VF1020	Signal	VF1012	VF1020	Signal	VF1012	VF1020	Signal	VF1012	VF1020
IOB1	3	3	IOB51	53	36	IOB101			IOB151	138	105	IOB201		
IOB2	4	4	IOB52	54	37	IOB102			IOB152	139	106	IOB202		142
IOB3	5	5	IOB53	55	38	IOB103	95	72	IOB153		107	IOB203		143
IOB4	6	6	IOB54	56	39	IOB104	96	75	IOB154	142	108	IOB204		144
IOB5	7	7	IOB55	57	43	IOB105	97	76	IOB155	143	109	IOB205		145
IOB6	10	10	IOB56	58	44	IOB106		77	IOB156	144	110	IOB206		146
IOB7	11	11	IOB57	59	45	IOB107		78	IOB157	145	111	IOB207		147
IOB8	12	12	IOB58		46	IOB108		79	IOB158	146	114	IOB208		148
IOB9	13	13	IOB59	62	47	IOB109	98	82	IOB159	147	115	IOB209		149
IOB10	14	14	IOB60	63	50	IOB110	99	83	IOB160	148	116	IOB210		150
IOB11	15	15	IOB61		51	IOB111		84	IOB161	149	117	IOB211		151
IOB12	16	16	IOB62		52	IOB112	102	85	IOB162	150	118	IOB212		154
IOB13	17	17	IOB63		53	IOB113	103	86	IOB163	151	122	IOB213		155
IOB14	18	18	IOB64	64	54	IOB114	104	89	IOB164	154	123	IOB214		156
IOB15	19	19	IOB65	65	55	IOB115	105		IOB165	155	124	IOB215		157
IOB16			IOB66	66	56	IOB116	106		IOB166	156	125	IOB216		158
IOB17	22	22	IOB67		57	IOB117	107		IOB167	157	126			
IOB18	23	23	IOB68		58	IOB118	108		IOB168	158	129			
IOB19			IOB69		59	IOB119	109	90	IOB169					
IOB20			IOB70	67		IOB120	110	91	IOB170					
IOB21			IOB71	68	62	IOB121	111		IOB171					
IOB22	24		IOB72	69	63	IOB122	114		IOB172					
IOB23	25		IOB73			IOB123	115		IOB173		130			
IOB24	26		IOB74			IOB124	116		IOB174		131			
IOB25		24	IOB75			IOB125	117		IOB175					
IOB26		25	IOB76	70		IOB126	118		IOB176					
IOB27		26	IOB77	71		IOB127	122	92	IOB177					
IOB28	27		IOB78			IOB128	123	93	IOB178					
IOB29	28		IOB79	72	64	IOB129	124	94	IOB179					
IOB30	29		IOB80	75	65	IOB130	125		IOB180					
IOB31			IOB81	76	66	IOB131	126		IOB181		132			
IOB32			IOB82	77		IOB132	129		IOB182		133			
IOB33			IOB83	78		IOB133			IOB183		134			
IOB34	30	27	IOB84	79		IOB134	130		IOB184					
IOB35	31	28	IOB85	82		IOB135	131		IOB185					
IOB36		29	IOB86	83		IOB136		95	IOB186					
IOB37	32		IOB87	84		IOB137		96	IOB187					
IOB38	35		IOB88	85	67	IOB138		97	IOB188					
IOB39	36		IOB89	86	68	IOB139	132		IOB189					
IOB40	37		IOB90	89	69	IOB140	133		IOB190		135			
IOB41	38		IOB91			IOB141	134		IOB191		136			
IOB42	39		IOB92	90		IOB142			IOB192		137			
IOB43	43	30	IOB93	91		IOB143			IOB193					
IOB44	44	31	IOB94			IOB144			IOB194					
IOB45	45		IOB95			IOB145	135	98	IOB195					
IOB46	46		IOB96			IOB146	136	99	IOB196					
IOB47	47		IOB97	92	70	IOB147	137		IOB197					
IOB48	50		IOB98	93	71	IOB148		102	IOB198					
IOB49	51	32	IOB99	94		IOB149		103	IOB199		138			
IOB50	52	35	IOB100			IOB150		104	IOB200		139			

144 TQFP PACKAGE



144 TQFP Signals (VF1012)

Group	Signal	Pin
Clock Inputs	SET/RESET	143
	CLK0	2
	CLK1	38
	CLK2	73
	CLK3	109
JTAG Interface	TDI	37
	TMS	144
	TDO	108
	TCLK	1
Configuration, Dedicated	PROGRAM	36
	DONE	72
	CCLK	107
Configuration, Multiplexed	HDC	39
	/LDC	40
	/INIT	41
	M0	42
	M1	43
	M2	67
	/CSO	68
	CS1	69
	/RS	70
	/WS	71
	RDY/(/BUSY)	110
	DOUT	111
	D7	112
	D6	113
	D5	114
	D4	138
	D3	139
	D2	140
	D1	141
	D0	142
Power Pins	VCC (12)	8, 17, 29, 44, 53, 65, 80, 92, 101, 116, 128, 137
	GND (12)	9, 18, 30, 45, 54, 66, 79, 91, 100, 115, 127, 136

144 TQFP INPUT/OUTPUT BLOCKS (VF1012)

Signal	VF1012	Signal	VF1012	Signal	VF1012	Signal	VF1012
IOB1	3	IOB43	39	IOB85	74	IOB127	110
IOB2	4	IOB44	40	IOB86	75	IOB128	111
IOB3	5	IOB45	41	IOB87	76	IOB129	112
IOB4	6	IOB46	42	IOB88	77	IOB130	113
IOB5	7	IOB47	43	IOB89	78	IOB131	114
IOB6	10	IOB48	46	IOB90	81	IOB132	117
IOB7		IOB49		IOB91		IOB133	
IOB8		IOB50		IOB92		IOB134	
IOB9		IOB51		IOB93	82	IOB135	118
IOB10	11	IOB52	47	IOB94		IOB136	
IOB11	12	IOB53	48	IOB95		IOB137	
IOB12	13	IOB54	49	IOB96		IOB138	
IOB13	14	IOB55	50	IOB97	83	IOB139	119
IOB14	15	IOB56	51	IOB98	84	IOB140	120
1OB15	16	IOB57	52	IOB99	85	IOB141	121
IOB16		IOB58		IOB100		IOB142	
IOB17	19	IOB59	55	IOB101		IOB143	
IOB18	20	IOB60	56	IOB102		IOB144	
IOB19		IOB61		IOB103	86	IOB145	122
IOB20		IOB62		IOB104	87	IOB146	123
IOB21		IOB63		IOB105	88	IOB147	124
IOB22	21	IOB64	57	IOB106		IOB148	
IOB23	22	IOB65	58	IOB107		IOB149	
IOB24	23	IOB66	59	IOB108		IOB150	
IOB25		IOB67		IOB109	89	IOB151	125
IOB26		IOB68		IOB110	90	IOB152	126
IOB27		IOB69		IOB111		IOB153	
IOB28	24	IOB70	60	IOB112	93	IOB154	129
IOB29	25	IOB71	61	IOB113	94	IOB155	130
IOB30	26	IOB72	62	IOB114	95	IOB156	131
IOB31		IOB73		IOB115	96	IOB157	132
IOB32		IOB74		IOB116	97	IOB158	133
IOB33		IOB75		IOB117	98	IOB159	134
IOB34	27	IOB76	63	IOB118		IOB160	
IOB35		IOB77		IOB119		IOB161	
IOB36		IOB78		IOB120		IOB162	
IOB37	28	IOB79	64	IOB121	99	IOB163	135
IOB38	31	IOB80	67	IOB122	102	IOB164	138
IOB39	32	IOB81	68	IOB123	103	IOB165	139
IOB40	33	IOB82	69	IOB124	104	IOB166	140
IOB41	34	IOB83	70	IOB125	105	IOB167	141
IOB42	35	IOB84	71	IOB126	106	IOB168	142