MACH 5 Timing and High Speed Design

INTRODUCTION

When implementing a design into a MACH® 5 device, it is often critical to understand how the placement of the design will affect the timing. The MACH 5 device has numerous paths a signal can take, each of which affects the timing in one fashion or another. To more accurately describe the different paths, the MACH 5 timing model has been changed. This technical note explains the new MACH 5 timing model.

MACH 5 ARCHITECTURE BASICS

The architecture used in the MACH 5 family of devices is the next step in the evolution of complex programmable logic devices (CPLDs). A CPLD can be viewed as a group of PLDs connected together by a programmable switch matrix. The MACH 5 devices take the concept of hierarchy one step further by connecting multiple CPLDs together with a programmable switch matrix. This concept is illustrated in Figure 1.

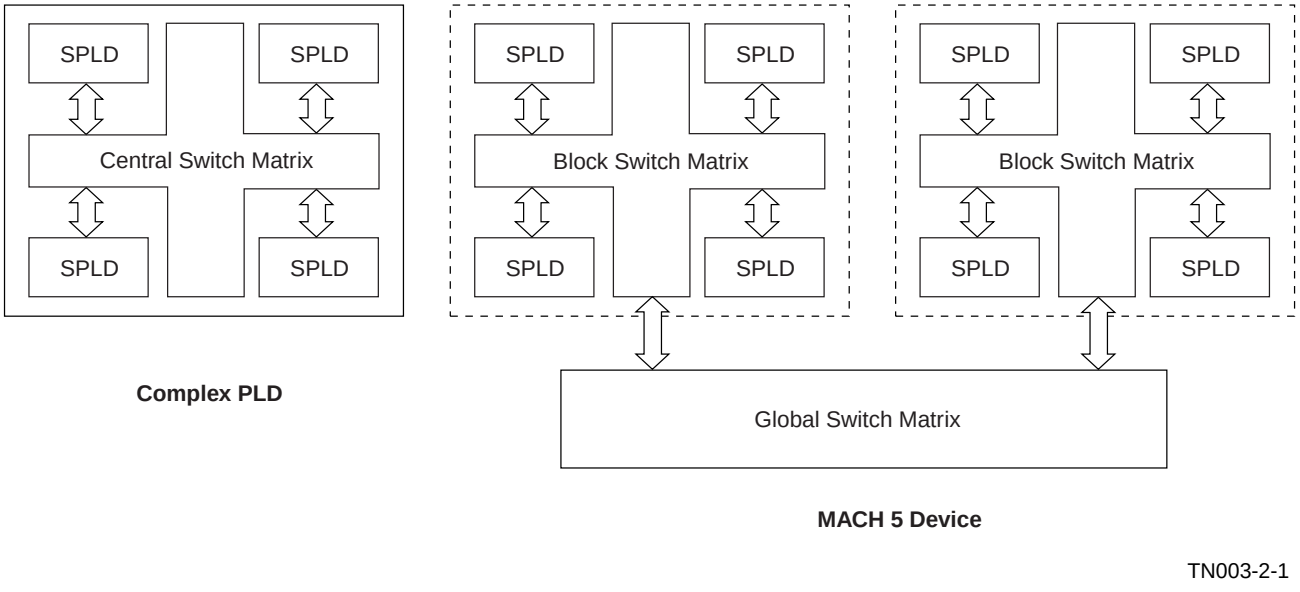

Figure 1. CPLD and MACH 5 Architecture Diagrams

There are several benefits inherent in the MACH 5 architecture including the ability to attain higher densities while maintaining fast speeds. These fast speeds, however, are only available on those paths that use local feedback from a block back into itself. If a signal has to go through a Block Switch Matrix or the Global Switch Matrix, there is an additional adder to speed. In the MACH 1, MACH 2, and MACH 4 devices, where all signals go through the Central Switch Matrix, there are no such adders, so the speed for any given path will be SpeedLocked™.

Application Notes

Feedback Types

Any given macrocell output signal will traditionally have two different feedback paths into the switch matrix. These two paths are referred to as **internal feedback** and **external feedback**. A signal uses internal feedback when it is fed back into the switch matrix or block without having to go through the output buffer. When a signal is fed back into the switch matrix after having gone through the output buffer, it is using external feedback. Both feedback types are shown in Figure 2.

In the previous timing model used for the MACH 5 family of devices, the only feedback path reported in a timing report was the external feedback path. Signals using internal feedback were reported as if they had used an external feedback path. As a result, the reported delays for those signals would be greater than what would actually be seen in the real device. The MACH 5 timing model now makes a distinction between those signals using internal feedback and those using external feedback.

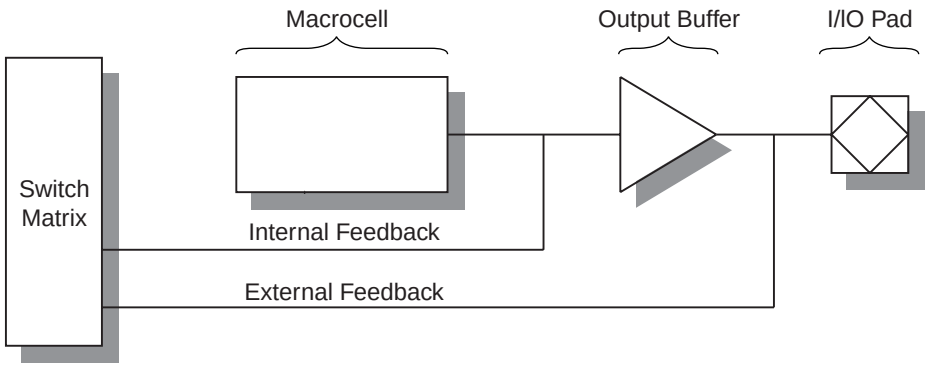

Figure 2. Feedback Types

Input Register Timing

Another area in which the MACH 5 timing model has been improved is in the reporting of input register timing. Because there was previously no mechanism for reporting the internal timing of a MACH 5 device, the timing used for input registers could become complicated. The specifications found in the original MACH 5 data sheets relied on timing that went through both an input register and an output register. As an example, the parameter t_{ICOA} represented the clock-to-output time for a signal to go through an input register to a combinatorial macrocell, plus the time it took to go through the combinatorial macrocell and to an I/O pad. This method of determining timing was very difficult for the software implementation of the timing model and for designers attempting to determine their timing requirements.

The MACH 5 timing model has greatly simplified the input register timing by reporting all as internal feedback. The same parameter, t_{ICOA}, will no longer exist but rather will be calculated as the clock-to-internal feedback of the input register plus a t_{PDi} and a t_{BUF}. The parameter t_{PDi} is the time it takes a signal to go through a combinatorial macrocell to internal feedback, and t_{BUF} is the time it takes a signal to go through the output buffer. Because of this timing methodology, several input register specifications have been removed from the MACH 5 data sheet.

MACH 5 TIMING MODEL

The primary focus of the MACH 5 timing model is to accurately represent the timing in a MACH 5 device while, at the same time, be easy to understand. To accomplish the accuracy, the distinction between internal and external feedback is made. To make the timing easier to understand, the input register specifications are simplified. A diagram representing the MACH 5 timing model is shown in Figure 3.

To make the distinction between internal and external feedback, several timing parameters have been changed, and the parameter t_{BUF} has been added. All of the changed parameters deal with a signal going to the I/O pad. As an example, the parameter t_{PD} was originally defined as an input, I/O or feedback going to a combinatorial output. This parameter is now the sum of two parameters: t_{PDi} and t_{BUF}. The parameter t_{PDi} is defined as the time it takes an input, I/O or feedback to go to a combinatorial feedback, while t_{BUF} is the time it takes to go from feedback, through the output buffer and to the I/O pad. The naming convention used for the changed parameters is to add an "i" after the original name if the signal is going to the internal feedback rather than to the I/O pad. A list of the changed parameters along with their definitions is given in Table 1.

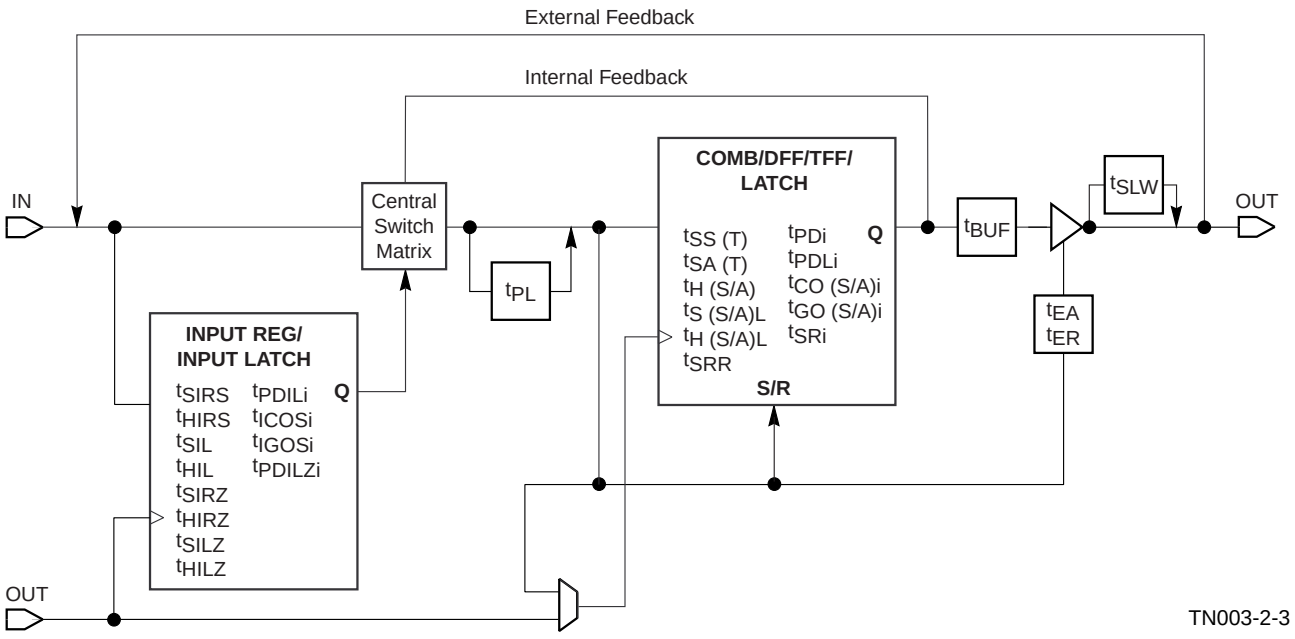

Figure 3. MACH 5 Timing Model

Table 1. MACH 5 Parameter Description

External Parameter	Internal Parameter	Description
t_{PD}	t_{PDi}	Input, I/O, or feedback to feedback
t_{COS}	t_{COSi}	Global clock to feedback
t_{COA}	t_{COAi}	Product term clock to feedback
t_{RP}	t_{SRi}	Asynchronous Reset or Preset to registered or latched feedback
t_{GO}	t_{GOAi}	Latch gate to feedback
t_{PDL}	t_{PDLi}	Input, I/O or feedback to feedback through transparent latch
	t_{BUF}	Feedback to Output

The input register in the MACH 5 device is a macrocell register that takes its input from an I/O pad rather than from the product term array. As a result, the output timing for an input register is the same as that for a macrocell register. Several input register parameters have been eliminated from the original MACH 5 timing model and data sheet because they can now be derived in the new timing model. Table 2 shows the derivations of the eliminated data specifications.

To maintain consistency with the timing models of other MACH families, some of the parameters have been renamed. In particular the set/reset parameters t_{RP}, t_{PRW}, and t_{PRR} have been renamed to t_{SR}, t_{SRW}, and t_{SRR}. Additionally, the latch parameters have been renamed to denote their asynchronous nature. The parameters t_{SL}, t_{HL}, and t_{GO} have been renamed to t_{SAL}, t_{HAL}, and t_{GOA}, respectively. Information about all of the timing parameters can be found in the *MACH 5(A) Family Data Sheet* and is shown below in Table 3.

Table 2. Derivations of Eliminated Parameters

Eliminated Parameter	Derivation
t_{PDIL}	$t_{PDILi} + t_{PDi} + t_{BUF}$
t_{ICOG}	$t_{COSi} + t_{PDi} + t_{BUF}$
t_{ICOA}	$t_{COAi} + t_{PDi} + t_{BUF}$
t_{PDLL}	$t_{PDILi} + t_{PDLi} + t_{BUF}$
t_{RCSS}	$t_{COSi} + t_{SS}$
t_{RCSA}	$t_{COSi} + t_{SA}$
t_{RCAS}	$t_{COAi} + t_{SS}$
t_{RCAA}	$t_{COAi} + t_{SA}$
t_{SLL}	$t_{PDLi} + t_{SL}$

Table 3. MACH 5 Internal Timing Parameter Definitions

Combinatorial Delay:	t_{PDi}	Input, I/O, or Feedback to Combinatorial Feedback
Register Delays:	t_{SS}	Setup Time from Input, I/O or Feedback to Global Clock
	t_{SA}	Setup Time from Input, I/O or Feedback to Product Term Clock
	t_{HS}	Register Data Hold Time Using a Global Clock
	t_{HA}	Register Data Hold Time Using a Product Term Clock
	t_{COSi}	Global Clock to Feedback
	t_{COAi}	Asynchronous Clock to Feedback
Latch Delays:	t_{SAL}	Setup Time from Input, I/O or Feedback to Product Term Gate
	t_{HAL}	Latch Data Hold Time
	t_{PDLi}	Input, I/O, or Feedback to Feedback through Transparent Latch
	t_{GOAi}	Latch Gate to Feedback
Input Register Delays:	t_{SIRS}	Input Register Setup Time Using a Global Clock
	t_{SIRA}	Input Register Setup Time Using a Product Term Clock
	t_{HIRS}	Input Register Hold Time Using a Global Clock
	t_{HIRA}	Input Register Hold Time Using a Product Term Clock
Input Latch Delays:	t_{SIL}	Input Latch Setup Time Using a Product Term Clock
	t_{HIL}	Input Latch Hold Time
	t_{PDILi}	I/O to Feedback Through Transparent Input Latch
Output Delays:	t_{BUF}	Feedback to I/O Through Output Buffer
	t_{SLW}	Slow Slew Rate Delay
	t_{EA}	Output Enable Time
	t_{ER}	Output Disable Time
Power Delays:	t_{PL1}	Power Level 1 Delay
	t_{PL2}	Power Level 2 Delay
	t_{PL3}	Power Level 3 Delay
Cluster Delay:	t_{PT}	Product Term Cluster Delay
Interconnect Delays:	t_{BLK}	Block Interconnect Delay
	t_{SEG}	Segment Interconnect Delay
Reset/Preset Delays:	t_{SRi}	Asynchronous Reset or Preset to Internal Register Output
	t_{SRR}	Reset and Set Register Recovery Time
Clock Enable Delays:	t_{CES}	Clock Enable Setup Time
	t_{CEH}	Clock Enable Hold Time

USING THE MACH 5 TIMING MODEL

The use of the MACH 5 timing model will be demonstrated with an example. The example includes multiple t_{PD} paths and demonstrates the use of internal feedback.

Example

Signal "A" enters the MACH 5-256 through Block A, Segment 0. It then goes to Node "B" in Block C, Segment 0 and to Output "C" in Block B, Segment 1. Node B is internally fed back to create Output "D" in Block A, Segment 2. Block B, Segment 1 is in high power and Block C, Segment 0 is in low power. All Outputs are configured to have a fast slew rate.

The timing from Signal "A" to Output "C" is given by:

$$t_{DELAY} = t_{PDi} + t_{SEG} + t_{BUF}$$

The t_{PDi} is the time it takes for the signal to go from the input in Block A, Segment 0 to feedback. Because the output is in a different segment, t_{SEG} is added. Finally, t_{BUF} is added as the time it takes to go from feedback to the output.

The timing from Signal "A" to Output "D" through Node "B" is given by:

$$t_{DELAY} = t_{DELAYAB} + t_{DELAYBD}$$

$$t_{DELAYAB} = t_{PDi} + t_{BLK} + t_{PL3}$$

$$t_{DELAYBD} = t_{PDi} + t_{SEG} + t_{BUF}$$

The delay path from Signal "A" to Output "D" is broken up into two elements. The delay from Signal "A" to Node "B", $t_{DELAYAB}$, includes t_{PDi} for the combinatorial delay to feedback, t_{BLK} because Signal "A" and Node "B" are in different blocks inside the same segment, and t_{PL3} because Block C, Segment 0 is in low power. The original MACH 5 timing model required an additional t_{BUF} be added to the delay path because internal feedback was not defined.

The delay path from Node "B" to Output "D", $t_{DELAYBD}$, includes t_{PDi} to account for the delay from feedback to output, t_{SEG} because Node "B" and Output "D" are in different segments, and t_{BUF} to account for the signal going to the output.

The use of the MACH 5 timing model is straightforward and merely requires the addition of internal parameters to arrive at the external parameters or device timing.

HIGH-SPEED DESIGN WITH MACH 5 DEVICES

While the possibility has always existed to control the implementation of high speed designs into a MACH 5 device, the reporting of the timing never made it easy because no distinction was made between internal and external feedback. The improved MACH 5 timing model makes that critical distinction, making it easier to understand how a design is fit into a device.

During the fitting process, the software may use external feedback on timing critical nodes where internal feedback may be required to meet a particular speed. It is also possible that the software feeds a signal into either the block or global switch matrices, which will affect timing. Constraints can be placed on a design to ensure that the critical paths are fit to meet timing. The more a design is constrained, the more difficult it becomes to fit the design. Some methods that can be used to constrain a design are briefly covered here and are more fully covered in the *MACHXL® User's Manual* and the Application Note entitled, *PI File Reference Guide*. MACHXL

software uses the PI File to control the fitting process and constrain the design. It contains pinout and placement information along with directives that determine the fitting algorithms used.

Controlling Feedback

Within the PI File, there are two directives available that provide for the control of signal feedback. The first of these directives, FORCE_INTERNAL_FEEDBACK, forces a signal to use an internal feedback path rather than giving it a choice of using an external or internal feedback path. By forcing a signal to use internal feedback, the delay caused by the output buffer is saved. The second directive, FORCE_LOCAL_FEEDBACK, forces signals to use a local feedback path back into the PAL® block rather than sending the signal into either the block or global level switch matrix. By doing this, the block or segment delay adders are saved.

Grouping Signals

In the PI file, MACHXL software provides for the grouping of signals into either the same block or the same segment. When signals are grouped into a single block, the chances that those signals will be fed back into that block using the local feedback paths increases significantly, thereby increasing the chances that the fastest timing possible is attained. Grouping signals does not guarantee, however, that local feedback will be used. The use of the FORCE_LOCAL_FEEDBACK directive along with grouping signals may be needed to get the required timing.

Pin and Node Locking

The third way to constrain a design is to force both pin locations and node locations. By doing so, the signals can be grouped within a block or segment, and it becomes easier to enforce local feedback on the critical path signals. Information on pin and node locking can be found in the *MACHXL User's Manual*.

CONCLUSION

The MACH 5 timing model provides for a more accurate, easier to understand timing calculation. It defines both internal and external feedback paths and simplifies the timing used for internal registers. By using and understanding the timing model in the proper way, it becomes easier to control the critical path timing in a high speed design using the properties in the PI file.