MACH 4 Timing and High Speed Design

INTRODUCTION

When implementing a design into a MACH® 4 device, it is often critical to understand how the placement of the design will affect the timing. The MACH 4 device has numerous paths a signal can take, each of which affects the timing in one fashion or another. To more accurately describe the different paths, the MACH 4 timing model has been enhanced[1]. This application note explains the new MACH 4 timing model and high-speed design techniques utilizing this timing model.

MACH 4 ARCHITECTURE BASICS

The fundamental architecture of the MACH 4 device consists of multiple optimized PAL® blocks (PAL33/34V16) interconnected by a programmable central switch matrix. The central switch matrix allows communication between PAL blocks and routes inputs to the PAL blocks. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with multiple paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins. This concept is illustrated in Figure 1. In a MACH 4 device, all signals incur the same delays, regardless of routing. Performance is design-independent and is guaranteed by Vantis' SpeedLocking™ feature.

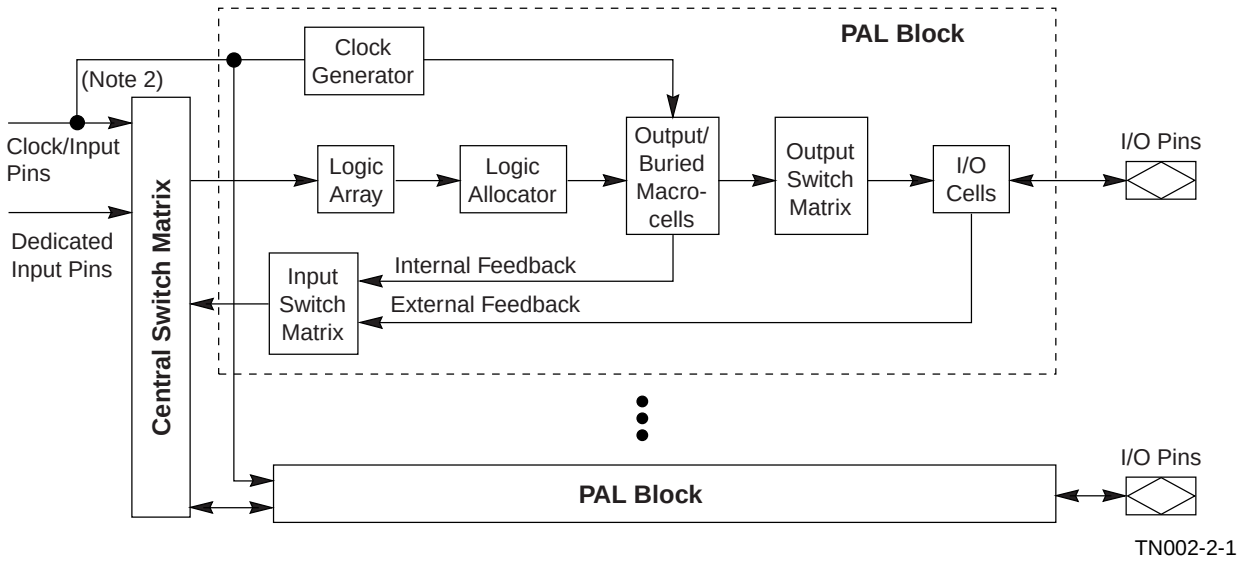

Figure 1. MACH 4 Block Diagram and PAL Block Structure

As indicated in Figure 1, any given macrocell output signal has two different feedback paths into the switch matrix. These two paths are referred to as **internal feedback** and **external feedback**.

1. The new timing model is implemented in MACHXL® software v.6.1 and later.
2. M4-192/96 and M4-256/128 do not have clock/input pins connected to central switch matrix.

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A signal uses internal feedback when it is fed back into the central switch matrix without going through the output switch matrix and the I/O cell. When a signal is fed back into the central switch matrix after having gone through the output switch matrix and the I/O cell, it is using external feedback. For simplicity, the output switch matrix and the I/O cell together are modeled as an output buffer. Both feedback types are shown below in Figure 2.

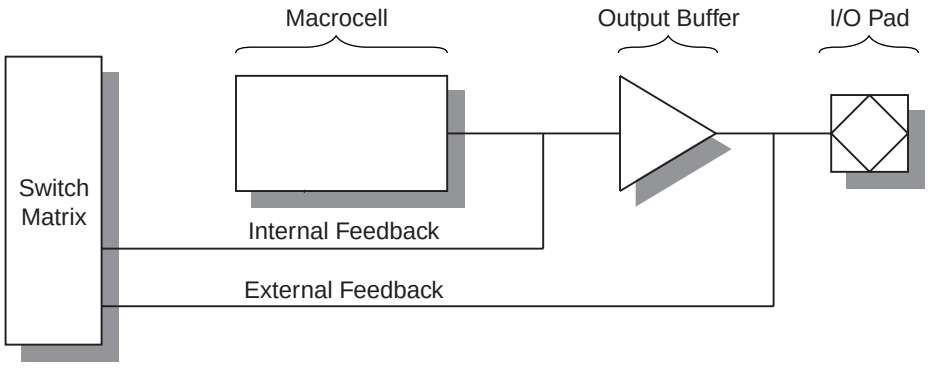

Figure 2. MACH 4 Signal Feedback Types

ENHANCED MACH 4 TIMING MODEL

The primary focus of the MACH 4 timing model is to accurately represent the timing in a MACH 4 device while, at the same time, be easy to understand. To accomplish the accuracy, the distinction between internal and external feedback is made. To make the timing model easier to understand and use, the timing is modularized so that each logic element in the signal path will have its own parameters. In particular, the new parameters associated with the input register/latch are a result of this. A diagram representing the MACH 4 timing model is shown in Figure 3.

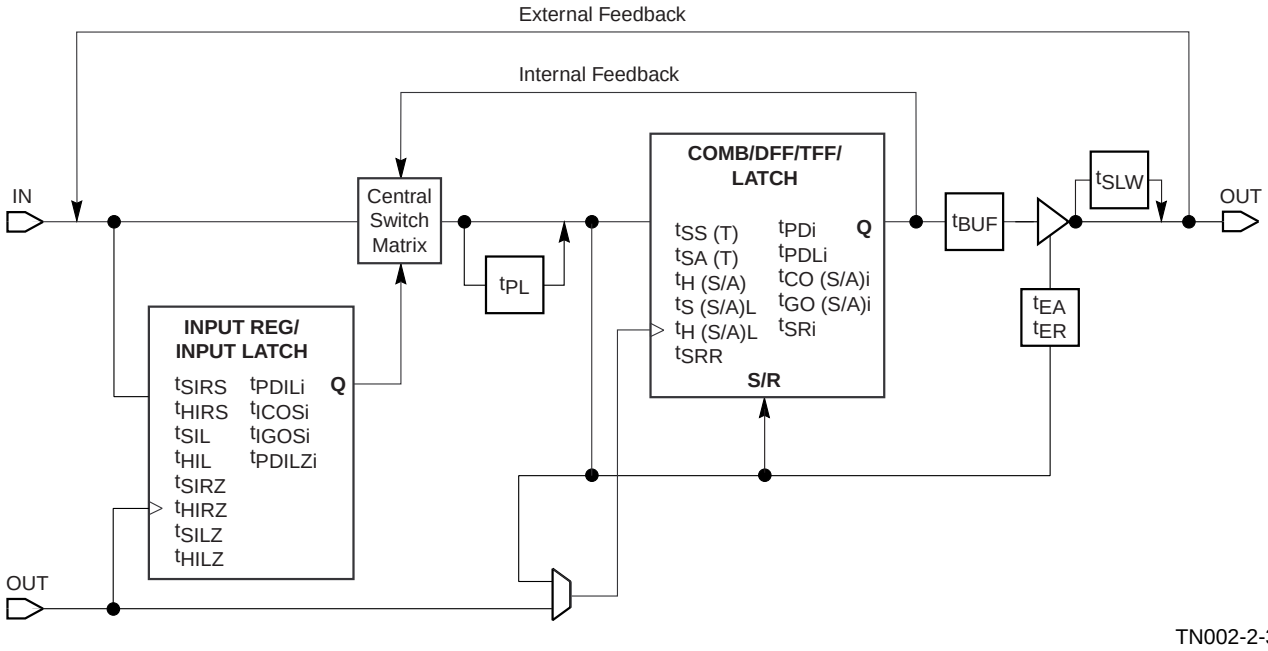

Figure 3. Enhanced MACH 4 Timing Model

Table 1 lists the MACH 4 timing parameters and their descriptions. To understand the new timing model and parameters, an understanding of the naming convention is necessary. An "i" has been added to all parameters that have delays that are "internal" to the device. Several parameters in both the macrocell register and the input register are affected by the change from external parameters to internal parameters. Delays for parameters that have an "i" appended to them are measured to an internal node rather than to an I/O. Table 2 describes the parameters using this convention.

Table 1. MACH 4 Family Timing Parameters

Combinatorial Delay:	t_{PDi}	Internal combinatorial propagation delay
Register Delays:	t_{SS}	Synchronous clock setup time, D-type register
	t_{SST}	Synchronous clock setup time, T-type register
	t_{SA}	Asynchronous clock setup time, D-type register
	t_{SAT}	Asynchronous clock setup time, T-type register
	t_{HS}	Synchronous clock hold time
	t_{HA}	Asynchronous clock hold time
	t_{COSi}	Synchronous clock to internal output
	t_{COAi}	Asynchronous clock to internal output
Latch Delays:	t_{SSL}	Synchronous Latch setup time
	t_{SAL}	Asynchronous Latch setup time
	t_{HSL}	Synchronous Latch hold time
	t_{HAL}	Asynchronous Latch hold time
	t_{PDLi}	Transparent latch to internal output
	t_{GOSi}	Synchronous Gate to internal output
	t_{GOAi}	Asynchronous Gate to internal output
Input Register Delays:	t_{SIRS}	Input register setup time
	t_{HIRS}	Input register hold time
	t_{ICOSi}	Input register clock to internal feedback
Input Latch Delays:	t_{SIL}	Input latch setup time
	t_{HIL}	Input latch hold time
	t_{IGOSi}	Input latch gate to internal feedback
	t_{PDILi}	Transparent input latch to internal feedback
Input Register Delays with ZHT Option:	t_{SIRZ}	Input register setup time - ZHT
	t_{HIRZ}	Input register hold time - ZHT
Input Latch Delays with ZHT Option:	t_{SILZ}	Input latch setup time - ZHT
	t_{HILZ}	Input latch hold time -ZHT
	t_{PDILZi}	Transparent input latch to internal feedback - ZHT

Table 1. MACH 4 Family Timing Parameters (Continued)

Output Delays:	t_{BUF}	Output buffer delay
	t_{SLW}	Slow slew rate delay adder
	t_{EA}	Output enable time
	t_{ER}	Output disable time
Power Delay:	t_{PL}	Power-down mode delay adder
Reset and Preset Delays:	t_{SRi}	Asynchronous reset or preset to internal register output
	t_{SRR}	Asynchronous reset and preset register recovery time

Table 2. MACH 4 Internal/External Parameters Description

External Parameter	Internal Parameter	Description
t_{PD}	t_{PDi}	Input, I/O, or feedback to feedback
t_{COS}	t_{COSi}	Global clock to feedback
t_{COA}	t_{COAi}	Product term clock to feedback
t_{SR}	t_{SRi}	Asynchronous Reset or Preset to registered or latched feedback
$t_{GO(S/A)}$	$t_{GO(S/A)i}$	Latch gate to feedback
t_{PDL}	t_{PDLi}	Input, I/O or feedback to feedback through transparent latch
	t_{BUF}	Feedback to Output

Many of the parameters from the original timing model can be derived from the new, modularized timing parameters. In the enhanced timing model, these original parameters have been eliminated. A list of the eliminated parameters and their derivations is shown in Table 3.

Table 3. Derivation of Eliminated Parameters

Eliminated Parameter and its Description		Derivation
t_{IGOL}	Input latch gate to output through transparent output latch	$t_{IGOSi} + t_{PDLi} + t_{BUF}$
t_{IGO}	Input latch gate to combinatorial output	$t_{IGOSi} + t_{PDi} + t_{BUF}$
t_{IGSA}	Input latch gate to output latch setup using PT output latch gate	$t_{IGOSi} + t_{SAL}$
t_{IGSS}	Input latch gate to output latch setup using global output latch gate	$t_{IGOSi} + t_{SSL}$
t_{ICO}	Input register clock to combinatorial output	$t_{ICOSi} + t_{PDi} + t_{BUF}$
t_{ICS}	Input register clock to output register setup, D-type	$t_{ICOSi} + t_{SS}$
t_{ICS}	Input register clock to output register setup, T-type	$t_{ICOSi} + t_{SST}$
t_{SLLA}	Setup time from input through transparent input latch to PT output gate	$t_{PDILi} + t_{SAL}$
t_{SLLS}	setup time from input through transparent input latch to output gate	$t_{PDILi} + t_{SSL}$
t_{PDLL}	Input to output through transparent input and output latches	$t_{PDILi} + t_{PDLi} + t_{BUF}$
t_{PDLI}	Input, I/O, or feedback to output through input register	$t_{PDILZi} + t_{PDi} + t_{BUF}$

Table 3. Derivation of Eliminated Parameters (Continued)

Eliminated Parameter and its Description		Derivation
t_{SLLAI}	Setup time from input through transparent input latch to PT output gate	$t_{PDILZi} + t_{SAL}$
t_{SLLSI}	Setup time from input through transparent input latch to output gate	$t_{PDILZi} + t_{SSL}$
t_{PDLLI}	Input to output through transparent input and output latches	$t_{PDILZi} + t_{PDLi} + t_{BUF}$

To maintain consistency with the timing models of other MACH families, some of the parameters have been renamed. In particular, the set/reset parameters, t_{RP}, t_{PRW}, and t_{PRR}, have been renamed to t_{SR}, t_{SRW}, and t_{SRR}. Information about all of the timing parameters can be found in the *MACH 4 (A) Family Data Sheet* and in Table 1.

Feedback Timing

In the original MACH 4 timing model, the only feedback path reported in a MACHXL timing report was the external feedback path. Signals using internal feedback were reported as if they had gone through the external feedback path. As a result, the reported delays for those signals would be greater than what would actually be seen in the real device. The new MACH 4 timing model now makes a distinction between those signals using internal feedback and those using external feedback.

To make the distinction between internal and external feedback, several timing parameters have been changed, and the parameter t_{BUF} has been introduced. All of the changed parameters deal with a signal going to the I/O pad. As an example, the parameter t_{PD} was originally defined as an input, I/O or feedback going to a combinatorial output. This parameter is now the sum of two parameters: t_{PDi} and t_{BUF}. The parameter t_{PDi} is defined as the time it takes an input, I/O or feedback to go through a combinatorial path to the internal feedback, while t_{BUF} is the time it takes to go from internal feedback through the output buffer and to the I/O pad.

Input Register/Latch Timing

Another area in which the MACH 4 timing model has been improved is in the reporting of input register/latch timing. Because there was no mechanism for reporting the internal timing of a MACH 4 device, the timing used for input registers/latches could become complicated. The specifications found in the original MACH 4 data sheets relied on timing that went through both an input register/latch and an output register/latch. As an example, the parameter t_{ICOA} represented the clock-to-output time for a signal to go through an input register to a combinatorial macrocell, plus the time it took to go through the combinatorial macrocell and to an I/O pad. This method of determining timing was very difficult for the software implementation of the timing model and for designers attempting to determine their timing requirements.

The MACH 4 timing model has greatly simplified the input register timing by reporting all parameters as internal feedback. The same parameter, t_{ICO}, will no longer exist but rather will be calculated as t_{ICOi}, the clock-to-internal feedback of the input register, plus a t_{PDi} and a t_{BUF}. Because of this modularized timing model, several of the original input register/latch specifications have been eliminated.

USING THE MACH 4 TIMING MODEL

The use of the MACH 4 timing model will be demonstrated using two examples. The first example is a combinatorial logic design and demonstrates the use of internal feedback. The second example is a synchronous sequential logic design and demonstrates how to calculate f_{MAX}.

Example 1

This combinatorial logic design is fit into an M4-64/32. A group of input signals are routed to Block A, which is in high power mode. Logic is generated in array "A" and allocated to macrocell A5, which is configured as a combinatorial path. This logic is sent to pad I/O6, which is configured to have a slow slew rate. The signal delay T1 of this path would be:

$$T1 = t_{PDi} + t_{BUF} + t_{SLW}$$

This logic is also fed back to the central switch matrix via the internal feedback path and then routed to Block D, which is in low power mode. A second logic is generated in array "D" using the first logic along with another group of input signals. This second logic is allocated to macrocell D8, which is configured as a combinatorial path. This second logic is sent to pad I/O31, which is in fast slew rate. The longest delay path of this design would be from Block A to I/O31 and the delay $T_{CRITICAL}$ is:

$$T_{CRITICAL} = t_{PDi} + t_{PL} + t_{PDi} + t_{BUF}$$

The original MACH 4 timing model required an additional t_{BUF} be added to the delay path because internal feedback was not defined.

Example 2

This synchronous sequential logic design has a 16-bit up-counter with load enable and reset. It is fit into an M4-96/48 using 16 macrocells configured with T-type registers. Register inputs are defined by the device inputs and flip-flop output, which is internally fed back to the switch matrix. Under these conditions, the period t_{CNT} is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs.

$$t_{CNT} = t_{COSi} + t_{SST}$$

The f_{MAX} is designated "f_{MAXINT}."

$$f_{MAXINT} = 1/t_{CNT}$$

Again, the original MACH 4 timing model required an additional t_{BUF} be added to the delay path when calculating t_{CNT} because internal feedback was not defined. Consequently, f_{MAX} was slower.

The modular approach to the MACH 4 timing model is straightforward, and its use merely requires the addition of internal parameters to arrive at the device timing.

HIGH SPEED DESIGN WITH MACH 4 DEVICES

While the possibility has always existed to control the implementation of high speed designs into a MACH 4 device, the reporting of the timing never made it easy because no distinction was made between internal and external feedback. The improved MACH 4 timing model makes that critical distinction, making it easier to understand how a design is fit into a device.

During the fitting process, the software may use external feedback on timing critical nodes where internal feedback may be required to meet a particular speed. It is also possible that the software feeds a signal into either the block or global switch matrices, which will affect timing. Constraints can be placed on a design to ensure that the critical paths are fit to meet timing. The more a design is constrained, the more difficult it becomes to fit the design. Some methods that can be used to constrain a design are briefly covered here and are more fully covered in the *MACHXL® User's Manual* and the Application Note entitled, *PI File Reference Guide*. MACHXL software uses the PI File to control the fitting process and constrain the design. It contains pinout and placement information along with directives that determine the fitting algorithms used.

Controlling Feedback

To control the signal feedback path, the PI File directives, FORCE_INTERNAL_FEEDBACK, can be utilized. This PI property forces a signal to use an internal feedback path rather than giving it a choice of using an external or internal feedback path. By forcing a signal to use internal feedback, the delay caused by the output buffer is saved.

CONCLUSION

The MACH 4 timing model provides for a more accurate, easier to understand timing calculation. It defines both internal and external feedback paths and simplifies the timing used for internal registers/latches. By using and understanding the timing model in the proper way, it becomes easier to control the critical path timing in a high speed design using the properties in the PI File.