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# VF1 FPGA Power Estimation

## INTRODUCTION

During the initial stage of system design, the power requirements for the system are considered. To estimate the system power, the power of each active subsystem must be calculated. When the subsystem is a printed circuit board, the power estimation for the subsystem is the sum of the power of each device. To facilitate the process of calculating power, all devices provide graphical or algebraic methods to estimate power. FPGAs are no exception, but they do provide special complexity. FPGAs can implement an indefinite amount of logic designs. Therefore, estimating the power of each design is as unique as the design. In this application brief, a method to estimate the VF1™ FPGA power is presented.

## POWER DISSIPATION

The two components to power in semiconductor devices is static and dynamic power. Static power occurs during inactive device periods whereas dynamic power occurs during active device periods. Stated in equation form:

$$P_{TOTAL} = P_{STATIC} + P_{DYNAMIC}$$

Static power is a function of the static leakage current which a device dissipates. During an inactive period, a device connected to supply and ground has biased internal nodes. Parasitic junctions inherent to internal nodes become active during this period drawing leakage current. Hence, static power follows the equation:

$$P_{STATIC} = V_{CC}\, SI_{CC}$$

Conversely, dynamic power is not a function of leakage current; it is a function of dynamic internal and output switching. Dynamic internal and output switching both charge and discharge capacitive loads. Internal switching charges and discharges internal node capacitors whereas output switching charges and discharges external load capacitors. In either case, current is drawn and dissipated. In equation form:

$$P_{DYNAMIC} = P_{INT} + P_{OUT}$$

Note that output nodes can have internal pull-up resistors or latches to maintain known states during output tristate. The internal pull-ups or latches also contribute to the total power consumption and are included in output power. Moreover, the complexity of calculating PINT and POUT require separate sections for the calculation of each.



Publication# **TB001-1**
Amendment/**0** Issue Date: **November 1998**

## INTERNAL POWER DISSIPATION ($P_{INT}$)

The internal power dissipation of a device is a result of charging and discharging of internal nodes. However, the multiple designs which can be implemented into FPGAs have varying quantities of nodes. This variance provides a unique dilemma: how to produce an estimate for internal power? The method which the FPGA industry has adopted is to generate power data from FPGAs saturated with 16-bit counters. The data is used to determine the power factor $K_{PWR}$ which is used in the following internal power equation:

$$P_{INT} = K_{PWR} V_{CC} F_{MAX} N_{CBB} T_{RATE}$$

Where: $K_{PWR}$ = VF1 FPGA Power Constant (A/Hz)

$V_{CC}$ = Supply Voltage (V)

$F_{MAX}$ = Maximum Clock Frequency (Hz)

$N_{CBB}$ = Total Number of VF1 FPGA Configurable Building Blocks Used

$T_{RATE}$ = Average Number of Internal Nodes Toggling at a Given Clock (20% for most designs; 12.5% for 16-Bit Counters)

| VF1 FPGA | $K_{PWR}$ (A/Hz) |
|---|---|
| VF1012 | TBD |
| VF1020 | TBD |
| VF1025 | 7 E-12 |
| VF1036 | TBD |

### Output Power Dissipation ($P_{OUT}$)

Output power dissipation is a function of capacitive load, supply voltage, output switching frequency, and the quantity of outputs switching at a given time. Stated mathematically:

$$P_{OUT} = \sum_{i=1}^{n} C_i V_i^2 F_i$$

Where: $C_i$ = Output Capacitive Load (F)

$V_i$ = Output Voltage Swing (V)

$F_i$ = Output Switching Frequency (Hz)

n = Total Number of Outputs

The implication of the previous equation is that every output needs to be analyzed to calculate the output power. For a simpler estimation, the following simplifications can be made.

| | | | |
|---|---|---|---|
| $C_i$ | $\cong$ $C_{avg}$ | = | Average Output Load Capacitance (F) |
| $V_i$ | = $V_o$ | = | Output Voltage Swing (V) |
| $F_i$ | $\cong$ 1/2 $F_{max}$ | = | Average Output Switching Frequency (Hz) |
| n | $\cong$ $N_{out}$ * $T_{rate}$ | = | (Total Number of Outputs) * (Percentage of Outputs Switching at a Given Time) |

The simplifications result in the following equation:

$$P_{OUT} = 1/2\ C_{avg}\ V_o^2\ F_{max}\ N_{out}\ T_{rate}$$

## EXAMPLE

For an example, consider a 32-bit counter running at 50 MHz and driving a 32-bit bus loaded with 30 pF. The target device is a VF1025. The capacity needed for this design is 32 CBBs and the toggle rate is 6.25%. Using this information, the internal and external power estimates are calculated below.

Internal Power: $P_{INT} = K_{PWR}\ V_{CC}\ F_{MAX}\ N_{CBB}\ T_{RATE}$

$= (7E\text{-}12\ A/Hz)\ (3.3V)\ (5OE{+}6\ Hz)\ (32)\ (0.0625)$

$= 2.31\ mW$

Output Power: $P_{OUT} = l/2\ C_{avg}\ V_o^2\ F_{max}\ N_{out}\ T_{rate}$

$= l/2\ (30E\text{-}12\ F)\ (3.3V)^2\ (5OE{+}6\ Hz)\ (32)\ (0.0625)$

$= 16.34\ mW$

Total Power: $P_{TOT} = P_{STATIC} + P_{DYNAMIC}$

$= P_{STATIC} + P_{INT} + P_{OUT}$

$= 0{+}2.31\ mW + 16.34\ mW$

$= 18.65\ mW$

## SUMMARY

Power estimation during the initial phase of system design must be calculated to determine whether system power constraints are satisfied. To calculate the system power, each individual device must provide a method to calculate power. For VF1 FPGAs, a method for calculating the total power dissipation has been provided. A designer should use this approach as an approximation. Actual power consumption will ultimately depend on the unique implementation of a design into a VF1 FPGA.