VANTIS
BEYOND PERFORMANCE

# Power-Up Reset

MACH® devices have been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will depend on the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways $V_{CC}$ can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The $V_{CC}$ rise must be monotonic from ground.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

| Parameter Symbol | Parameter Description | Max | Unit |
|---|---|---|---|
| $t_{PR}$ | Power-Up Reset Time | 10 | µs |
| $t_S$ | Input or Feedback Setup Time | See Switching Characteristics | |
| $t_{WL}$ | Clock Width LOW | | |
| $V_{PWR}$ | Power-up Voltage for 3.3V Devices | 2.7 | V |
| | Power-Up Voltage for 5V Devices | 4 | V |

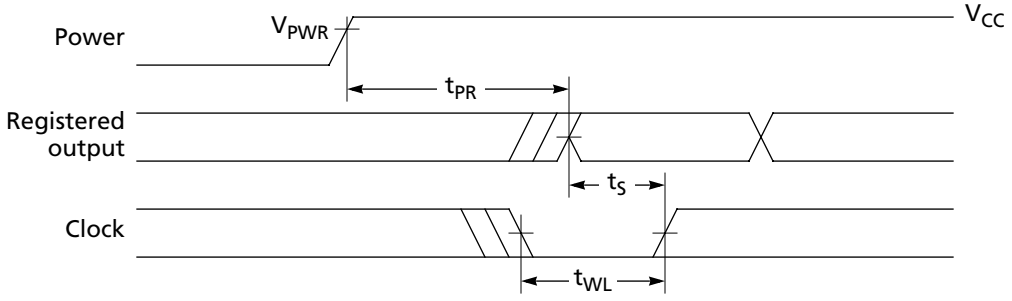


**Figure 1. Power-Up Reset Waveform**

General Information