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BEYOND PERFORMANCE

Hot Socketing and Mixed Supply Design with MACH 4 and MACH 5 Devices

ABSTRACT

Vantis provides robust and feature-rich I/O structures on its MACH® 4 and MACH 5 families of devices. To take advantage of these features, it is helpful to understand the characteristics on both a family basis and a technology basis. This technical note will describe two Vantis I/O characteristics: hot socketing and mixed supply design as they pertain to the MACH 4 and MACH 5 families manufactured in Vantis' 0.50-µm (EE6.5) and 0.35-µm (EE7) process technologies.

BACKGROUND

The Vantis MACH 4 and MACH 5 CPLD families have superior routability, performance, and I/O characteristics that make them ideal for today's complex system designs. The routability features include multiple switch matrices, complex macrocell architectures, wide product-term allocators, and large numbers of inputs into the arrays. The performance features include fast, predictable speeds, power management capabilities, and slew rate control. Detailed information about MACH routability and performance can be obtained from the MACH data sheets.

The I/O characteristics are what really set the MACH 4 and MACH 5 devices apart from all other architectures. Some of the advanced features they offer to enhance a system design include Bus-Friendly™ latches, hot socketing, mixed supply capability, and PCI compliance. Due to their dependence on process technology, hot socketing and mixed supply design capability need additional description over that found in the data sheets.

Vantis has access to world class process technologies. The two process technologies used in the manufacture of the MACH 4 and MACH 5 devices are the 0.50-µm L_{eff} process and the 0.35-µm L_{eff} process. As device feature sizes are reduced, so must the voltage supply because of the internal electric fields that are generated across the gate oxides. The 0.50-µm process is a 5-volt technology, while the 0.35-µm process is a 3.3-volt technology. As a result, the designs used in the I/O and input buffers will be different and will have somewhat different characteristics. Table 1 shows which of these process technologies is used to manufacture the MACH 4 and MACH 5 devices, and what V_{CC} supplies each can be used with.

Table 1. Device Process and Supply Reference

V_{cc} Supply	0.50-µm	0.35-µm
3.3 Volts		All M4LV-M5LV
5 Volts	M5-128 M5-192 M5-256	All M4 M5-320,M5-384 M5-512

Application Notes

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HOT SOCKETING

Hot socketing is a feature that means different things to different designers. There are two common scenarios found in hot socketing environments. The first is when a board or device is plugged into a system that is already powered-up. The second is a board in a system where the board is powered-down while the system is still powered-up and active, and the powered-down board or devices continue to be connected to the active nets in the system. Due to design differences between the two manufacturing processes, various MACH devices will behave differently for each hot socketing scenario.

In the scenario where a device or board is plugged into an already powered-up system, the principal cause for concern is latch-up. When inserting a part or board, it can be several milliseconds before all of the required connections have been made, and there is no particular order in which those connections are made. As a result, signal pins can be connected and driven before either V_{CC} or ground, and this can lead to latch-up in CMOS devices if they are not designed to handle this condition. When a device latches-up, a low-impedance path to ground is formed within the device, and the device begins to sink large amounts of current. If the situation is not rectified quickly (i.e., by cycling the system power), the device could be thermally destroyed, necessitating its replacement.

In the scenario where a powered-down device is in a powered-up system, the possibility of signal disturbance can arise. Signal disturbance takes place when an inactive device affects the functionality of active signals. This can happen when the inactive device has a leakage path to either V_{CC} or ground, or when the device is driving the signal line during power-up or power-down. All MACH 4 and MACH 5 devices tri-state their I/Os during power-up and power-down, and as a result, this is not a concern for bus disturbance.

Hot Socketing Specification

The most dangerous of the two hot socketing scenarios takes place when a voltage is placed on an input, and the device goes into latch-up as a result. Most devices are designed to prevent latch-up from happening when V_{CC} is at a nominal level such as 5.0 volts or 3.3 volts. When V_{CC} is at 0.0 volts however, the situation is much different in that signals driven into inputs or I/Os could potentially force the device into latch-up. The hot socket latch-up current specification in Table 2 indicates the amount of latch-up current that MACH devices can tolerate without being damaged. This information also appears in the Absolute Maximum Ratings section of the device data sheets.

Table 2. I_{LUHS} Specification

Parameter Symbol	Parameter Description	Test Description	Max	Unit
I_{LUHS}	Hot Socket Latch-up Current	V_{CC} = 0.0 Volts, V_{IN} = 5.5 Volts	200	mA

The second of the two scenarios is much less dangerous from both the device standpoint and the system design standpoint. When a device no longer has power applied to it yet is still connected to active signals and busses, that device should have no effect on the active signals. If it does, precautions must be taken to ensure the system will not be adversely affected and can tolerate the strong leakage paths. If the system cannot tolerate the influence of the powered-down devices, there are design techniques that can be employed to work around the problems.

5-Volt, 0.50-µm I/O Buffer Hot Socketing Characteristics

The 5-volt, 0.50-µm MACH 5 devices are perhaps the most robust of the devices from the hot socketing standpoint. Not only do they meet the requirements for latch-up current, but they also have a minimal amount of leakage current when the devices have no power applied. During power-up, all of the MACH 4 and MACH 5 devices have their output drivers disabled such that the I/Os are in a high impedance state. Because of the design and the process, the 0.50-µm MACH 5 devices have a leakage current of less than 10 µA when V_{CC} = 0.0 volts and 0 V < V_{pin} < 5.5 V.

5-Volt, 0.35-µm I/O Buffer Hot Socketing Characteristics

As with the 5-volt, 0.50-µm devices, the 5-volt, 0.35-µm MACH 4 and MACH 5 devices also meet the requirements for latch-up. These devices are not as robust as the 0.50-µm devices when it comes to leakage current and source a significant amount of current that must be considered when using these devices in a hot socketing environment. During power-up and power-down, the output drivers are disabled. However, because of the nature of the 3.3-volt process and its design requirements, there is a parasitic diode that becomes forward biased and will source current when V_{CC} is less than 0.7 volts. The I-V curves in Figure 1 show the leakage current that can be expected on an input or I/O pin for a typical device when 0 V < V_{CC} < 0.6 V. Note that the differences in I_{LK} for 0.4 V < V_{CC} < 0.6 V are minimal and are represented in Figure 1 by V_{CC} = 0.6 volts.

The curves are shown with V_{PIN} at a maximum value of 3.0 volts. This was done because minimum V_{IH} levels for most devices are 2.0 volts or greater, and 3.0 volts will provide sufficient margin. When designing a system which could be affected by devices exhibiting leakage current when V_{CC} = 0 volts, the primary consideration that must be taken into account is the integrity of the signal levels and the ability to maintain minimum V_{IH} levels. Because the leakage currents are relatively small for this group of devices, the effects can be overcome with the use of pull-up resistors on the signals connected to the MACH device. To have the desired effect, the pull-up resistors must be placed at the system level that will remain powered-up rather than on the board where the MACH device is located that will be powered-down. The example below shows how to select the correct value for a pull-up resistor that will overcome the leakage current on a signal which needs to be held high during power-up:

Example: V_{CC} =5.0 volts, V_{IH} (min) = 2.0 volts

at V_{IH} (min) = 2.0 volts and a device V_{CC} of 0.0 volts (worst case), I_{LK} = 0.85 mA then RPU = (V_{CC} - V_{IH}) / I_{LK} = (5 V - 2 V) / 0.85mA = 3.53 KΩ

The pull-up resistor needed to maintain signal integrity would have a value of 3.3 KΩ.

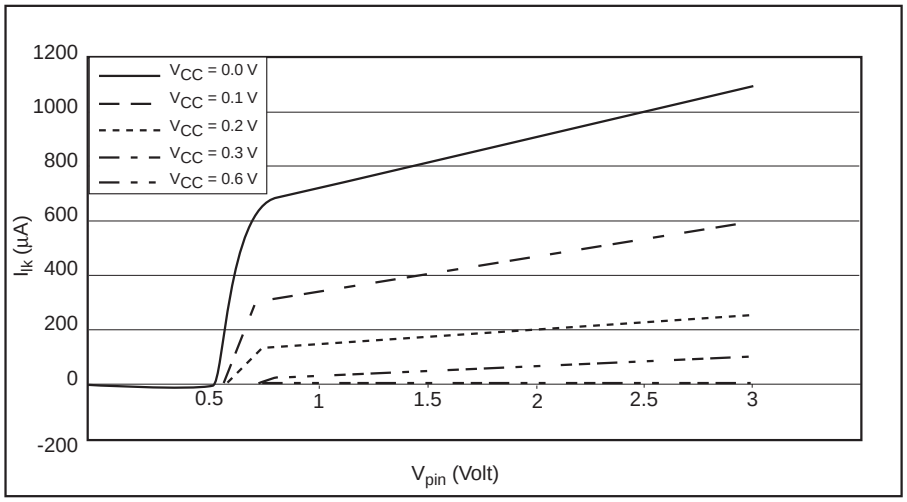

Figure 1. 5-Volt, 0.35-µm Typical Leakage Current Characteristics

3.3-Volt, 0.35-µm I/O Buffer Hot Socketing Characteristics

The 3.3-volt MACH 4 and MACH 5 devices meet the requirements for latch-up current but are significantly worse when it comes to leakage current as shown below in Figure 2. The maximum leakage current is nearly 9 mA when V_{CC} is 0 volts and V_{PIN} is 3.0 volts. Using the assumptions from the example above, the resistor value needed to maintain minimum V_{IH} levels is on the order of 462 **Ω**. This smaller resistor will have an adverse effect on both speed and power consumption and should be avoided. The reason for the increased leakage current is a result of the need for PMOS transistors in the design of the output buffers to pull the output up to the V_{CC} rail when the pin is driving high. The PMOS transistor creates a parasitic diode that is the source of the leakage when V_{CC} < 0.7 volts.

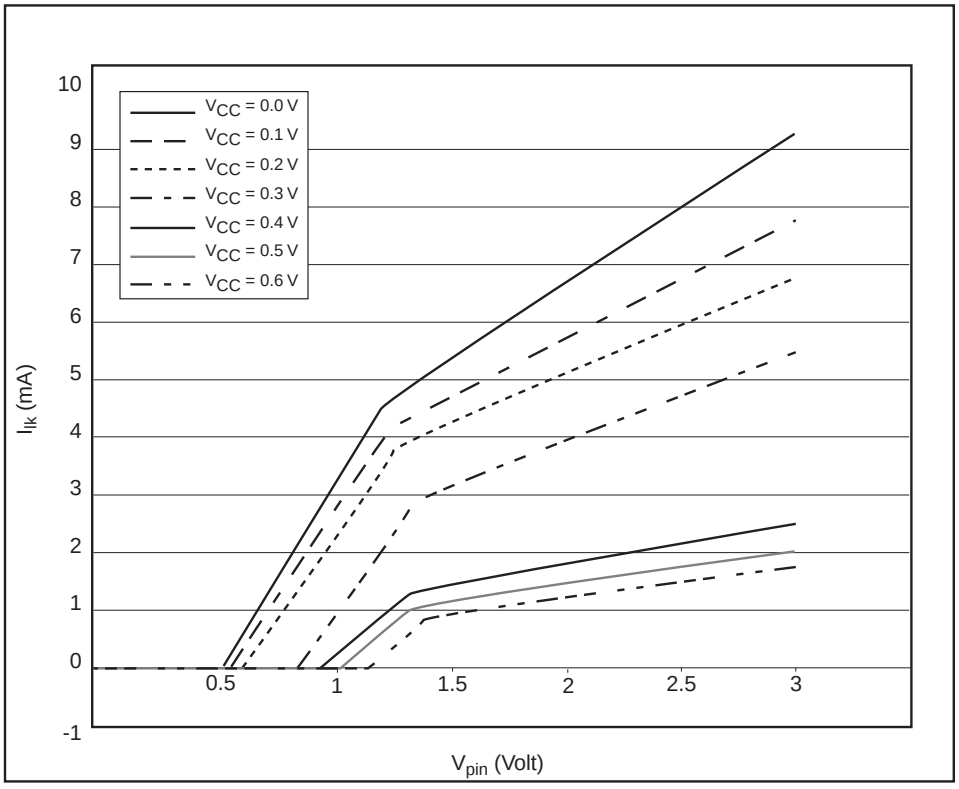

Figure 2. 3.3-Volt, 0.35-µm Typical Leakage Current Characteristics

As a result, the design techniques needed to use the 3.3-volt, 0.35-µm devices in a hot socketing environment are somewhat more difficult and costly to implement. One technique is to use buffers or FET equivalent switches on the signals connected between the MACH device and the system. The drawback to this approach is that additional board space is required and there is an additional delay in the speed paths. If board space is not at a premium and speed is not an issue, this may be an acceptable option. A second technique that can be implemented is the use of hot-socket connectors which keep power and ground supplied to the board until after the signal lines have been disconnected. They have longer power and ground pins that guarantee the I/Os are disconnected prior to (for hot removal) or connected after (for hot insertion) the supply connections. By doing so, there is no need to first power down a board before inserting or removing it from a system. When using this option, it is important for a designer to understand exactly how the system will respond in this situation. These techniques, while not optimal, will allow the use of these devices in a design requiring hot socketing capability.

MIXED SUPPLY DESIGN

As the semiconductor industry migrates from a 5-volt process technology to a 3.3-volt process technology, the need to be able to design in a mixed supply environment becomes increasingly important. There are four situations to be aware of when designing in such an environment to ensure the reliability of all devices. The first is when a 3.3-volt device drives the input of a 5-volt MACH device. The second is when a 5-volt MACH device drives the input of a 3.3-volt device. The third is when a 3.3-volt MACH device drives the input of a 5-volt device, and the final is when a 5-volt device drives the input of a 3.3-volt MACH device. All of the conditions are described by the minimum and maximum specifications for V_{OH} and V_{IH}.

5-Volt Tolerant and 3.3-Volt Safe Specifications

The specification for 5-volt tolerance deals with the device input levels while 3.3-volt safety deals with device output levels. For a 3.3-volt device to be 5-volt tolerant, it must be able to handle an input as great as V_{CC} (max) for the 5-volt device when V_{CC} of the 3-volt MACH device is at a minimum. For a 5-volt device to be 3.3-volt safe, its outputs must drive no higher than V_{IH} (max) of the 3.3-volt device when V_{CC} for the 3.3-volt device is at a minimum and V_{CC} for the 5-volt MACH device is at its maximum value. Furthermore, the source current of the pin being driven by the 5-volt MACH device should be 0 mA. Additionally, the same 5-volt MACH device must meet the minimum requirements needed to reliably interface with devices that conform to the TTL level specification. The TTL specification requires that the outputs drive no less than the V_{IH} (min) of the 5-volt TTL device when V_{CC} (5-volt TTL device) is at a minimum and with a load current of 3.2 mA. The ideal specifications are given in Table 3, and are derived from the requirements needed for both 5-volt TTL and 3.3-volt CMOS devices. The 3.3-volt CMOS requirements can be found in the JEDEC LVCMOS specification, JED-8A. The value for V_{OH} (max) is given for a 5-volt device driving into a 3.3-volt CMOS device that is operating at its minimum V_{CC} of 3.0 volts. In this condition, the determining factor is set by the CMOS device's V_{IH} (max) limit of V_{CC} + 0.3 when V_{CC} is at 3.0 volts and with no source current. If a nominal V_{CC} of 3.3 volts is assumed rather than the minimum V_{CC} of 3.0 volts, V_{OH} (max) will be 3.6 volts. The conditions necessary to meet the hot socketing requirements without going into latch-up also guarantee the V_{IH} specifications in Table 3. This includes all of the MACH 4 and MACH 5 devices. All of these MACH devices will also meet the minimum TTL specification for V_{OH} when V_{CC} = Min and I_{OH} = -3.2 mA. The following discussions will cover the V_{OH} maximum specification.

Table 3. 5-Volt Tolerant/3.3-Volt Safe Ideal Specifications

Parameter Symbol	Parameter Description	Test Description	MIn	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -3.2 mA	2.4		V
V_{OH}	Output High Voltage	V_{CC} = Max, I_{OH} = 0 mA		3.3	V
V_{IH}	Input High Voltage	V_{CC} = Min		5.5	V

0.50-µm, 5-Volt Device Mixed Supply Design Characteristics

The 0.50-µm devices were not originally designed to meet the specifications given above, and as a result do not meet them. This does not, however, mean these devices cannot be used in a mixed supply environment. When V_{CC} is at 5.25 volts, an output will typically need to source less than 25 µA to provide an output voltage of 3.6 volts. Additionally, many systems will not be designed to operate at the maximum V_{CC} of 5.25 volts, but rather will operate at the more typical 5.0 volts. The design of the output buffer is such that when V_{CC} drops 0.1 volts, so does the output voltage. As a result, a more typical V_{OH} when V_{CC} is at 5.0 volts will be around 3.4 volts. This ensures that a 5-volt device can drive a 3.3-volt device running at 3.1 volts or greater.

The 0.50-µm devices were designed such that V_{OH} will be no greater than 3.3 volts with a source current of -3.2 mA when V_{CC} (min) = 4.75 volts. All of the 0.50-µm devices will meet this specification, but are not considered 3.3-volt safe since they do not meet an I_{OH} specification which is compatible with CMOS device inputs. These devices are tested to meet a specification of V_{OH} = 3.5 volts when V_{CC} = 5.25 volts and I_{OH} = -1.5mA.

An additional measure of safety can be added at the system level by using series current limiting resistors on those outputs that are required to be 3.3-volt safe. The series resistor should be no less than 150 Ω, which will limit the maximum amount of current driven into the 3.3-volt device's input. This also ensures that the current flow into the ESD structure on that input will be less than 10 mA, which is considered safe in terms of latch-up current (typically specified at 200 mA).

0.35-µm, 3.3-Volt and 5-Volt Device Mixed Supply Design Characteristics

The 0.35-µm, 3.3-volt devices will not have any difficulty meeting the V_{OH} (max) specifications because their output buffers can only drive up to the level of V_{CC}. As a result, for the 3.3-volt MACH 4 and MACH 5 devices, V_{OH} (max) = V_{CC}. The design of the 0.35-µm, 5-volt device output buffers limits the maximum output voltage to 3.3 volts when V_{CC} = Max and I_{OH} = 0 mA. All of the 0.35-µm MACH 4 and MACH 5 devices are safe for mixed supply design and can accept inputs from or drive outputs to any 3.3-volt or 5-volt device.

CONCLUSION

The MACH 4 and MACH 5 devices offer several advanced features that can be invaluable in a system design. To take full advantage of these features, the designer must be aware of the effects that each feature may have on the system. Because of process and design differences, not all of the devices will act in quite the same manner. The classifications for each of the devices are:

- 5-volt, 0.50-µm MACH 5 devices - M5-128, M5-192, and M5-256
- 5-volt, 0.35-µm MACH 4 and MACH 5 devices - All MACH 4 devices, M5-320, M5-384, and M5-512
- 3.3-volt, 0.35-µm MACH 4 and MACH 5 devices - All MACH 4LV and MACH 5LV devices

Where hot socketing is concerned, there are differences between all three of the categories that the designer needs to be aware of. With mixed supply design, the differences are found between the 0.50-µm devices and the 0.35-µm devices and are primarily concerned with V_{OH} levels. By knowing and understanding the differences between the devices, a designer will be able to best use the advanced features offered in each.