VANTIS

BEYOND PERFORMANCE

Packages

INTRODUCTION

Vantis provides its programmable logic devices (PLDs) in a wide range of packages. These packages provide benefits such as high power dissipation capability, small footprint, and high I/O. This section provides details about the packages that Vantis supplies.

EXTERNAL LEAD DESIGNS

The shape of the leads on leaded surface-mount packages, which includes all but the BGA package, are formed in either a gull-wing or J-bend shape. Both lead shapes offer the advantage of being flexible, which allows them to absorb thermal expansion mismatches between the IC package and the board.

Plastic Package Design	Leadcounts	Lead Design/Direction
Leaded Chip Carrier (PLCC)	20—84 leads	J-Bend/4 sides
Quad Flat Pack (PQFP)	100—240 leads	Gull-wing/4 sides
Thin Quad Flat Pack(TQFP)	44—176 leads	Gull-wing/4 sides
Ball Grid Array (BGA)	256—352 balls	Solder Balls/Array
Plastic Dual-In-Line (PDIP)	20—28 leads	Through-hole
Small Outline Plastic (SOIC)	20—24 leads	Gull-wings/2 sides

- Gull-Wing Lead Design

  Gull-wing leads are similar to dual-in-line, through-hole leads except that the leads are bent at the tips to rest flat on the board surface. This provides a built-in standoff between the package and the board, enabling thorough board cleaning and easy-to-inspect solder joints.

- J-Bend Lead Design

  Like the gull-wing design, J-bend leaded packages can be mounted directly to the board, thus offering a built-in standoff and all the advantages inherent in this. A strong, inspectable bond is easily attainable provided the solder lands include extensions out from under the package. The J-bend design also allows easy socketing, which facilitates device testing and programming.

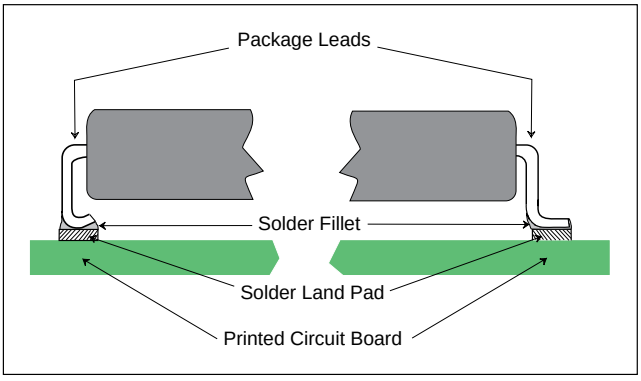

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Figure 1. J-Bend (On the Left) and Gull-Wing Lead Formations (On the Right) Allow Components to be Mounted onto the Surface of the Circuit Board

PACKAGE MATERIALS

The materials used in Vantis' plastic packages and flammability data are provided in this section.

Table 1. Flammability Ratings per Package Type and Size

Package	Leadcount	Ul Rating & Oxygen Index[1]	Resin Weight Per Unit (grams)	Compound Weight Per Unit (grams)
Plastic Leaded Chip Carriers (PL, PLH)	20 (PL)	94 V-0 & ≥28%	0.1	0.6
	28 (PL)		0.2	1.0
	44 (PL)		0.5	2.0
	68 (PL)		1.1	4.4
	84 (PL)		1.8	7.3
	84 (PLH)		1.4	5.8
Metric Plastic Quad Flat Pack (PQR)	100 (PQR)	94 V-0 & ≥28%	0.3	1.4
	144 (PQR)		1.2	4.8
	160 (PQR)		1.1	4.8
	208 (PQR)		1.2	4.8
Thermally Enhanced Metric Plastic Quad Flat Pack (heat spreader (PRH), heat sink (PQE))	160 (PQE)		0.9	3.8
	208 (PRH)		1.1	4.6
	208 (PQE)		0.9	3.8
	240 (PQE)		0.9	3.97
Thin Plastic Quad Flat Pack (1.0 mm thick (PQT); 1.4 mm thick (PQL) TQFP	44 (PQT)	94 V -0 & ≥ 28%	<0.1	0.1
	48 (PQL)		<0.1	0.1
	100 (PQL)		<0.1	0.3
	144 (PQL)		<0.1	0.7
	176 (PQL)		<0.1	0.7
Plastic Ball Grid Array	256 (BGD)	substrate: UL 94V-O glob top: UL 94HB	0.07 (Note 2)	0.26 (Note 3)
	352 (BGD)		0.12 (Note 2)	0.45 (Note 3)
Plastic Dual-In-Line	20	94 V -0 & ≥ 28%	0.3	1.2
	24 (PD3) (Note 3)		0.3	1.5
	28 (PD3) (Note 3)		0.4	1.6
Small Outline Plastic	20		<0.1	0.2
	24		<0.1	0.2

Notes:

1. *The mold compound is tested according to the ASTM Standard D2863-77,:Standard Method for Measuring Oxygen Concentration to Support Candlel-Like Combustion of Plastics (Oxygen Index)." The flammability rating is determined by the Underwriters Laboratories (UL) Standard 94, "Test for Flammability of Plastic Materials for Parts in Devices and Applications.*
2. *Refers to the weight of the glob-top encapsulation.*
3. *PD3 (300-mil) designates a PDIP design for which the package mil size is not what is standard for that lead count.*

Table 2. Package Materials [1]

Package Type & Leadcount	Package Part		Material	Percentage of Composition[2]
All Plastic Surface Mount Packages (excluding Ball Grid Array Packages)				
All Package Types and Lead Counts	Package body		epoxy novolac	13.0%—30.5%
			silica filler	69.5%—87.0%
			chlorine	7—80 ppm
			bromine	0.0%—0.9% weight
			antimony trioxide	0%—1.8%
			sodium	5—40 ppm
			potassium	0—10 ppm
	Die attach adhesive		epoxy	20%—30%
			silver filler	80%—70%
			sodium	5—50 ppm
			chlorine	5—50 ppm
			potassium	5—20 ppm
	Die-to-package interconnections	bond wire	gold	99.99%
	Leadframe	copper	copper	96.2%—99.9%
			nickel	3.0%
			iron	0.005%—2.35%
			silicon	0.65%
			magnesium	0.15%
			zinc	0.12%
			zirconium	0.0%—0.15%
			phosphorous, aluminum, manganese	traces, depending on the leadframe supplier
	Lead plating		tin/lead	85%, +5%, -0%/15%, -5%

Notes:

1. *Excluding the die*
2. *Ranges are provided in some cases, to cover the differences in materials per supplier. Contact your local Vantis sales representative for more product specific information.*

Table 3. Package Materials [1]

Package Type & Leadcount	Package Part		Material	Percentage of Composition [2]
Ball Grid Array Packages				
All Plastic Package Versions	Package body	substrate	organic resin	40%—60%
			glass fibers	40%—60%
		circuitry	copper (Note 3)	99%—100%
		solder mask	resin	40%—60%
			inorganic fillers	35%—55%
			additives	1%—10%
	Die attach adhesive		epoxy	20%—30%
			silver filler	70%—80%
	Die-to-package interconnections	bond wire	gold	99.99%
	Package-to-board outerconnections	solder balls	tin, lead	63%, 37% (eutectic)
	Glob top encapsulation		epoxy resin	20%—40%
			silica filler	60%—80%
	Heat spreader		copper	96%—99%
			iron	0%—2.4%

Notes:

1. *Excluding the die*
2. *Ranges are provided in some cases to cover the differences in materials per supplier. Contact your local Vantis sales representative for more product specific information.*
3. *The internal leads are electroplated with nickel, copper, and gold. These persentages vary depending on the specific package. Contact your local Vantis sales represenative should you need product specific information.*

Table 4. Materials Not Detectable in Vantis' Plastic Components

4-Aminodiphenyl and its salts	Hydrazine	Polyhalogenated Dibenzofurans/Dioxins
Ammonium Salts	2-Naphthylamine and its salts	Polychlorinated Naphthalenes
Arsenic	Nickel Tetracarbonyl	Polycyclic Compounds
Asbestos	N, N-Dimethylformamide	Selenium
Benzene	N, N-Dimethylacetamide	Tetrabromobenzylimidazole
Brominated Diphenyl Oxides	N-Nitrosoamines	Tetrabromobisphenol A
Cadmium and Cadmium Compounds	Mercury and Mercury Compounds	Tetrabromoethylene
Decabromodiphenyl Ether	Ozone Depleting Compounds	Toluene
4, 4-Diaminophenyl Methane	Octabromodiphenyl Ether	Triethylamine
Epichlorhydrine	Oils and Greases	Tris (2, 3-Dibromopropyl) Phosphate
Ethylene Glycol ethers	Palladium	Tris (aziridinyl) Phosphin Oxide
Fluorine	Phthalate	Vinyl Chloride Monomer
Formaldehyde	Halogenated Aliphatic Hydrocarbons	Xylene
Halogenated Aliphatic Hydrocarbons	Polyhalogenated Bi/Triphenyl Ethers	

Thermally Enhanced Plastic Package Designs

In addition to the standard package designs, Vantis' PLCC and PQFP package families include high-performance variations for devices having greater power and faster speed. We are also evaluating high-performance designs in our TQFP and BGA package families.

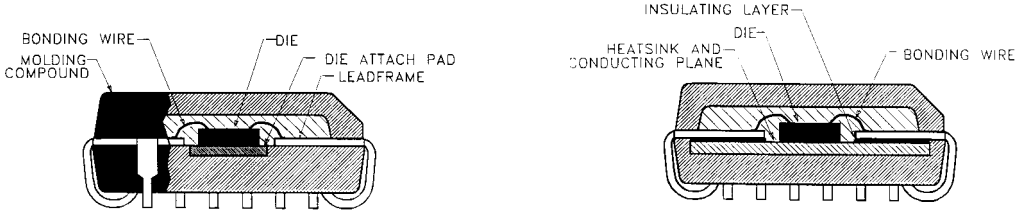
The high-performance package designs include two variations: one in which a heat spreader is embedded in the package, and the other entails assembling into the package a heat sink which is visible on the topside of the package.

Heat Spreader Design

This design includes a heat sink that is attached to a padless leadframe using a B-stage adhesive. The heat sink, referred to in this design as a heat spreader because it serves as the die attach pad, fills the narrow gap between where the die-attach pad would normally end and the leads begin. This provides a more efficient means of heat transferal since heat from the device no longer has to pass over a gap to escape to the leadframe. Also thermally advantageous, a thin strip of insulating tape in the B-stage epoxy allows the heat sink to be quite close to the leadframe without actually touching it (since to do so would cause an electrical short.

The heat sink also serves as a fixed potential plane in that its voltage level will not vary much from the voltage on the back of the die. Because the heat sink is underneath the die, separated from it by only the epoxy and the 0.003-inch thick insulating tape, it is closer to all the input/output, power, and ground leads than in a standard PLCC package (in which the closest ground is on the circuit board, ≈0.090 inch below the leads). This significantly lowers lead inductance which keeps the noise level down.

Comparative analysis of package performance using the same device in a standard versus a high-performance PLCC package have shown the latter to outperform the standard package in the areas of lead inductance, thermal impedance (θ_{ja}), speed, and yields.



Standard PLCC Package Design

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High Performance PLCC Package Design

21552B-004

Figure 2. A High-Performance PLCC Package Includes a Heat Spreader Within the Package—a Feature not Present in a Standard PLCC Package Design

Exposed Heat Sink Design

For very high-power devices, it is necessary that the heat sink conduct the heat all the way to the surface of the IC package. For such devices, a much thicker heat sink is used to span the entire encapsulated portion of the leadframe. This design can be achieved in either a cavity-down version (see Figure 3), in which the heat sink is visible on the top of the package, or a cavity-up version,

in which the heat sink is exposed on the package bottom (Figure 3). This style of heat sink is sometimes referred to as a heat slug, since the metal comes in contact with the chip itself (as opposed to a heat sink that is attached to the exterior of the package body).

Thermal Performance Improvement

The improvement in thermal performance for, say, a 28-mm body PQFP, is approximately 30 percent for the heat spreader design and 60 percent for the exposed heat sink version.

Contact your Vantis sales representative should you need additional information about Vantis' high-performance plastic package designs.

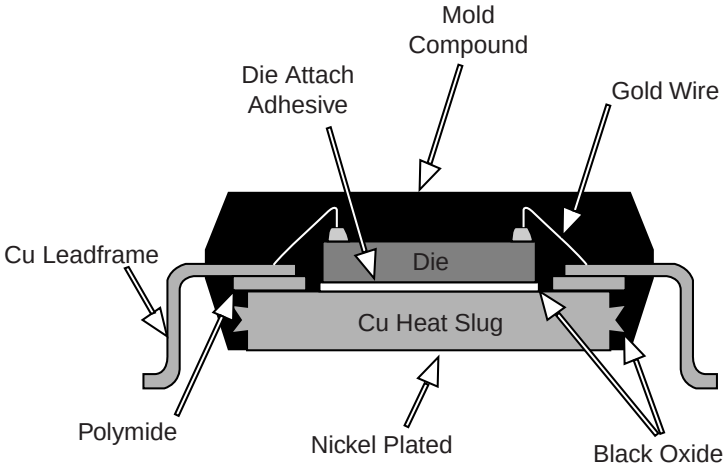

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Figure 3. A Heat Sink Assembled in a Thermally Enhanced PQFP (Known as PQE Package) is Visible on the Bottom Side of the Package

Plastic Leaded Chip Carrier (PLCC) Packages

The PLCC package design is an attractive alternative to higher leadcount plastic DIPs because it can accommodate larger die sizes and offer the advantages of SMT. Above 84 leads, the PLCC configuration and lead-pitch are impractical given the availability of lower profile, high leadcount packages, such as finer pitch PQFPs.

The PLCC package construction consists of a device attached to the die pad of a leadframe, the circuitry of which is wire bonded to the lead fingers. A plastic epoxy material is injection-molded to encapsulate the device/leadframe configuration. The quad-directional leads are trimmed and formed to a J-bend formation.

The 50-mil lead-pitch of a PLCC package is half the conventional lead spacing of a DIP. This, coupled with the PLCC leads being located on all four sides of the package, greatly reduce the footprint. A comparison of package dimensions is shown in Table 5.

Table 5. PLCC (PL) [1] Package Size Overview

Leadcount	Package Body Area (L X W) Inches SQ.	Lead Pitch Inches	Package Weight (Grams)
20	0.125	0.05	0.65
28	0.205		1.07
44	0.426		2.22
68	0.908		4.62
84	1.33		7.45

Note:

1. PL is Vantis' internal abbreviation for a PLCC package.

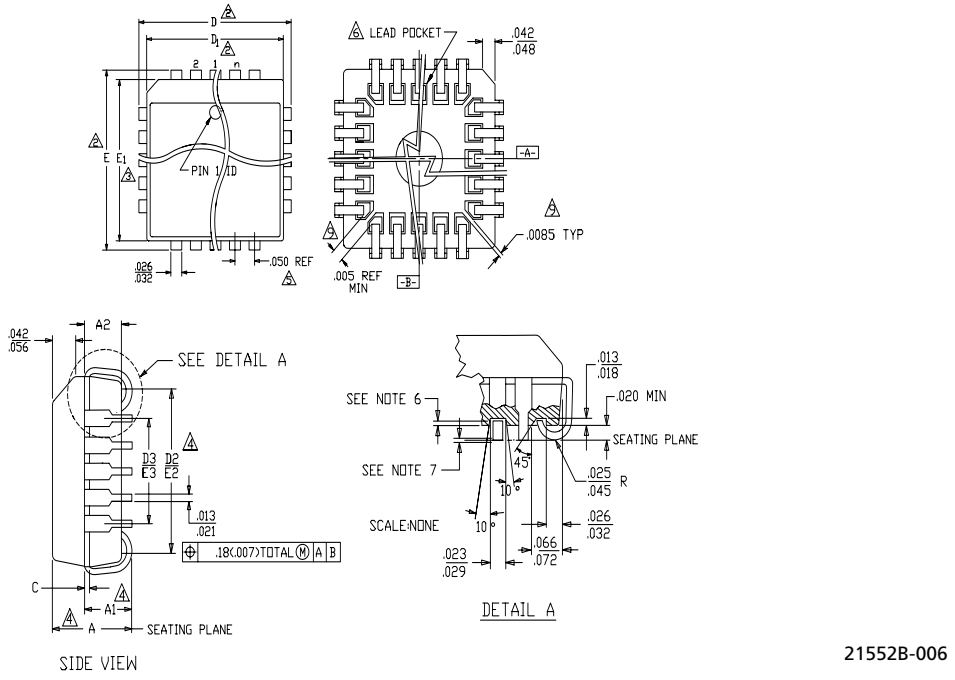

Figure 4. Square Packages (PL)

Dimension Codes	Vantis Package Type & Leadcount (JEDEC Drawing Number)									
	PL 020		PL 028		PL 044		PL 068		PL 084, PLH084	
	(MS-018(A)AA)		(MS-018(A)AB)		(MS-018(A)AC)		(MO-047(B)AE)		(MO-047(B)AF)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.165	0.180	0.165	0.180	0.165	0.180	0.165	0.180	0.165	0.180
A1	0.090	0.120	0.090	0.120	0.090	0.120	0.090	0.130	0.090	0.130
A2	0.062	0.083	0.062	0.083	0.062	0.083	0.062	0.083	0.062	0.083
D, E	0.385	0.395	0.485	0.495	0.685	0.695	0.985	0.995	1.185	1.195
D1, E1	0.350	0.356	0.450	0.456	0.650	0.656	0.950	0.956	1.150	1.156
D2, E2	0.290	0.330	0.390	0.430	0.590	0.630	0.890	0.930	1.090	1.130
D3, E3	0.200 REF		0.300 REF		0.500 REF		0.800 REF		1.000 REF	
C	0.009	0.015	0.009	0.015	0.009	0.015	0.007	0.013	0.007	0.013

Notes:

1. *All dimensions are in inches.*
2. *Dimensions "D" and "E" are measured from the outermost point.*
3. *Dimensions "D1" and "E1" do not include corner mold flash. Allowable corner mold flash is 0.010 inch.*
4. *Dimensions "A, A1, D2, and E2" are measured from the points of contact to the base plane.*
5. *Lead spacing as measured from the center-line to the center-line shall be within ±0.005 inch.*
6. *J-bend lead tips should be located inside the "pockets."*
7. *Lead coplanarity shall be within 0.004 inch as measured from the seating plane.*
8. *Lead tweeze shall be within 0.0045 inch on each side as measured from a vertical flat plane.*
9. *The lead pocket may be rectangular (as shown) or oval. If the corner lead pockets are connected, then 0.005-inch minimum lead spacing is required.*
10. *PL is Vantis' internal abbreviation for a PLCC. PLH refers to one that has been thermally enhanced with an embedded heat spreader.*

Plastic Quad Flat Pack (PQFP) Packages

PQFP packages were developed primarily for high-leadcount applications. The finer lead-pitch of a PQFP enables this design to accommodate higher leadcount devices than desirable in PDIP, PLCC, and SOIC packages. As the benefits of the PQFP package configuration were realized within the industry, the design was extended to lower leadcounts.

The PQFP package construction consists of a device attached to the die pad of a leadframe, the circuitry of which is wire bonded to the lead fingers. A plastic epoxy material is injection-molded to encapsulate the device/leadframe configuration. The quad-directional leads are trimmed and formed to a gull-wing formation.

Vantis' PQFP package family includes a wide range of leadcount variations (from 100 to 240). For the most part, the package designs comply with JEDEC and/or EIAJ package versions. Some of the packages are thermally enhanced with either a heat spreader, embedded in the package body; or an exposed heat sink.

Table 6. PQFP (PQR)[1] Package Size Overview

Leadcount	Package Body Area (L X W) Inches SQ. (mm SQ.)	Lead Pitch Inches (mm)	Package Weight (Grams)
100 (PQR)	0.434 (280.0)	0.030 (0.80)	1.66
144 (PQR)	1.215 (784.0)	0.025 (0.65)	5.21, 5.34
160 (PQR)	1.215 (784.0)		5.30
160 (PQE)	1.215 (784.0)		5.37
208 (PQR, PRH)	1.215 (784.0)	0.020 (0.50)	9.53, 9.68
208 (PQE)			10.87
240 (PQE)	1.588 (1024.0)		15.07

Note:

1. *PQR (cavity up) is Vantis' internal abbreviations for metric PQFPs. Thermally ehanced versions are denoted as PRH (cavity up with heat spreaders) and PQE (cavity up with exposed heat sink).*

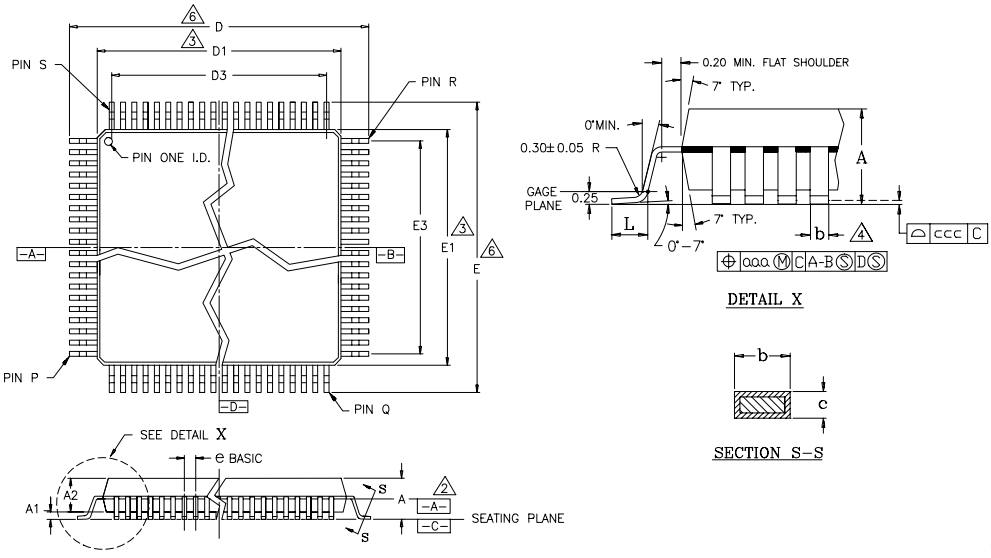

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Figure 5. Rectangular Metric, Cavity-Up Packages (PQR)

	Vantis Package Type & Leadcount	
	PQR, PRH100	
	(MO-108(B)CC-1)	
Dimension Codes	**Min**	**Max**
A	—	3.35
A1	0.25	—
A2	2.70	2.90
b (Note 4)	0.22	0.38
c	0.15	0.23
D (Note 5)	17.00	17.40
D1 (Note 3)	13.90	14.10
D3	12.35 REF	
e (Note 7)	0.65 BASIC	
E (Note 5)	23.00	23.40
E1 (Note 3)	19.90	20.10
E3	18.85 REF	
aaa	0.13 NOM	
ccc	0.10 NOM	
L	0.73	1.03
Lead P	30	
Lead Q	50	
Lead R	80	
Lead S	100	

Notes:

1. *All dimensions are in millimeters, and the dimensions and tolerances conform to ANSI Y14.5M-1982.*
2. *Datum plane —A— is located at the mold parting line and is coincident with the bottom of the lead where the lead exits the plastic body.*
3. *Dimensions "D1 and E1" do not include mold protrusion. Allowable mold protrusion is 0.25 mm per side. (Also see Note 5.)*
4. *Dimension "b" does not include dambar protrusion.*
5. *Dimensions "D1 and E1" do include mold mismatch and are determined at datum plane —A—.*
6. *Dimensions "D and E" are measured from both the innermost and outermost points.*
7. *Deviation from the lead-tip true position shall be within ±0.076 mm for packages having lead pitch >0.5 mm, and within ±0.04 mm when the pitch is ≤0.5 mm.*
8. *Lead coplanarity shall be within 0.10 mm for devices having lead pitch of 0.65—0.80 mm, and 0.076 mm when the lead pitch is 0.50 mm.*
9. *The half span (center of the package to the lead tip) shall be within ±0.0085.*
10. *PQR is Vantis' internal abbreviation for a metric PQFP.*

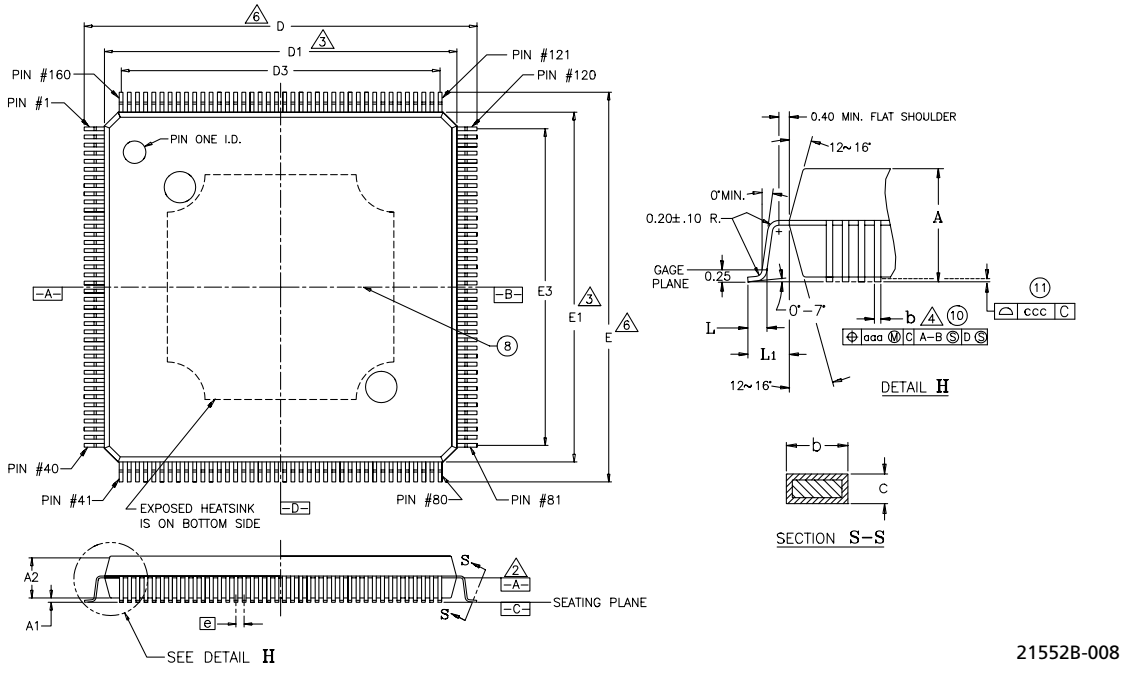

Figure 6. 160-Lead Square Metric, Cavity-Up Package with a Heat Sink (PQE)

Dimension Codes	Vantis Package Type & Leadcount (JEDEC Drawing Number)	
	PQE160 (MS-022(A)/DD-2)	
	Min	Max
A	—	4.00
A1	0.25	0.45
A2	3.25	3.45
b	0.22	0.38
c	0.11	0.17
D, E	30.80	31.60
D1, E1	27.90	28.10
D3, E3	25.35 REF	
e	0.65 BASIC	
L	0.73	1.03
L1	1.60 NOM	
aaa	0.08 NOM	
ccc	0.08 NOM	

Notes:

1. *All dimensions are in millimeters, and the dimensions and tolerances conform to ANSI Y14.5M-1982.*
2. *Datum plane -A- is located at the mold parting line and is coincident with the bottom of the lead where the lead exits the plastic body.*
3. *Dimensions "E1 and D1" do not include mold protrusion. Allowable mold protrusion is 0.25 mm per side. (See also Note 5.)*
4. *Dimension "b" does not include dambar protrusion.*
5. *Dimensions "E1 and D1" do include mold mismatch and are determined at datum plane -A-.*
6. *Dimensions "D and E" are measured from both the outermost points.*
7. *The pin-one ID may be inside the top ejector mark or separate.*
8. *The heatsink center line is aligned to the package body's center line at a tolerance of ±0.30 mm.*
9. *The half span (center of the package to the lead tip) shall be within 15.30 ± 0.165 mm.*
10. *No lead distortion (bent leads, etc.) shall cause deviation from the lead's true position by greater than ±0.04 mm at the maximum of the "b" dimension.*
11. *Lead coplanarity with respect to the seating plan shall not exceed 0.10 mm.*
12. *PQE is Vantis' internal abbreviation for a cavity-up, metric PQFP which has been thermally enhanced with an exposed heat sink.*

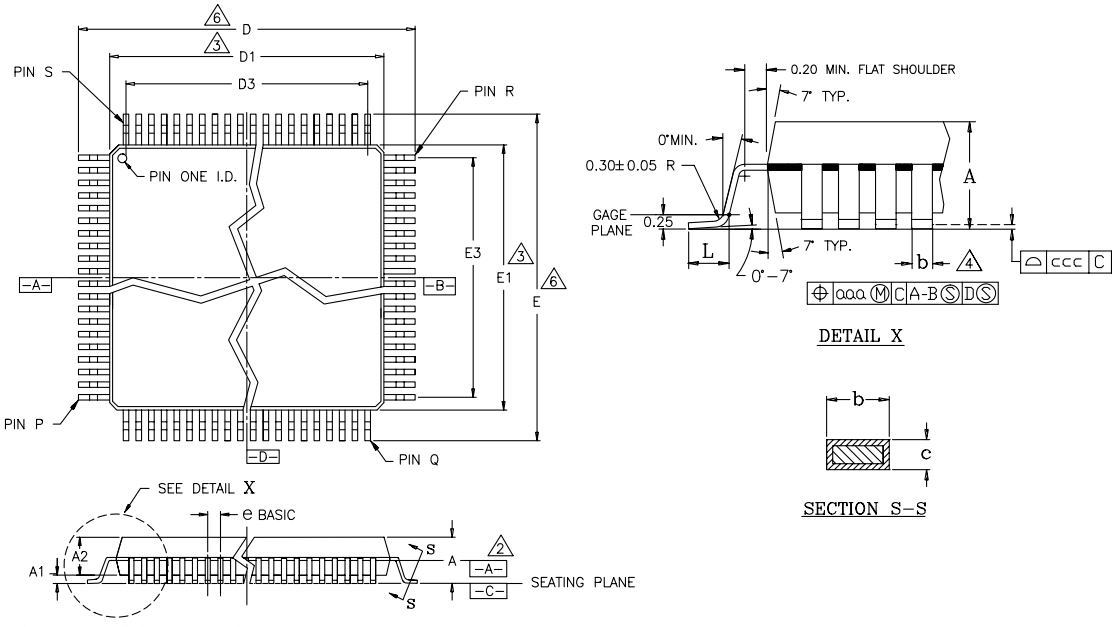

Figure 7. Plastic Quad Flat Pack (PQFP) Packages

Dimension Codes	Vantis Package Type & Leadcount (JEDEC Drawing Number)					
	PQR 144		PQR160		PQR, PRH 208	
	(MO-108(B)DC-1)		(MO-108(B)DD-1)		(MO-143(B)FA-1)	
	Min	Max	Min	Max	Min	Max
A	—	3.95	—	3.95	—	3.95
A1	0.25	—	0.25	—	0.25	—
A2	3.20	3.60	3.20	3.60	3.20	3.60
b (Note 4)	0.22	0.38	0.22	0.38	0.18	0.30
c	0.13	0.23	0.13	0.23	0.13	0.20
D, E (Note 5)	31.00	31.40	31.00	31.40	30.40	30.80
D1, E1 (Note 3)	27.90	28.10	27.90	28.10	27.90	28.10
D3, E3	22.75 REF		25.35 REF		25.50 REF	
e (Note 7)	0.65 BASIC		0.65 BASIC		0.50 BASIC	
aaa	0.13 NOM		0.13 NOM		0.08 NOM	
ccc	0.10		0.10		0.08	
L	0.73	1.03	0.73	1.03	0.50	0.75
Lead P	36		40		52	
Lead Q	72		80		104	
Lead R	108		120		156	
Lead S	144		160		208	

Notes:

1. *All dimensions are in millimeters, and the dimensions and tolerances conform to ANSI Y14.5M-1982.*
2. *Datum plane -A- is located at the mold parting line and is coincident with the bottom of the lead where the lead exits the plastic body.*
3. *Dimensions "D1 and E1" do not include mold protrusion. Allowable mold protrusion is 0.25 mm per side. (Also see Note 5.)*
4. *Dimension "b" does not include dambar protrusion.*
5. *Dimensions "D1 and E1" do include mold mismatch and are determined at datum plane -A-.*
6. *Dimensions "D and E" are measured from both the innermost and outermost points.*
7. *Deviation from the lead-tip true position shall be within ±0.08 mm for packages having lead pitch >0.5 mm, and within ±0.04 mm when the pitch is≤0.5 mm.*
8. *Lead coplanarity shall be within 0.10 mm for devices having lead pitch of 0.65—0.80 mm, and 0.08 mm when the lead pitch is 0.50 mm.*
9. *The half span (center of the package to the lead tip shall be within ±0.0085.*
10. *PQR (cavity up) is Vantis' internal abbreviation for metric PQFPs. Thermally-enhanced PQFPs are denoted by those with heat spreaders embedded in them (PRH for cavity up).*

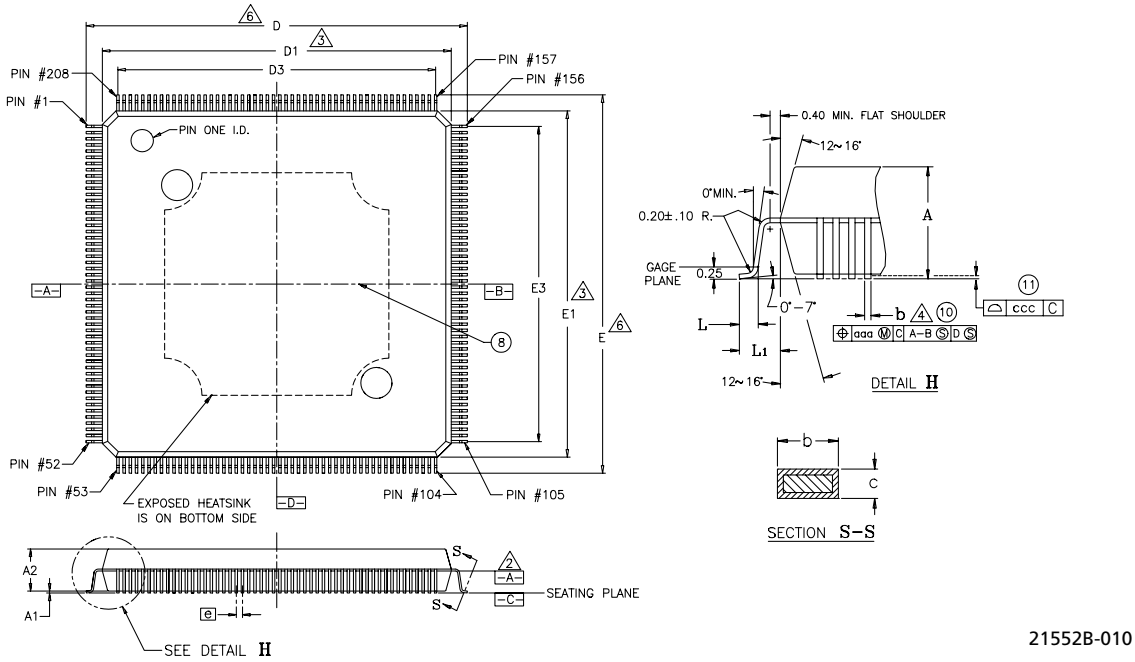

Figure 8. 208-Lead Metric Cavity-Up Package with a Heat Sink (PQE)

Dimension Codes	Vantis Package Type & Leadcount (JEDEC Drawing Number)	
	PQE208 (MO-143(B)FA-1)	
	Min	Max
A	—	3.70
A1	0.25	0.42
A2	3.29	3.45
b	0.17	0.27
c	0.10	0.20
D, E	30.40	30.80
D1, E1	27.90	28.10
D3, E3	25.50 REF	
e	0.50 BASIC	
L	0.50	0.75
L1	1.30 NOM	
aaa	0.08 NOM	
ccc	0.08 NOM	

Notes:

1. *All dimensions are in millimeters, and the dimensions and tolerances conform to ANSI Y14.5M-1982.*
2. *Datum plane -A- is located at the mold parting line and is coincident with the bottom of the lead where the lead exits the plastic body.*
3. *Dimensions "E1 and D1" do not include mold protrusion. Allowable mold protrusion is 0.25 mm per side. (See also Note 5.)*
4. *Dimension "b" does not include dambar protrusion.*
5. *Dimensions "E1 and D1" do include mold mismatch and are determined at datum plane -A-.*
6. *Dimensions "D and E" are measured from both the outermost points.*
7. *The pin-one ID may be inside the top ejector mark or separate.*
8. *The heatsink center line is aligned to the package body's center line at a tolerance of ±0.30 mm.*
9. *The half span (center of the package to the lead tip) shall be within 15.30 ± 0.165 mm.*
10. *No lead distortion (bent leads, etc.) shall cause deviation from the lead's true position by greater than ±0.04 mm at the maximum of the "b" dimension.*
11. *Lead coplanarity with respect to the seating plan shall not exceed 0.08 mm.*
12. *PQE is Vantis' internal abbreviation for a cavity-up, metric PQFP that has been thermally enhanced with an exposed heat sink.*

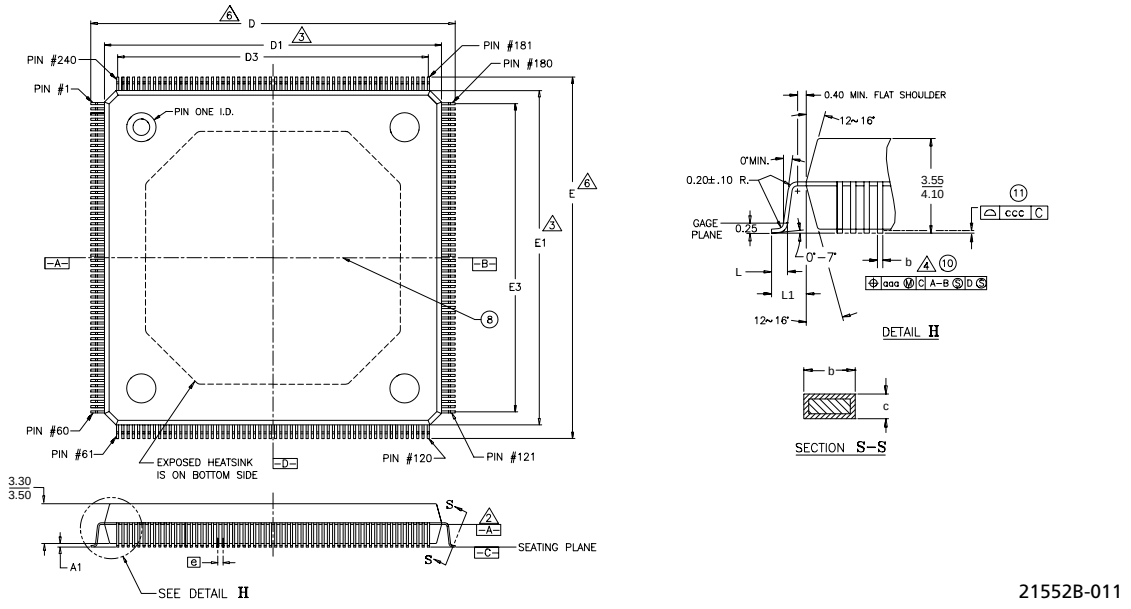

Figure 9. 240-Lead Metric Cavity-Up Package with a Heat Sink (PQE)

Dimension Codes	Vantis Package Type & Leadcount (JEDEC Drawing Number)	
	PQE240 (MO-143(B)/GA)	
	Min	Max
A1	0.25	0.45
b	0.17	0.27
c	0.10	0.20
D, E	34.35	34.85
D1, E1	31.90	32.10
D3, E3	29.50 REF	
e	0.50 BASIC	
L	0.45	0.75
L1	1.30 NOM	
aaa	0.08 NOM	
ccc	0.08 NOM	

Notes:

1. *All dimensions are in millimeters, and the dimensions and tolerances conform to ANSI Y14.5M-1982.*
2. *Datum plane -A- is located at the mold parting line and is coincident with the bottom of the lead where the lead exits the plastic body.*
3. *Dimensions "E1 and D1" do not include mold protrusion. Allowable mold protrusion is 0.25 mm per side. (See also Note 5.)*
4. *Dimension "b" does not include dambar protrusion.*
5. *Dimensions "E1 and D1" do include mold mismatch and are determined at datum plane -A-.*
6. *Dimensions "D and E" are measured from both the outermost points.*
7. *The pin-one ID may be inside the top ejector mark or separate.*
8. *The heatsink center line is aligned to the package body's center line at a tolerance of ±0.30 mm.*
9. *The half span (center of the package to the lead tip) shall be within 15.30 ± 0.165 mm.*
10. *No lead distortion (bent leads, etc.) shall cause deviation from the lead's true position by greater than ±0.04 mm at the maximum of the "b" dimension.*
11. *Lead coplanarity with respect to the seating plan shall not exceed 0.08mm.*
12. *PQE is Vantis' internal abbreviation for a cavity-up, metric PQFP that has been thermally enhanced with an exposed heat sink.*

Thin Quad Flat Pack (TQFP) Packages

The TQFP package is the same basic package design as a PQFP except the package is thinner, and the dimensions governing the solder land pattern are different. The thickness of the package body is 1.0 mm to 1.4 mm, versus the 3.5-mm thickness of a standard PQFP. This is possible because the die is back ground down to a 0.34-mm thickness.

The major applications for TQFP packages are in handheld products, small disk drives, double-sided boards, and PCMCIA cards.

Vantis' family of TQFP packages includes cavity-up versions (denoted internally as PQT and PQL) from 44 to 176 leads.

Table 7. TQFP[1] Package Size Overview

Leadcount	Package Body Area (L X W) Inches Sq. (mm sq.)	Lead Pitch Inches (mm)	Package Body Thickness Inches (mm)	Package Weight (Grams)
44 (PQT)	0.155 (100)	0.03 (0.80)	0.04 (1.00)	0.232
48 (PQL)	0.076 (49)	0.02 (0.5)	0.055 (1.4)	0.17
100 (PQL)	0.304 (196)	0.02 (0.50)	0.055 (1.40)	0.63
144 (PQL)	0.62 (400)	0.02 (0.50)	0.055 (1.40)	1.32
176 (PQL)	0.893 (576)	0.02 (0.50)	0.055 (1.40)	1.82

Note:

1. *PQT is Vantis' internal abbreviation for TQFPs having a package body thickness of 1.0 mm. PQL denotes TQFPs with package body thickness of 1.4 mm.*

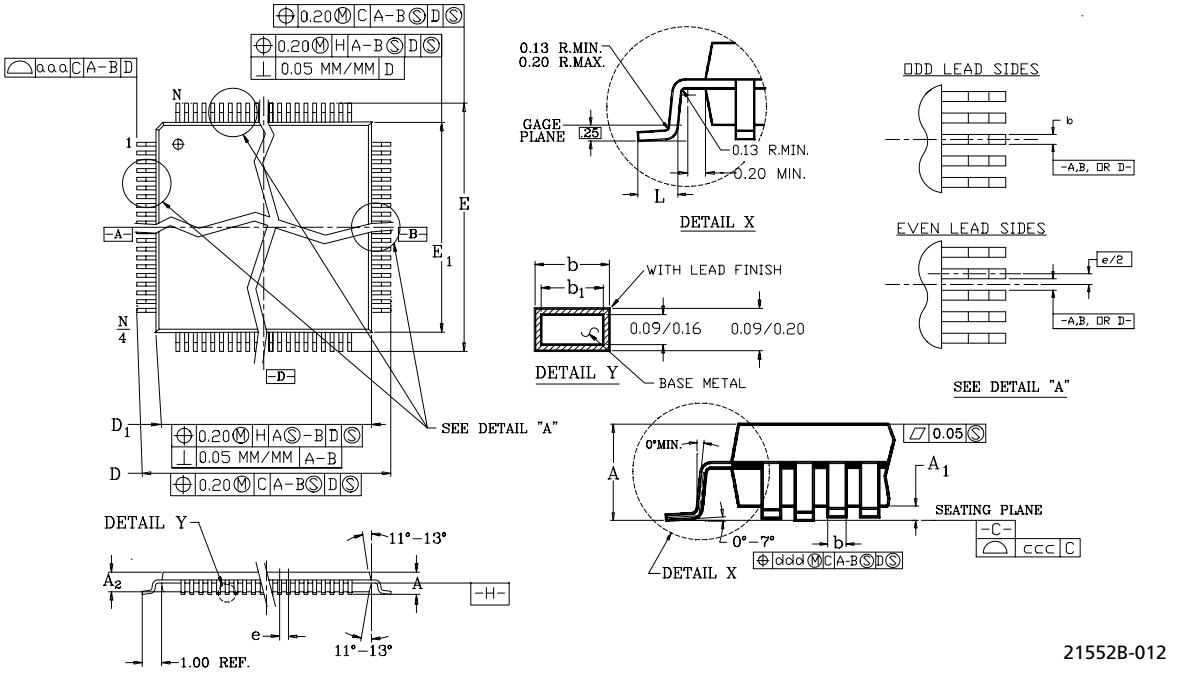

Figure 10. Thin Plastic Quad Flat Pack (TQFP) Packages

Vantis Package Type & Leadcount (JEDEC Drawing Number)										
Dimension Codes	PQT044 (MS-026(A)ACB)		PQL048 (MO-136(B)AE)		PQL100 (MS-026(A)BED)		PQL144 (MS-026(A)BFB)		PQL176 (note 12) (MS-026(A)BGA)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	—	1.20	—	1.60	—	1.60	—	1.60	—	1.60
A1	0.05	0.15	0.05	0.15	0.05	0.15	0.05	0.15	0.05	0.15
A2	0.95	1.05	1.35	1.45	1.35	1.45	1.35	1.45	1.35	1.45
D, E	11.80	12.20	9.00 BASIC		15.80	16.20	21.80	22.20	25.80	26.20
D1, E1	9.80	10.20	7.00 BASIC		13.80	14.20	19.80	20.20	23.80	24.20
L	0.45	0.75	0.45	0.75	0.45	0.75	0.45	0.75	0.45	0.75
N	44		48		100		144		176	
e	0.80 BASIC		0.50 BASIC		0.50 BASIC		0.50 BASIC		0.50 BASIC	
b	0.30	0.45	0.17	0.27	0.17	0.27	0.17	0.27	0.17	0.27
b1	0.30	0.40	0.17	0.23	0.16	0.23	0.17	0.23	0.17	0.23
ccc	—	0.10	—	0.08	—	0.08	—	0.08	—	0.08
ddd	—	0.20	—	0.08	—	0.08	—	0.08	—	0.08
aaa	—	0.20	—	0.20	—	0.20	—	0.20	—	0.20

Notes:

1. *All dimensions are in millimeters, and the dimensions and tolerances conform to ANSI Y14.5M-1982.*
2. *Datum plane -H- is located at the mold parting line and is coincident with the bottom of the lead where the lead exits the plastic body.*
3. *Dimensions "E1 and D1" do not include mold protrusion. Allowable mold protrusion is 0.254 mm per side. (See also Note 5.)*
4. *Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the "b" dimension at maximum material condition. The dambar cannot be located on the lower radius or the foot.*
5. *Dimensions "E1 and D1" do include mold mismatch and are determined at datum plane -H-.*
6. *Dimensions "D and E" are measured from both the innermost and outermost points.*
7. *Deviation from the lead-tip true position shall be within ±0.076 mm for packages having lead pitch >0.5 mm, and within ±0.04 mm when the pitch is ≤0.5 mm.*
8. *Lead coplanarity shall be within 0.10 mm for devices having lead pitch of 0.65—0.80 mm, and 0.08 mm when the lead pitch is 0.50 mm.*
9. *The half span (center of the package to the lead tip) shall be within ±0.16 mm.*
10. *"N" is the total number of terminals.*
11. *The top of the package is smaller than the bottom of the package by 0.15 mm.*
12. *PQT is Vantis' internal abbreviation for a 1.0-mm thick TQFP. PQL designates a 1.4-mm thick TQFP.*

Ball Grid Array (BGA) Packages

The BGA package is a relatively new package design which is gaining popularity as an attractive package solution for Programmable Logic and FPGA devices. It offers a high-density package with a smaller form/fit factor than a comparable leadcount quad flat pack package. More importantly, it is designed with solder balls instead of leads, which are more durable and loosely pitched than the fragile package leads of a comparable surface-mount component. This results in higher board yields.

Package Design

The package consists of a thin Printed Circuit Board (PCB) made of a BT epoxy laminate, double-sided, and overlaid with copper over which metallized wire bond pads and a die pad are fabricated. The wirebond pads extend outward to plated through-hole vias located around the board's periphery. These vias provide the electrical continuity from the top of the board to the other side where copper traces run from the holes to a matrix of solder bumps. The bumps are soldered onto a land pattern on a circuit board in the end-use application. A solder mask is photo defined on the backside of the package to contain the flow of solder during board assembly.

The die is attached to the die pad using a standard epoxy die attach method. Gold ball bonding is used to connect the die pads to the wire bond pads, and the die is encapsulated with epoxy encapsulation material to protect it.

Table 8. BGA Package Size Overview

Ball Count	Package Body Area (L X W) Inches Sq. (mm sq.)	Ball Pitch Inches (mm)	Package Weight (Grams)
256 (BGD) (Note 1)	1.13 (729.0)	0.05 (1.27)	4.23
352 (BGD) (Note 1)	1.90 (1225.0)		6.99

Note:

1. BGD is Vantis' internal abbreviation for a wirebonded, cavity-down, ball grid array, thermally enhanced with a heat slug

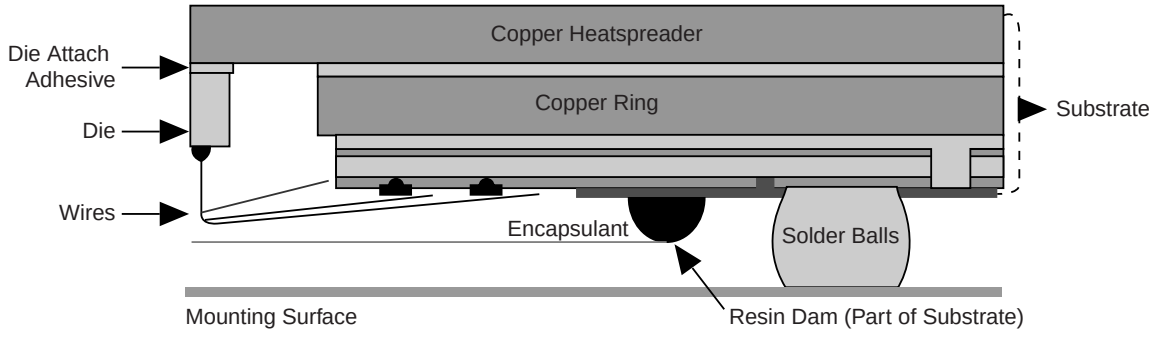

Figure 11. BGD Cross-section

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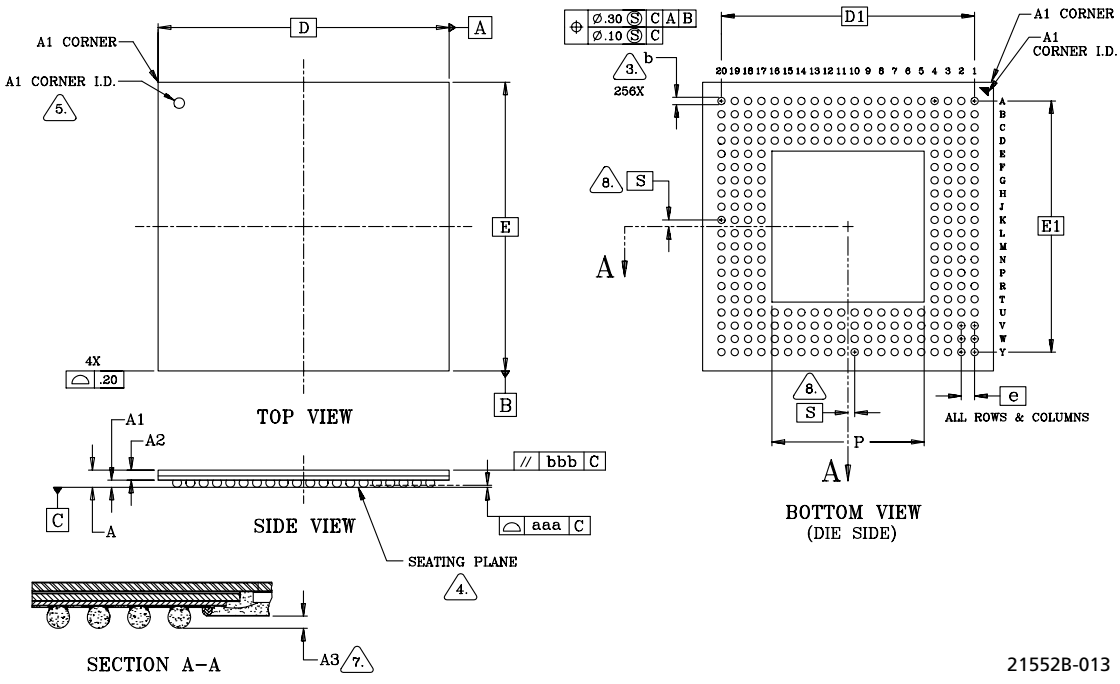

Figure 12. 256-Ball (27 x 27) Cavity-Down Package (BGD)

Dimension Codes	Vantis Package Type & Leadcount (JEDEC Drawing Number) BGD256 (MO-151(B)/BAL-2)[1] Min	Max	Note
A	1.10	1.65	overall thickness
A1	0.50	0.70	ball height
A2	0.60	0.95	body thickness
A3 (Note 7)	0.15	0.45	seating plane clearance
D, E	27.00 BASIC		body size
D1, E1	24.13 BASIC		ball footprint
M	20 x 20		ball matrix size
N	256		total ball count
MR (Note 6)	4		number of rows deep
e	1.27 BASIC		ball pitch
b	0.60	0.90	ball diameter
P	14.8	15.2	encapsulation area
S	0.635 BASIC		solder ball placement

Note:

1. *BGD is Vantis' internal abbreviation for a wirebonded, plastic, cavity-down ball grid array that has been thermally enhanced with a heat sink.*

Geometric Tolerances		
aaa	0.15	coplanarity
bbb	0.15	parallelism

Notes:

1. *All dimensions are in millimeters.*
2. *Dimensioning and tolerancing conform to ASME Y14.5M—1994.*
3. *Dimension "b" is measured at the maximum solder ball diameter on a plane parallel to datum C.*
4. *Datum C and the seating plane are defined by the spherical crowns of the solder balls.*
5. *A1 corner I.D. is marked with ink.*
6. *Refers to the number of peripheral rows or columns.*
7. *Refers to the height from the encapsulation to the seating plane.*
8. *"S" is measured with respect to datums A and B and defines the position of the solder balls nearest the package centerlines. When there is an odd number of solder balls in the outer row "S" = 0.000; when there is an even number of solder balls in the outer row the value "S" =e/2.*

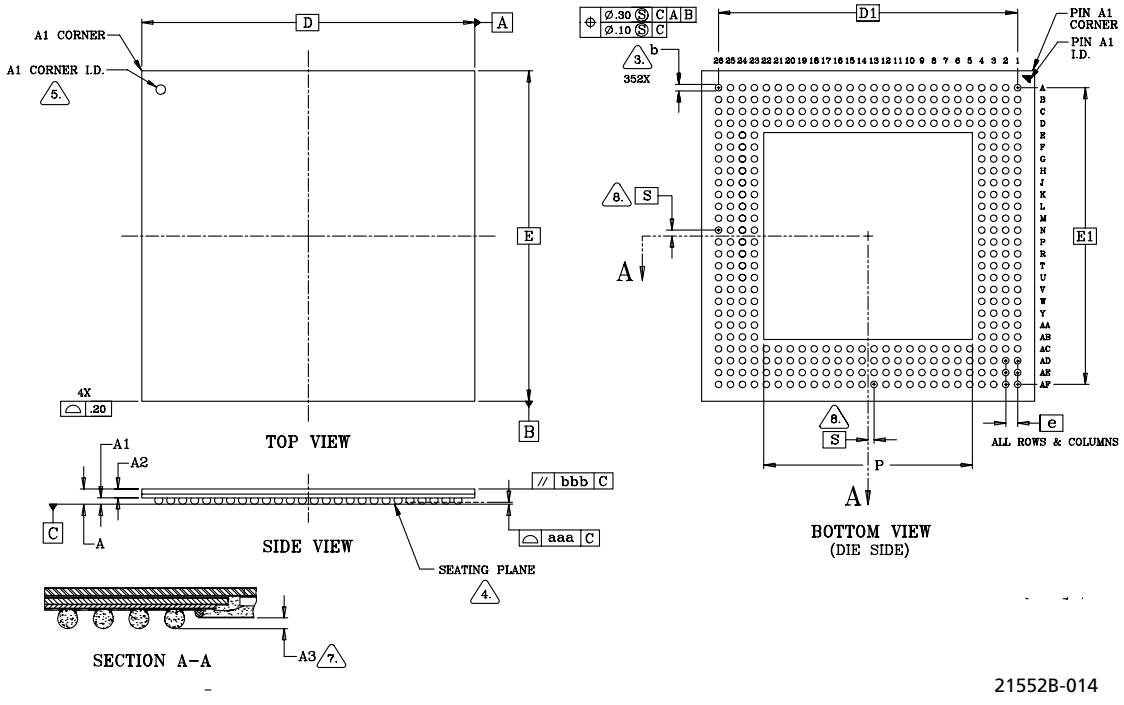

Figure 13. 352-Ball (35 x 35) Cavity-Down Package (BGD)

Dimension Codes	Vantis Package Type & Leadcount (JEDEC Drawing Number) BGD352 (MO-151(B)/BAR-2)		
	Min	Max	Note
A	1.10	1.65	overall thickness
A1	0.50	0.70	ball height
A2	0.60	0.95	body thickness
A3 (Note 7)	0.15	0.45	seating plane clearance
D, E	35.00 BASIC		body size
D1, E1	31.75 BASIC		ball footprint
M	26 x 26		ball matrix size
N	352		total ball count
MR (Note 6)	4		number of rows deep
e	1.27 BASIC		ball pitch
b	0.60	0.90	ball diameter
P	20.4	21.2	encapsulation area
S	0.635 BASIC		solder ball placement

Geometric Tolerances		
aaa	0.15	coplanarity
bbb	0.15	parallelism

Notes:

1. *All dimensions are in millimeters.*
2. *Dimensioning and tolerancing conform to ASME Y14.5M—1994.*
3. *Dimension "b" is measured at the maximum solder ball diameter on a plane parallel to datum C.*
4. *Datum C and the seating plane are defined by the spherical crowns of the solder balls.*
5. *A1 corner I.D. marked by ink.*
6. *Refers to the number of peripheral rows or columns.*
7. *Refers to the height from the encapsulation to the seating plane.*
8. *"S" is measured with respect to datums A and B and defines the position of the solder balls nearest the package centerlines. When there is an odd number of solder balls in the outer row "S" = 0.000; when there is an even number of solder balls in the outer row the value "S" =e/2.*
9. *BGD is Vantis' internal package abbreviation for a wirebonded, plastic, cavity-up package.*

Plastic Dual-In-Line Packages (PDIP)

The Plastic Dual-In-Line package (PDIP) construction consists of a device attached to the die pad of a leadframe, the circuitry of which is wire bonded to the lead fingers. A plastic epoxy material is injection-molded to encapsulate the device/leadframe configuration. The leads are trimmed and formed to a through-hole lead design, with lead extensions along the two long ends of the rectangular package.

Table 9. PDIP (PD) Package Size Overview

Leadcount	Package Body Area (L X W) Inches	Lead Pitch Inches	Package Weight (Grams)
20	0.267	0.10	1.39
24	0.69		3.55
24 (PD3 (Note 1))	0.32		1.60
28	0.81		4.20

Note:

1. PD3 (300 mil) designate PDIP designs for which the package mil size is not what is standard for that lead count.

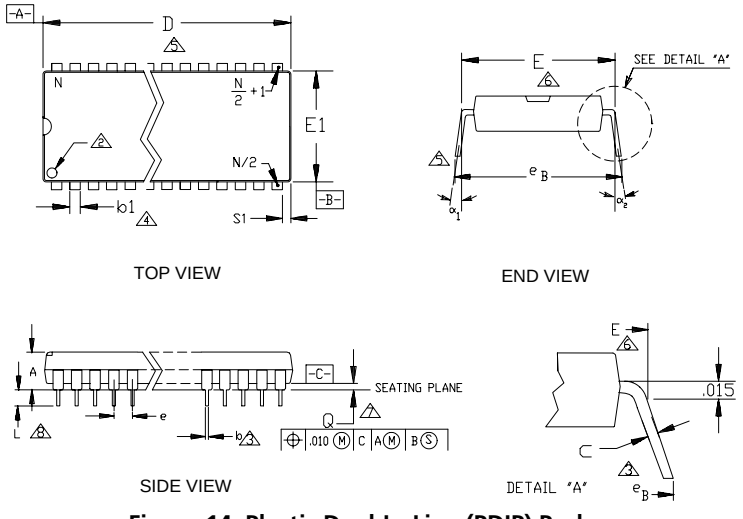

Figure 14. Plastic Dual-In-Line (PDIP) Packages

Dimension Codes	Vantis Package Type & Leadcount (JEDEC Drawing Number)									
	PD 020		PD 024		PD3024		PD 028		PD3028 (288 body)	
	(MS-001(D)AD)		(MS-011(B)AA)		(MS-011(B)AA)		(MS-011(B)AB)		(MO-095(A)AH)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.140	0.200	0.140	0.225	0.140	0.200	0.140	0.225	0.140	0.180
b	0.014	0.022	0.014	0.022	0.014	0.022	0.014	0.022	0.014	0.022
b1	0.045	0.065	0.045	0.065	0.045	0.065	0.45	0.65	0.45	0.60
C	0.008	0.015	0.008	0.015	0.008	0.015	0.008	0.015	0.008	0.015
D	1.010	1.040	1.240	1.280	1.150	1.270	1.440	1.480	1.345	1.385
E1	0.240	0.280	0.520	0.580	0.240	0.280	0.530	0.580	0.275	0.295
E	0.300	0.325	0.600	0.625	0.300	0.325	0.600	0.625	0.300	0.325
e	0.090	0.110	0.120	0.160	0.120	0.160	0.090	0.110	0.090	0.110
L	0.120	0.160	0.090	0.110	0.090	0.110	0.120	0.160	0.120	0.150
Q	0.015	0.060	0.015	0.060	0.015	0.060	0.015	0.060	0.015	0.060
S1	0.005	—	0.005	—	0.005	—	0.005	—	0.005	—
e_b	0.330	0.430	0.630	0.700	0.330	0.430	0.630	0.700	0.330	0.430
$(\alpha_1 - \alpha_2)$	0°	10°	0°	10°	0°	10°	0°	10°	0°	10°
(α_1, α_2)	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°
N	20		24		24		28		28	

Notes:

1. *All dimensions are in inches.*
2. *A notch, tab, or pin one identification mark shall be located adjacent to the device pin one.*
3. *Lead thickness increases by a maximum of 0.003 inch when a the solder lead finish is applied.*
4. *These dimensions do not include mold flash or protrusion.*
5. *This dimension is measured from the outside of the leads and 0.015 inch below the plane of the package exit, as defined by the top of the lead.*
6. *This dimension is measured from the seating plane to the base plane.*
7. *This dimension is measured from the seating plane (or from the lowest point of the lead shoulder width that measures 0.040 inch) to the lead tip.*
8. *The difference between these two dimensions should not exceed 7°.*
9. *When standoff has radii, the seating plane location is defined where the lead width equals 0.040 inch.*
10. *PD is Vantis' internal designator for a plastic dual-in-line package.*

Small Outline (SOIC) Plastic Packages

The SOIC package is an surface-mount alternative for low leadcount devices. Its design is similar to the conventional Dual-In-Line (DIP) package—an attractive feature for circuit designers already familiar with DIPs and memory boards.

Like plastic DIPs, the SOIC package consists of a device attached to the die pad of a leadframe, the circuitry of which is wire bonded to the lead fingers. A plastic epoxy material is injection-molded to encapsulate the device/leadframe configuration. The leads extending from the two long sides of the rectangular package body are trimmed and formed to a gull-wing formation.

The 50-mil lead pitch of SOIC packages allows for considerable reduction in package size over comparable DIPs, as shown in the table to the right. Not only are SOIC packages smaller, they are lighter, too. This makes them ideal for foil/film mounting and virtually all automated board assembly operations.

Table 10. SOIC (SO)[1] Package Size Overview

Leadcount	Package Body Area (L X W) Inches Sq. (mm sq.)	Lead Pitch Inches (mm)	Package Weight (Grams)
20	0.149 (96.13)	0.05 (1.27)	0.51
24	0.180 (115.51)		0.62

Note:

1. SO is Vantis' internal abbreviation for an SOIC package.

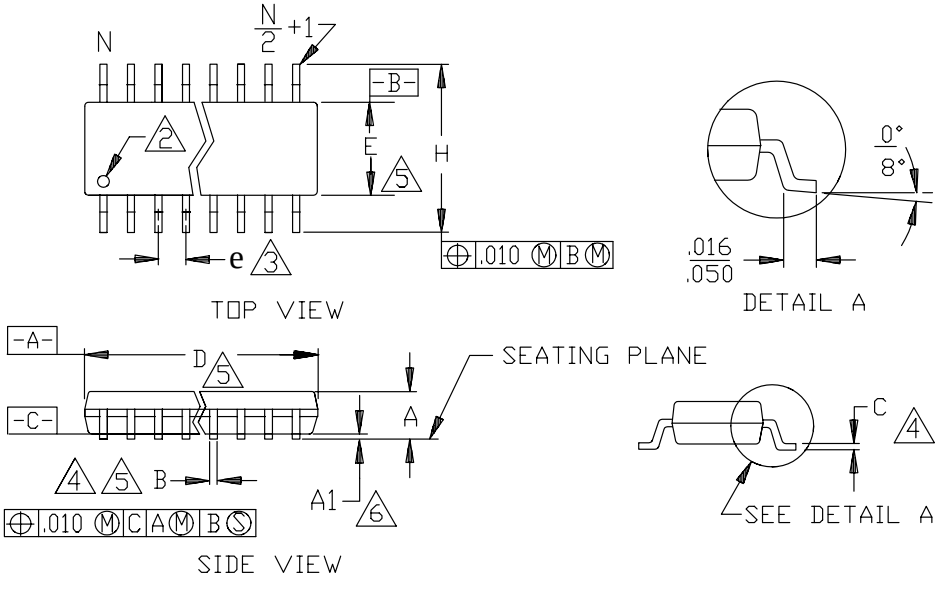

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Figure 15. JEDEC English Packages

Dimension Codes	Vantis Package Type & Leadcount			
	SO 20		SO 24	
	Min	Max	Min	Max
A	0.0926	0.1043	0.0926	0.1043
A1	0.0040	0.0118	0.0040	0.0118
B	0.0138	0.0192	0.0138	0.0192
C	0.0091	0.0125	0.0091	0.0125
D	0.4961	0.5118	0.5985	0.6141
e	0.050 BASIC		0.050 BASIC	
E	0.2914	0.2992	0.2914	0.2992
H	0.3940	0.4190	0.3940	0.4190
N	20		24	

Notes:

1. *All dimensions are in inches.*
2. *An identification mark shall be located adjacent to the device pin one.*
3. *Dimension "e" is measured at the center line of the leads.*
4. *Dimensions "B" and "C" increase by 0.003 inch maximum for all leads when solder dip lead finish is applied.*
5. *Dimension "B" does not include dambar protrusion. Allowable protrusion is 0.004 inch.*
6. *Dimensions "A1" is measured from the base plane of contact, which is made when the packaged is allowed to rest freely on a flat, horizontal surface.*
7. *Lead coplanarity shall be within 0.004 inch as measured from the seating plane.*
8. *SO is Vantis' internal abbreviation for an SOIC package.*

PACKAGE DESIGN ADVANTAGES

The BGA package design offers many advantages over other high leadcount packages.

Board Real Estate Savings

Because of the small package size, the BGA offers significant savings in board real estate, occupying about 51 percent of the space a comparable QFP requires. It has a lower profile, too, about one third as thick as a plastic quad flat pack (PQFP) package.

Electrical Performance

The BGA offers superior electrical performance because the shorter wirebond lengths in it help reduce inductance. Comparing a 169-ball BGA to a 160-Pin PQFP, the BGA shows a 31 percent reduction in signal capacitance and a 46 percent reduction in signal time delay.

Thermal Performance

Studies have been conducted that show that the BGA thermally outshines a comparable PQFP when it is fabricated with "thermal vias" (i.e., through-hole vias) underneath the die pad. These vias allow heat generated by the device to flow to the board, which would improve thermal performance provided the board has a conducting plane built into it. To more accurately ascertain the thermal performance of a BGA, the specific end-use application environment needs to be considered.

Board Assembly Advantages

The pitch of the solder balls on a BGA is far more manageable during board assembly, at 1.0 to 1.5 mm, than the typical 0.5-mm pitch of high leadcount Quad Flat Packs (QFPs).

BGAs can be handled with the same pick-and-place equipment that is used for conventional surface-mount devices, including solder reflow methods. During reflow assembly, the wetting action of the solder balls tends to pull them into alignment so that placement of the component on the solder land does not need to be nearly as precise as with a QFP. The alignment can be off by as much as 6 mils—more forgiving than the 3 mils (0.076 mm) required for fine lead-pitch QFPs.

Post Assembly Inspections

Once the BGA is mounted on the board, there is the challenge of how to inspect the ball joints. Thus far, x-ray techniques appear the most viable solution, although these systems can be quite expensive. Once the component is mounted, it can be removed and a new component remounted; however, there is currently no process for reworking the removed component for reuse.

Vantis' Development Plans

Vantis is currently shipping BGA packages with body sizes of 27 mm x 27 mm and 35 mm x 35 mm at 1.27 mm ball pitch. Vantis will continue to develop other enhanced BGA packages with smaller ball pitches, better thermal performance and higher ball counts with smaller body sizes for our future products.

THERMAL CHARACTERIZATION OF PACKAGES

With the increased density and complexity of CMOS VLSI semiconductor devices, the need to accurately evaluate the thermal properties of packaged Integrated Circuits (ICs) is fundamental to the understanding and prediction of device reliability and performance. Failure rates are inseparably tied to the operating temperature of the device, and they increase exponentially as the temperature of the device junction rises. Therefore, it is important that the junction temperature of every IC in the system be controlled to attain high reliability and a long operating life. Likewise, understanding the thermal properties of each component in the system is important for addressing overall thermal concerns at the system level given the end-use application environment.

Thermal performance data is usually measured in the form of thermal resistance or thermal impedance characteristics ($R\theta_{JA}$, θ_{JA}), and it is used to estimate the junction temperature of a device operating in a given environment. A certain amount of caution should be exercised, however, when using thermal data to design or evaluate systems because many factors influence the thermal performance of the chip-package combination. These factors include such phenomenon as the ambient temperature, the power dissipation of the chip, the thermal conductivity of the Printed Circuit Board (PCB), the proximity and power dissipation of neighboring devices, and the airflow through the system. Therefore, it is important to carefully evaluate and analyze the entire system and its environment before utilizing any standard thermal data. Vantis reports data using the JEDEC JESD51 specification format so that the end user can approximate the effect of the application environment.

The following sections detail the methodology and techniques used by Vantis to evaluate the thermal performance of our devices, with an emphasis on fundamental heat flow properties. Our methods comply with established standards, both government and commercial, and we meet or exceed all military specifications for testing and reporting data. Our thermal data is collected for still air, moving air, and isothermal case temperature, using measurement techniques that are in conformance with MIL-SPEC 883D, Method 1012.1 specifications. We also adhere to the recently published improved standards for the thermal test method, environmental considerations, and mounting surface specification. These were published by the Engineering Industries Association (EIA) and Joint Electronic Devices Engineering Council (JEDEC), and they are documented in the JESD51 series.

At Vantis, we are committed to providing current and relevant thermal information for every product we manufacture. In our state-of-the art thermal characterization facility, we can evaluate the thermal performance of any Vantis product. Customers interested in product-specific thermal data should contact a Vantis sales representative.

TERMINOLOGY

The most common terminology used in the industry for specifying thermal performance is the θ_{JA} term and related forms. These are used to describe the thermal characteristics of semiconductor devices in various environments such as natural or forced convection. They are also used when simulating an infinite heat sink as in junction-to-case measurements. In addition, a new term has been recently defined to meet the needs of end users of plastic surface-mount packages. Denoted as Ψ_{JT} this measurement will allow a case temperature measurement during thermal test, which can then relate the case temperature in a free convection boundary condition to the junction temperature. The Ψ_{JT} parameter also helps to validate junction temperature measurements and calculations during thermal characterization.

The terminology commonly used to specify thermal performance, and mathematical constructs for calculating thermal resistance parameters, are provided in the following pages.

MEASUREMENT METHODS

Vantis uses two primary test methods to evaluate the thermal resistance of packaged ICs: the live device method and the thermal test die method. In both methods, we utilize a heat source that is mounted within the package. For the live device method, it is a thermal test chip.

Thermal Resistance Terminology

θ_{JA}, $R\theta_{JA}$ = Thermal resistance from junction to ambient: resistance from the operating portion of a semiconductor device to a natural convection (still air) environment; °C/W.

θ_{JMA}, $R\theta_{JA}$ = Thermal resistance from junction to moving air: resistance from the operating portion of a semiconductor device to a forced convection (moving gas) environment surrounding the device; the gas is assumed to be air unless stated otherwise; °C/W.

θ_{JC}, $R\theta_{JC}$ = Thermal resistance from junction to case: resistance from the operating portion of a semiconductor device to the outside surface of the package (case) closest to the chip mounting area when that same surface is properly heat sunk so as to minimize temperature variation across the surface; °C/W.

θ_{JR}, $R\theta_{JR}$ = Thermal resistance from junction to reference point: resistance from the operating portion of a semiconductor device to a defined reference point within the specified environment surrounding the device; °C/W.

θ_{JX}, $R\theta_{JX}$ = Thermal resistance from junction to environment: resistance from the operating portion of a semiconductor device to a defined non-standard environment surrounding the device; °C/W.

θ_{JL}, $R\theta_{JL}$ = Thermal resistance from the operating portion of a semiconductor device to a liquid environment surrounding the device; °C/W.

θ_{CA}, $R\theta_{CA}$ = Thermal resistance from specified reference location on the case of a semiconductor device to an ambient environment surrounding the device; °C/W.

Ψ_{JT} = Thermal characterization parameter from device junction to the top center of the package surface; °C/W.

T_J = Junction temperature; °C.

T_A = Ambient temperature; °C.

T_C = Case temperature; °C.

T_R = Reference temperature; °C, to standard environment.

T_X = Reference temperature; °C, to non-standard environment.

P_H = Device power dissipation, steady state; Watts.

I_{CC} = Device current supply; Amperes.

V_{CC} = Device voltage supply; Volts.

P_D = Device power dissipation in watts (V_{CC} x I_{CC}).

K_F = Kfactor; calibration constant for determining the $\Delta T/\Delta V$ relationship of the Thermally Sensitive Device (TSD); °C/mV.

TSD = Thermally sensitive device: usually a semiconductor junction which exhibits a linear relationship to temperature over a given temperature range with a constant current applied; °C/mV.

Note: θ_{JR} is an alternative symbol for $R\theta_{JR}$.

continued

Sample Calculations: Thermal Resistance

1) For calibration of a Thermally Sensitive Device (TSD):

$$K_F = \frac{T_{HI} - T_{LO}}{V_{LO} - V_{HI}} \quad (1)$$

where:

T_{HI} = High calibration temperature
T_{LO} = Low calibration temperature
V_{HI} = High TSD voltage
V_{LO} = Low TSD voltage

Note: This measurement is made at three or more temperatures to validate linearity of the TSD.

2) For calculating thermal resistance:

$$\theta_{JR} = \frac{T_J - T_R}{P_H} \quad (2)$$

where:

θ_{JR} is the thermal resistance from junction to some specified reference point for:

θ_{JA}: 2.54 mm below and 150 mm to the side of the device under test (see Figure 8.1)
θ_{JMA}: directly upstream from the device under test (see Figure 8.3).
θ_{JC}: side of the package directly adjacent to the backside of the die.

3) **For calculating the relationship between θ_{JA}, θ_{JC}, and θ_{CA}:**

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (3)$$

4) **For calculating junction temperature:**

$$T_J = T_R + (\theta_{JR} \times P_D) \quad (4)$$

where:

T_R is the temperature at some specified reference point.

θ_{JR} is the thermal resistance to some specified reference point, R, ^{0}C/W.

5) **Thermal characterization parameter, Ψ_{JT}, calculation:**

$$\Psi_{JT} = \frac{T_{JSS} - T_{TSS}}{P_H} \quad (5)$$

where:

Ψ_{JT} = Thermal characterization parameter from top surface of package to air.
T_{JSS} = Device junction temperature at steady-state power.
T_{TSS} = The package top surface, at steady-state power, measured by a thermocouple, infrared sensor, or fluoroptic sensor.

6) **Thermal characterization parameter, Ψ_{TA}, calculation:**

$$\Psi_{TA} = \frac{T_{TSS} - T_{ASS}}{P_H} \quad (6)$$

where:

Ψ_{TA} = Thermal characterization parameter from top surface of package to air.
T_{TSS} = Package (top surface) temperature at steady-state power.
T_{ASS} = The ambient temperature at steady-state power.

7) **For calculating the relationship between θ_{JA} and Ψ_{JT}:**

$$\theta_{JA} = \Psi_{JT} + \Psi_{TA} \quad (7)$$

Table 11. Typical Thermal Resistance Data (T_A=25°C. These Parameters are not Tested.)

Package Style	θ_{JC}[1] °C/W (Typ)	ψ_{JT}[2] °C/W (Typ)	θ_{Ja}[3] °C/W (Typ)	θ_{Jma} °C/W 200 lfpm (Typ)	θ_{Jma} °C/W 400 lfpm (Typ)	θ_{Jma} °C/W 600 lfpm (Typ)	θ_{Jma} °C/W 800 lfpm (Typ)
PL44		10.9	31.4	26.5	25	24.2	23.6
PL68		10	33	29.4	26.8	25.0	22.3
PL84		7.8	28.3	22.5	21.4	20.4	19.5
PLH84		3.2	15.9	13.2	11.5	9.7	8.8
PQE160	0.9	1.7	12.9	7.8	6.5	5.6	5
PQE208	0.9	1.9	11.6	6.4	5.2	4.6	4
PQE240	0.8	1.3	11.5	6.3	5.4	4.4	4.1
PQL48		4.7	32.5	26.4	24.8	22.8	21.8
PQL100		4.6	28.7	25.1	23.2	21.8	20.7
PQL144		6.4	29.5	26.1	24.9	23.3	22.2
PQR100		18.9	34.5	30.3	27.6	26	24.8
PQR144		13	32.1	22.1	18.5	18.2	17
PQR160		13.5	29.5	25.1	23.3	22	21.1
PQR208		17	51.4	46.6	44.4	42.8	41.7
PQT44		11.3	41	35	33.7	32.6	32
PRH144		5.1	19.5	16.4	14.1	12.5	11.7
PRH208		4.5	16.1	12.4	11.6	10.3	9.5
BGD256	1.2	2.9	14.5	11.7	10.7	9.8	9.1
BGD352	1	2.8	12.6	10.1	9.2	8.4	7.8

Notes:

1. *θ_{jc} is only valid for packages with direct thermal pathways to the surface of the package and should only be used to calculate junction temperature if a heat sink is applied.*
2. *ψ_{JT} is a thermal parameter allowing the calculation of junction temperature from a measured temperature at the top center of the package in natural convection. See JESD 51-2 for details (www.jedec.org/free standards)*
3. *All thermal data was generated according to EIA/JEDEC specifications JESD51 series. All measured packages were surface mounted on to 2S2P (2 signal, 2 internal Cu plane) boards.*

Plastic θ_{jc} Considerations

The data listed for plastic θ_{jc} are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θ_{jc} measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θ_{jc} tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

The live device method provides weighted average values for thermal resistance, and it can account for any hot spots or uneven temperature distributions on the die. The thermal test die method is preferred, however, because it enables the power dissipation and die size to be easily controlled. The following sections provide details on these two methods and the calibration process that is required.

CALIBRATION OF THE THERMALLY SENSITIVE DEVICE

When utilizing either the live device method or the thermal test die method, the Thermally Sensitive Device (TSD) must first be calibrated to determine the $\Delta T/\Delta V$ characteristics (i.e., the change in temperature over the change in voltage). (The TSD appropriate for each test method is defined in the sections that follow.)

The calibration factor (KF) for the TSD is used to relate the forward voltage of the TSD to a temperature, thereby allowing thermal resistance to be computed using the algorithm (1) provided under "Sample Calculations." The devices under test are calibrated over the temperature range of interest in either a convection type oven or a temperature controlled fluid bath.

Live Device Method

When measuring the thermal characteristics of a live semiconductor device, the device must first be biased to provide the typical power dissipation for that device type. Also, a TSD must be located on the die to enable the junction temperature to be measured and monitored. The most commonly used TSD is either the substrate isolation diodes or an ESD input protection diode. Substrate diodes are preferred because using an input diode for temperature sensing only gives the temperature information for a small region of the die. Substrate isolation diodes, on the other hand, provide an array of the intrinsic parasitic diodes inherent in many semiconductor processes.

To implement the electrical test method for a live device, the device must first be forward biased as it is in normal operation and allowed to dissipate power. Then it must be reverse biased and, at specified intervals (usually within 10 to 40 µs from the time power was removed), the TSD must be measured to determine the junction temperature. This is also referred to as the voltage-drop method or the pulse method. The parameter actually measured is the forward voltage drop of a semiconductor junction. The substrate isolation diodes are also electrically in parallel, so the junction temperature recorded is the weighted average of the hottest junction on the die, providing typical worst case values. Unfortunately, due to the increasing complexity of the silicon, the live device method is less popular and not widely used for high pin-count products. Biasing the die with the correct vectors and signals while switching from the forward- to reverse-bias modes is becoming more difficult, and in some cases impossible.

Thermal Test Die Method

When using the thermal test die method, a specially designed thermal test die is assembled into the IC package. This test die contains a resistive element for power dissipation. Semiconductor junctions (i.e., diodes) are used as TSD to enable the temperatures at various locations on the die to be measured. This method is used primarily to evaluate the thermal resistances of packages, generically, given the range of die sizes appropriate for the module size of the thermal test die (usually 75 to 100 mils^2). These modules can be arrayed to produce larger die sizes in increments of the unit module (i.e., 100 mils^2, 200 mils^2, etc.).

The thermal test die method is limited, however, in that it assumes evenly distributed power dissipation across the surface of the die. This typically produces a near-ideal heat source and lower thermal resistance results. Therefore, the die size and temperature distribution of the actual (production) device should be taken in to account when making these types of measurements. The temperature distribution of the production device can be determined by the use of non-contact thermometry methods such as liquid crystal thermography or infrared thermometry. The temperature distribution, assuming typical operating conditions, can then be computed based on

evidence of hot spots and the resulting temperature distribution across the die. Based on this analysis, the thermal properties of the production device can be correlated with those obtained with the thermal test die.

MEASUREMENT ENVIRONMENTS

When using thermal performance data for semiconductor devices, it is extremely important to consider the effects of the environment on the measured or modeled values. To simulate the environments devices will encounter in end-use applications, thermal measurements are taken in still and moving air environments and at the case (or package body) environment, as explained in the following sections.

Natural Convection (Still-Air) Environment

Natural convection measurements (θ_{JA}) are performed in a chamber which encloses one cubic-foot volume of still air. A diagram of a still-air chamber is shown in Figures 16 and 17. The test board near the device under test is mounted horizontally (or vertically, if requested) in the chamber, and the reference temperatures both inside and outside the chamber are monitored. The device is allowed to come to a steady state thermal condition both before and after heating power is applied.

Forced Convection (Moving-Air) Environment.

Forced convection (θ_{JMA})measurements are performed in a laboratory wind tunnel, a diagram of which is shown in Figure 18. The test boards can be mounted vertically or horizontally, depending on the requirement.

Air speeds of 100 to 1200 linear feet per minute (lfpm) are attainable in the tunnel. Air speed is monitored using a hot-wire anemometer, which is mounted on an XYZ stage near the device.

Case Environment

When taking case (θ_{JC}) measurements, a separate apparatus is required for hermetic versus plastic packages.

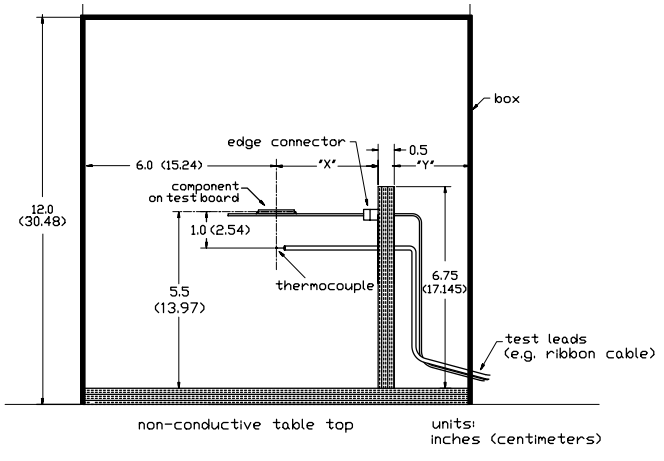

Figure 16. Side View of the Natural Convection Fixture, Which is Used for Still-Air Tests

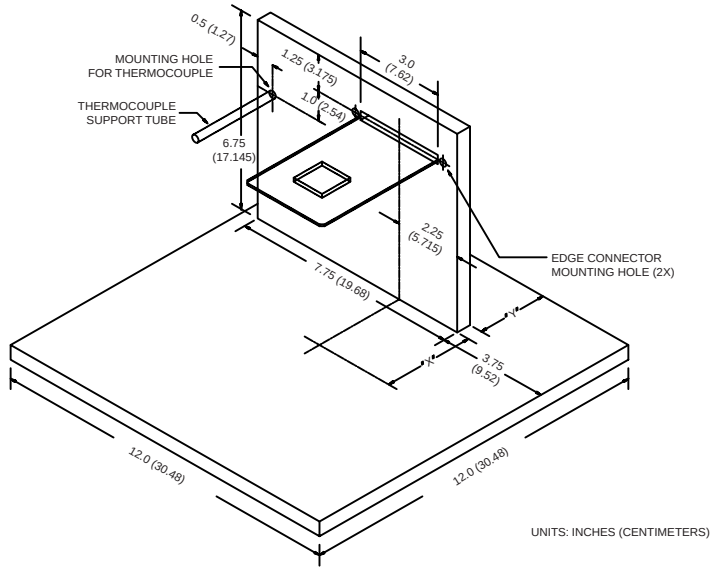

Figure 17. Isometric View of the Natural Convection Fixture

For hermetic packages, a thermoelectric device or cold plate is used to keep the case temperature constant during the measurement process. The package is placed against the cold plate and held in position with an adjustable clamp. A thin layer of thermal grease is used to thermally contact the package to the test fixture. A thermocouple is mounted into the test fixture that comes in contact with the package body to allow case temperature measurements. Fixtures for junction-to-case measurements are customized for each package style.

For plastic packages, a temperature-controlled fluid bath containing deionized water is used. Fluid is forced onto the package body from both sides from nozzles as shown in Figure 19. Due to the high heat transfer capabilities of this method, we assume the reference temperature is that of the liquid. This measurement is a relatively new technique that essentially provides the same boundary conditions as the cold plate method does for hermetic packages. But, caution should be used when attempting to calculate junction temperature from θ_{JC} values for plastic packages in end-use environments (see the following section on Ψ_{JT}).

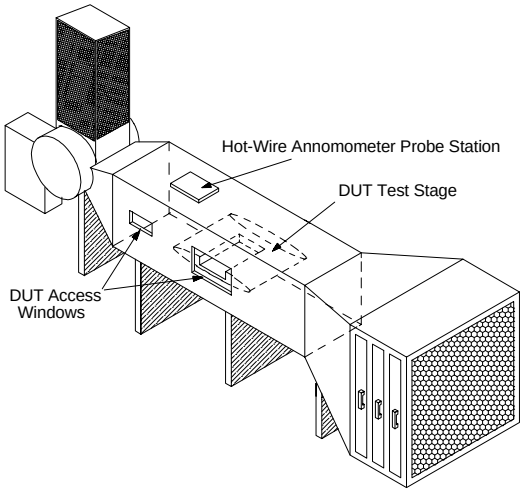

Figure 18. Forced Convection Chamber, Which is Used To Conduct Moving-Air Tests

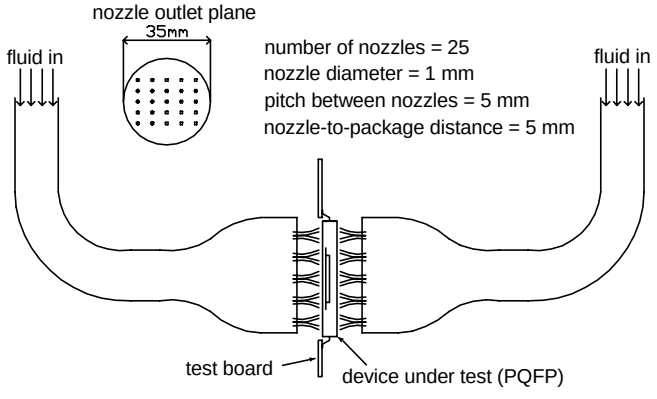

Figure 19. Jet Nozzle Impingement, Which is Used For Taking Case Measurements of a Plastic Package

THERMAL CHARACTERIZATION PARAMETER (Ψ_{JT})

A new parameter has gained popularity due to the misconceptions arising from using the value of θ_{JC} to calculate junction temperatures for plastic packaged devices in end-use environments. This parameter is proportional to the temperature difference between the top center of the package and the junction temperature, relative to the power dissipation. It is a useful parameter for verifying device temperatures in an end-use environment. The sample calculations on page 492 and 493 provide examples of calculations using this new parameter.

THERMAL TEST BOARDS

Before measuring the thermal characteristics of a semiconductor device, the component is assembled onto a test board using industry-standard techniques. The test boards Vantis uses for this are standardized to conform with the JEDEDC specification JESD51_3. Two types of test boards are commonly used: low-effective or high-effective thermal conductivity test boards.

Low-Effective Thermal Conductivity Test Boards

Low-effective thermal conductivity test boards are designed to simulate worst-case board mounting. These boards have no internal planes and minimum trace routing.

High-Effective Thermal Conductivity Test Boards

High-effective thermal conductivity test boards are fabricated to have two evenly spaced internal planes. These boards more closely reflect applications in which ground or power planes are used in the PCB.

For both board types, FR4 is used as the board material, and small gauge wire is used to connect the device to the test interface. The board dimensions are 76.2 mm wide by 114.3 mm long for packages having body sizes <28 mm. For package bodies ≥28 mm, the board size is 101.6 mm wide by 114.3 mm long.

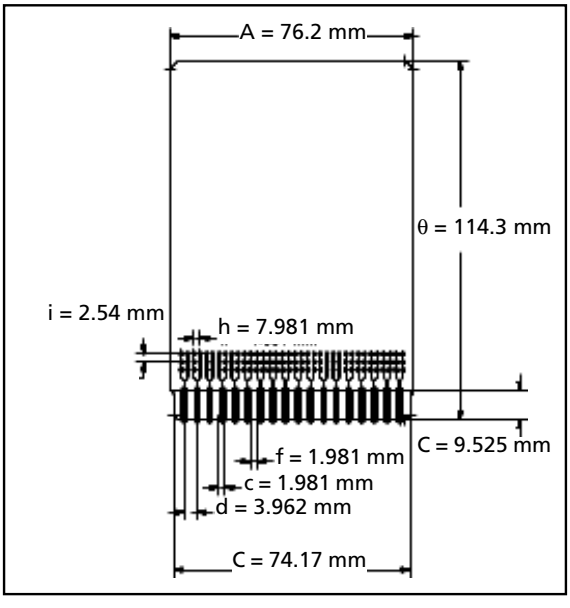

Figure 20. Thermal Test Board Design for IC Packages Having Body Sizes Less Than 28 mm

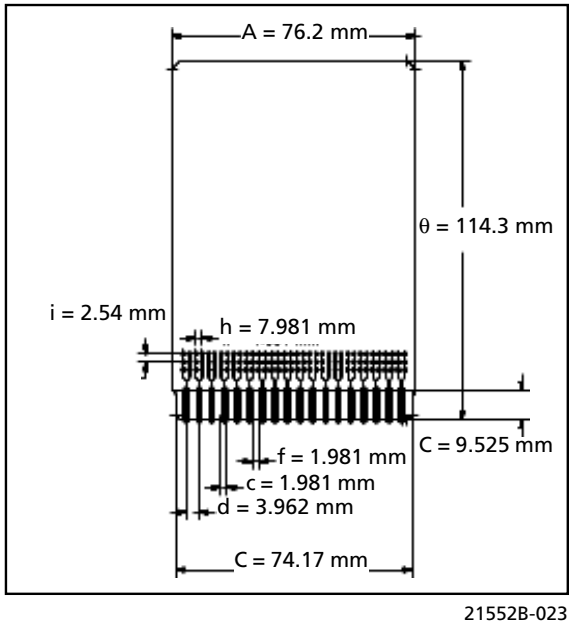

Figure 21. Thermal Test Board Design for IC Packages Having Body Sizes of 28 mm

(See Figures 20 and 21). By standardizing the board, the environment for testing is normalized to the board size, allowing comparisons between package families or package variations within a family. These PCB designs conform to JESD specifications.

PRODUCT CARRIERS PER PACKAGE TYPE

Packing methods for devices have become increasingly important to facilitate automated board assembly and optimize packing density. This goal, along with protecting product reliability, drives the design concepts behind some of the new packing systems.

Vantis offers several packing systems for its through-hole and surface-mount products. The table lists those systems that are used as a standard.

Vantis' packing system designs have kept pace with the sophistication of user needs and product sensitivity. This section provides in-depth descriptions of these designs.

Table 12. Product Carriers for IC Packages

Package Type	Leadcount	Device Carrier	Packing Container
Plastic Dual-In-Line	All leadcounts	Tube	Mini-Q or 1Q box
Plastic Leaded Chip Carrier	≥ 32 lead	Tube	Dry pack & 2k/4k box
		Tape & Reel (Note 1)	Dry pack & reel box
	All others	Tube	2k/4k box
		Tape & Ree (Note 1)	Reel box
Plastic Small Outline & Shrink Plastic Small Outlines	All leadcounts	Tube	Mini-Q or 1Q box
		Tape & Reel (Notes 1 & 2)	Reel box
Plastic Quad Flat Pack & Thin Plastic Quad Flat Pack	All leadcounts	Tray (Note 3)	Dry pack & tray box
Plastic Ball Grid Array	All configurations	Tray (Note 3)	Dry pack & tray box

Notes:

1. *Optional; upon request only*
2. *Except for the SO 028-lead package, which is not available in tape and reel.*
3. *These trays can withstand temperatures of -125 °C to 150 °C.*

Tubes

Tubes are used as unit carriers for most of our lower leadcount packages. The product carrier guide on the next page shows which package families are shipped in tubes as a standard.

All of our tubes are made of an antistatically coated PVC to protect product from electrical and mechanical damage. The tubes are designed to accommodate packages that are loaded with or without unit carriers depending on the package style. Tube sizes are standardized by package type to facilitate automated board assembly.

DEVICE LOADING

Devices are loaded into tubes, with each device pin one uniformly oriented (only one product date code per tube). A variety of end-plug designs, all of antistatic material, secure products in the tube and ensure that there is no excessive movement of product in the tube during shipping and handling. This protects the mechanical integrity of the package and leads; it also ensures an unimpaired dispensing of product for manufacturing operations.

When the end-plug design is a plastic stopper pin, all devices are loaded so pin one is oriented toward the green stopper pin to aid in manufacturing.

This section includes details about the quantity of devices per tube for each package style and leadcount. Vantis encourages but does not require ordering and shipping in full tube quantities. Following the quantity tables, dimension drawings for all of our tube sizes (by package type) are shown, along with the specific end-plug design used.

Consult your Vantis sales representative for additional information about our tubes.

Table 13. Q-Pack Tube and Box Quantity Information

Package		Leadcount	Devices Per Tube	Tubes Per Box	Devices Per Box
Plastic Leaded Chip Carriers	PL	20 lead, square	46	10	460
	PL, PLH	28 lead, square	37	15	555
	PL	44 lead, square	26	10 (note 1)	1040 (note 1)
	PL	68 lead, square	18	15 (note 2)	810 (note 2)
	PL, PLH	84 lead, square	15	16 (note 2)	720 (note 2)
Plastic Small Outline	SO	20 lead	38	15	570
	SO	24 lead	30	16	480

Notes:

1. *The tubes per box actually reflect the quantity of tubes in a dry pack bag, not the Q-Pack box. The device count per box, however, is accurate because four bags of parts are put in the box.*
2. *The tubes per box actually reflect the quantity of tubes in a dry pack bag, not the Q-Pack box. The device count per box, however, is accurate because three bags of parts are put in the box.*

Trays

Trays are used instead of tubes to protect higher leadcount packages from electrical and mechanical damage during handling and shipment. Trays are also suitable for product presentation to board assembly equipment.

All trays are uniformly sized, in compliance with standard JEDEC outlines. As much as possible, Vantis procures trays that are made of 25 percent recycled material. The PVC tray material is either carbon-filled or antistatically coated to provide ESD protection.

Trays for plastic packages can withstand continuous operation at temperatures up to 150°C.

Packages are placed in the trays so that the device pin one is oriented to the notched corner of the tray, enabling pick-and-place equipment setups to be compatible for all packages and leadcount.

For shipment, a stack of six trays are secured with straps; five containing parts and the sixth serving as a cover. The diagrams and tables that follow show tray dimensions per package and the quantities of parts per tray.

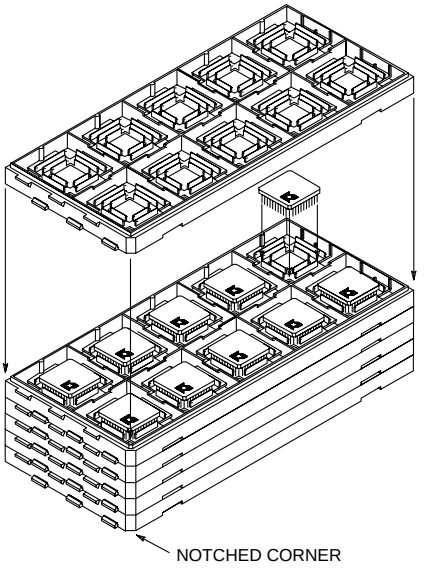

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Figure 22. Five Trays of Product are Stacked for Shipment, With a Sixth Tray Serving as a Cover, and All Devices are Uniformly Oriented so Pin One is Aligned With the Notched Corner of the Tray

Table 14. Tray Device Carriers: Full Tray Quantity Information All Applicable Packages – Tray and Box Quantities

Package		Leadcount	Device Per Tray	Trays Per Box [1]	Devices Per Box
Plastic Quad Flat Pack	PQR	100 lead	66	6 (Note 1)	330
	PQR, PRH, PQE	144 & 160 lead	24		120
	PQR, PRH, PQE	208 & 240 lead	24		120
Thin Plastic Quad Flat Pack	PQT	44 lead	160		800
	PQL	48 lead	250		1250
	PQL	100 lead	90		450
	PQL	144 lead	60		300
	PQL	176 lead	40		200
Plastic Ball Grid Array	BGD	256 ball	40		200
	BGD	352 ball	24		120

Note:

1. In all cases, the top tray is empty, serving as a cover.

Dry Pack Protection

Package cracking can occur when moisture-sensitive product is mounted directly onto a board, versus socket mounted, using a high temperature solder reflow process. As moisture in the encapsulation material heats and vaporizes, the pressure it creates can result in package cracking or delamination. Dry packing product keeps the moisture level in the encapsulation material below a critical level, providing you with “solder-safe” packages.

Product that is dry packed is first baked for 5 to 11 hours, depending on the product, at 125 °C and then sealed under a partial vacuum in a moisture barrier bag containing desiccant and a humidity indicator card. The bag interior is maintained at a safe relative humidity (RH) level of ≤20%. Once product is removed from the bag, or the bag seal is broken, the product should be board mounted within the recommended out-of-bag time (assuming the assumptions about the end-use factory environment are reasonably accurate). The out-of-bag time and the factory environment assumptions are listed on the dry pack caution label that is applied to the outside of every dry pack bag. If the out-of-bag time is exceeded, or the humidity indicator card upon opening the bag registers ≥30% RH, then product should be baked for 24 hours at 125 °C before board mounting. The tray in which Vantis ships product can withstand up to 150 °C; however, product in tubes or reels must be either put in metal tubes or baked for 192 hours at 40 °C at 5% RH.

Vantis determines the moisture sensitivity of our product by testing them per the JEDEC industry-standard A112-A/A113 process. Depending on the results, product classified under one of six sensitivity levels, with Level 1 being not moisture sensitive, The sensitivity rating for product is indicated on the dry pack caution label on the outside of every dry pack bag. The table lists the current sensitivity levels for all Vantis products that are dry packed.

Table 15. Vantis Moisture Sensitive Products

Package	Leadcount	JEDEC Level	Out-Of-Bag Time [1]
Plastic Leaded Chip Carriers (PLCCs)	≤ 28 Lead	2	1 year
	≥ 44 lead	3	168 hours
Metric (Note 2) Plastic Quad Flat Packs (PQFPs)	144 & 208 lead	3	168 hours
	All others	3	168 hours
Thin Plastic Quad Flat Packs (TQFPs)	All leadcounts	3	168 hours
Small Outline (SO)	≤ 24 lead	3	168 hours
Plastic Ball Grid Arrays (BGAs)	All ball counts	3	168 hours

Notes:

1. *Assumes an end-use factory environment of ≤30 °C and 60% RH.*
2. *Includes PQFP packages denoted internally by Vantis as PQR, PRH, and PQE.*

Tape & Reel: Full Reel Quantity Information

Tape-and reel device carriers are available for selected IC packages, as shown in the table below. This carrier is designed to protect product from mechanical and electrical damage, and it is suitable for device presentation to automatic pick-and-place equipment.

The tape-and-reel design consists of a pocketed carrier tape which is loaded with one device per pocket. Each device is oriented in the pocket so that its pin-one location complies with the Engineering Industries Association Standard 481. A protective cover tape is heated-sealed over the carrier tape to keep devices in the pockets. The carrier tape is made of conductive polystyrene, and the cover tape is antistatic polyester-both of which protect product from ESD damage.

Once loaded, the tape is wound onto an antistatic plastic reel for packing and shipment. Each reel is labeled with a standard inventory label identifying the contents. The number of device per full reel are provided in the table shown.

Package	Leadcount	Qty/Reel
Plastic Leaded Chip Carrier (PL, PLH)	20 lead	1000
	28 lead	750
	44 lead	500
	68 and 84 lead	250
Plastic Small Outline (SO)	20 and 24 lead	1000
Thin Plastic Quad Flat Pack (PQL, PQT)	44 lead (PQT)	1500
	48 lead (PQL)	2000
	100 lead (PQL)	1000
	144 lead (PQL)	500
Plastic Ball Grid Array (BGD)	256 ball count 352 ball count	TBD

Notes:

1. *300 mm of empty trailer pockets are provided at the beginning of the reel to facilitate feeding the tape into automatic board assembly equipment.*
2. *500 mm of empty leader pockets are provided at the end of the reel.*

CONTROLLING MOISTURE

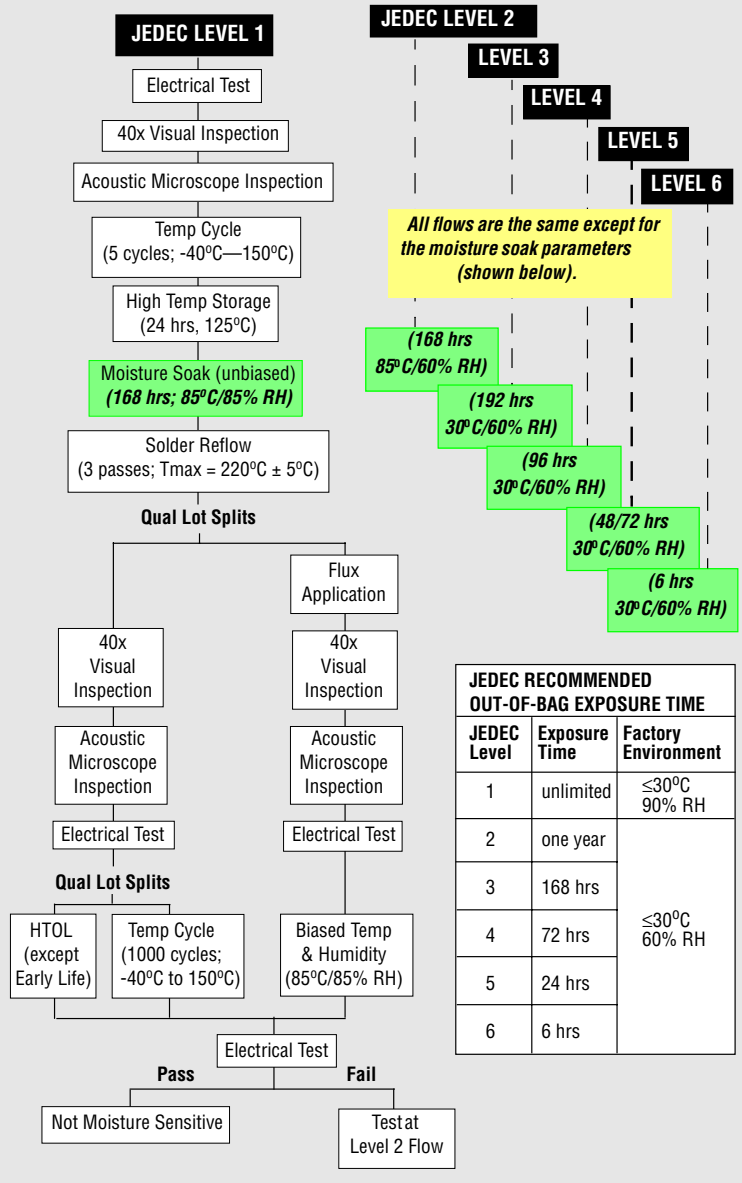
In designing packing materials and packing methods, Vantis is sensitive to the susceptibility of some IC packages to moisture-induced damage. The risk of this is highest when plastic encapsulation materials are used, as plastic is naturally permeable to moisture. The moisture in the package will increase or decrease to reach the Relative Humidity (RH) of the surrounding environment.

Therefore, controlling the moisture level in the package body is critical to reducing the risk of moisture-induced damage. Such damage may include delamination between the die and the plastic encapsulation material, which may result in open connections due to broken wirebonds. Package cracking may also occur when the components are exposed to the high temperatures and steep temperature gradients used in reflow board assembly techniques. Moisture in the package rapidly heats and vaporizes and, if there is sufficient steam due to the moisture in the package having reached a critical level, it will fracture the package to escape. This phenomenon is known as the "popcorn effect."

TESTING PRODUCTS FOR MOISTURE SENSITIVITY

To better understand and classify the moisture sensitivity of our products, Vantis has adopted the JEDEC test methods A112-A/A113A. These have been adopted by the industry as the standard process by which to determine the moisture sensitivity of IC components.

JEDEC A112-A/A113A Process Flows



JEDEC RECOMMENDED OUT-OF-BAG EXPOSURE TIME

JEDEC Level	Exposure Time	Factory Environment
1	unlimited	≤30ºC 90% RH
2	one year	≤30ºC 60% RH
3	168 hrs	
4	72 hrs	
5	24 hrs	
6	6 hrs	

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JEDEC Test Standard A112-A/A113A

This test standard (shown on page 507) defines six different moisture sensitivity levels, referred to as level 1, level 2, through to level 6. Each higher level denotes a higher level of sensitivity. Product that fails the level 1 flow is then tested at a higher level until it passes. Specific process steps in each flow subject the product to conditions designed to simulate the environment of an end-use application. Subsequent electrical testing and inspection steps determine if the device was damaged during the environmental stress steps.

The only difference between each A112-A/A113A flow is the parameters of the moisture soak step (also known as preconditioning). These parameters are designed to allow the component to absorb as much moisture as it can given its package size. The purpose of the testing is to determine the safe environmental conditions for product exposure.

Once it is determined that product is moisture sensitive (i.e., it fails the level 1 flow), Vantis dry packs the product for storage and shipment. This is done regardless of the type of product carrier used (e.g., tubes, trays, reels, etc.). Dry packing protects product from environmental moisture by maintaining the interior of the dry pack bag at ≤20 percent RH.

DRY PACKING PROCESS AND MATERIALS

The first step in the dry pack process is to remove any moisture buildup in the package by baking the finished product for 5 to 15.5 hours, depending on the package type, at 125 °C ± 5 °C. While baking, the product is contained in device trays (made of material that can withstand the high temperature) or aluminum trays or tubes. Within 50 hours after baking, the product is sealed in a dry pack bag under a partial vacuum. The bag is sealed using an impulse heat sealer at a seal time of 1.0 to 1.5 seconds; a seal pressure of 40 to 50 psi; and a temperature range of 191 °C to 232 °C.

Included in the dry pack bag are a prescribed number of humidity indicator cards and desiccant pouches, depending on the quantity of devices in the bag.

GENERAL REFERENCES

1. "Thermal Characteristics," Method 1012.1, MIL-STD-883C, Test Methods and Procedures for Microelectronics, Department of Defense, Washington, DC.
2. "Semiconductor Measurement Technology: Thermal Resistance Measurements," F.F. Oettinger and D.L. Blackburn, NIST Special Publication 400-86, Department of Commerce, Washington, DC.
3. Accepted Practices for Making Microelectronic Device Thermal Characteristics Tests - A User's Guide," JEDEC Engineering Bulletin No. 20, Electronic Industries Association, Washington, DC.
4. "Still-and Forced-Air Junction-To-Ambient Thermal Resistance Measurements of Integrated Circuit Packages," SEMI G38-87 Test Method, 1989 Book of SEMI Standards, Vol. 4, Packaging Division, SEMI, Inc. Mountain View, CA.
5. "Junction-To-Case Thermal Resistance Measurements of Molded-Plastic Packages," SEMI G43-87 Test Method, 1989 Book of SEMI Standards, Vol. 4, Packaging Division, SEMI, Inc. Mountain View, CA.
6. "Junction-to-Case Thermal Resistance Measurements of Ceramic Packages," SEMI G30-88 Test Method, 1989 Book of SEMI Standards, Vol. 4, Packaging Division, SEMI, Inc. Mountain View, CA.
7. "Unencapsulated Thermal Test Chip," SEMI G32-86 Guideline, 1989 Book of SEMI Standards, Vol. 4, Packaging Division, SEMI, Inc. Mountain View, CA.
8. "Thermal Test Board Standardization for Measuring Junction-to-Ambient Thermal Resistance of Semiconductor Packages," SEMI G42-88 Specification, 1989 Book of SEMI Standards, Vol. 4, Packaging Division, SEMI, Inc. Mountain View, CA.
9. "Thermal Transient Testing for Die Attachment Evaluation of Integrated Circuits," SEMI G46-88 Test Method, 1989 Book of SEMI Standards, Vol. 4, Packaging Division, SEMI, Inc. Mountain View, CA.
10. "Applying the Electrical Test Method To Thermal Characterization of MOS Integrated Circuits," B.S. Siegal, SAGE Enterprises, Mountain View, CA, 1985. (Semitherm 2 Conference Proceedings)
11. "An Electrical Technique for the Measurement of Integrated Circuit Thermal Resistance," TA7802, B. Siegal, SAGE Enterprises, Inc. Mountain View, CA.
12. "Junction-To-Case Thermal Resistance--Still A Myth?," Dutta, V. B., National Semiconductor Corp., Santa Clara, CA, Fourth Annual IEEE Semitherm Conference Proceedings
13. "How Fast Is It Blowing?: Design and Characterization of a Laboratory Wind Tunnel" Hayward, J.D., and Van Andel, R., Advanced Micro Devices, Sunnyvale, CA.
14. Microelectronics Packaging Handbook, Tummala, Rao R., Rymaszewski, Eugene J., 1989, Van Nostrand Reinhold
15. EIA/JEDEC JESD51, "Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)," Electronic Industries Association, 1995
16. EIA JEDEC JESD 51_1, "Integrated Circuit Thermal Measurement Method - Electrical Test Method (Single Semiconductor Device)," Electronic Industries Association, 1995

17.EIA JEDEC JESD 51_2, “Integrated Circuit Thermal Test Method - Environmental Conditions, Natural Convection (Still Air),” Electronic Industries Association, 1995

18.EIA/JEDEC JESD 51_3, “Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages,” Electronic Industries Association, 1995