VANTIS

BEYOND PERFORMANCE

The Evolution of Bus-Friendly Inputs and I/Os

INTRODUCTION

Vantis' PLDs have evolved over time. Like Darwin's theory of evolution and adaptation, Vantis' PLDs have evolved and adapted to the dynamic world of digital logic. When Vantis' PLDs were first introduced to the market in the mid-1980s, they had different characteristics than the PLDs presently in existence. The older devices were larger in size, slower in speed, and hungrier for power than their contemporary counterparts. As the computer industry evolved to accommodate applications requiring faster, smaller, and lower power devices, PLDs were modified in order to accommodate these changes and stay competitive in the PLD market arena.

DEVICES WITH UNBIASED INPUTS AND I/O

Originally, Vantis introduced PLDs with unbiased inputs and I/Os which is basically a carry over of the bipolar configuration. The circuit configuration is shown in Figure 1 and consists of a buffer that is directly connected to the pin pad.

If the pin is left unconnected, this configuration is termed "floating" because an unused input pin is allowed to float to any state, since there is no circuitry that would bias the pin to a known state. The consequence in leaving the pin floating is that excessive noise or having a voltage near the threshold voltage of the PLD could influence the PLD to produce an unwanted oscillatory output that could disturb the system. In addition, the noise on V_{CC} will also increase due to this oscillation. Figure 2 shows the event of device oscillation due to a noisy input signal through an unused input pin.

Even though it is recommended to tie unused input pins to ground or V_{CC}, traces must be cut on a printed circuit board in order to free the tied pins when changes are made. Unfortunately, this poses an inconvenience to the customer. As a result, Vantis decided it was best to modify the input and I/O circuitry of all PLD devices.

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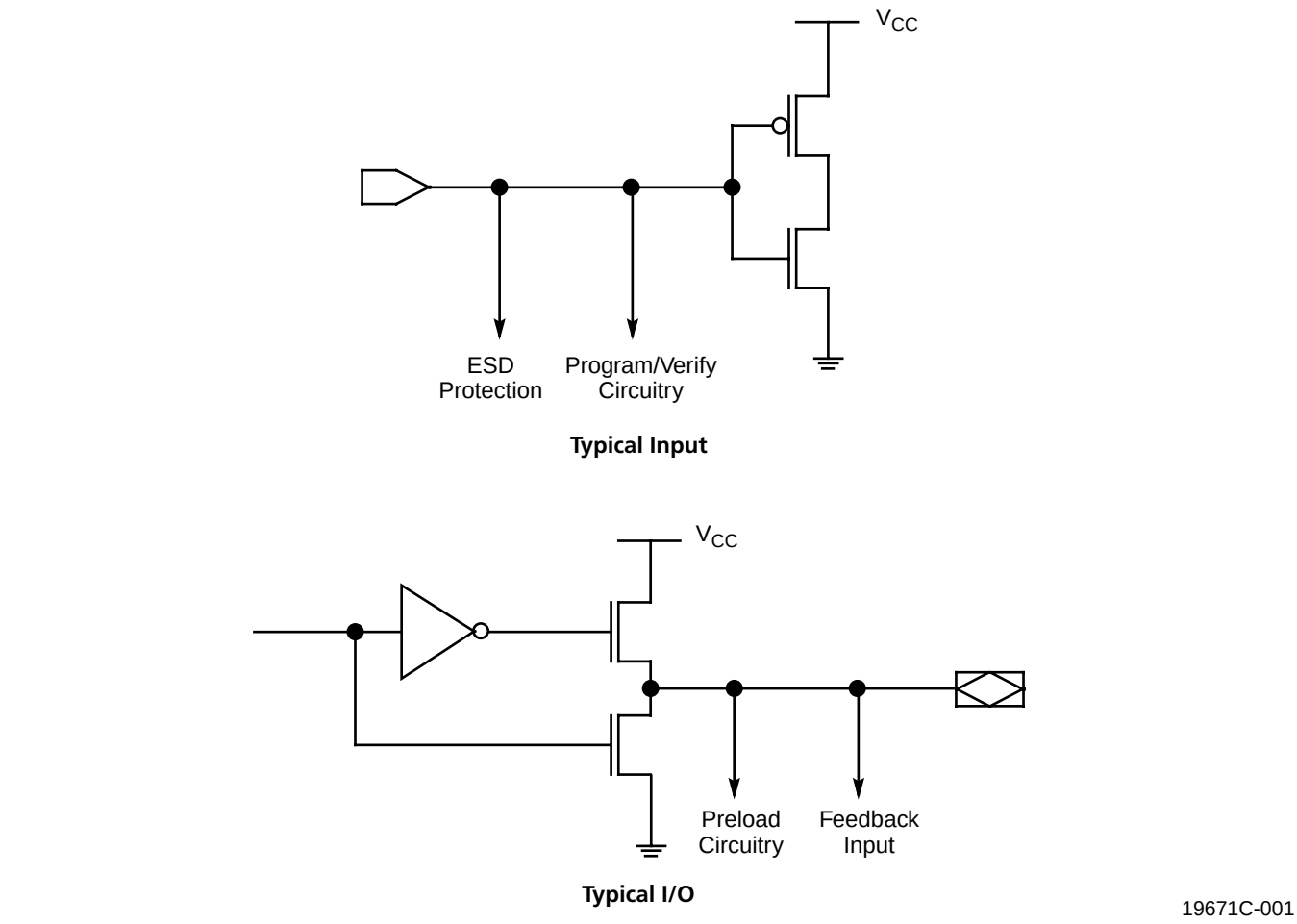


Figure 1. Equivalent Schematic of the Unbiased Input and I/O Scheme

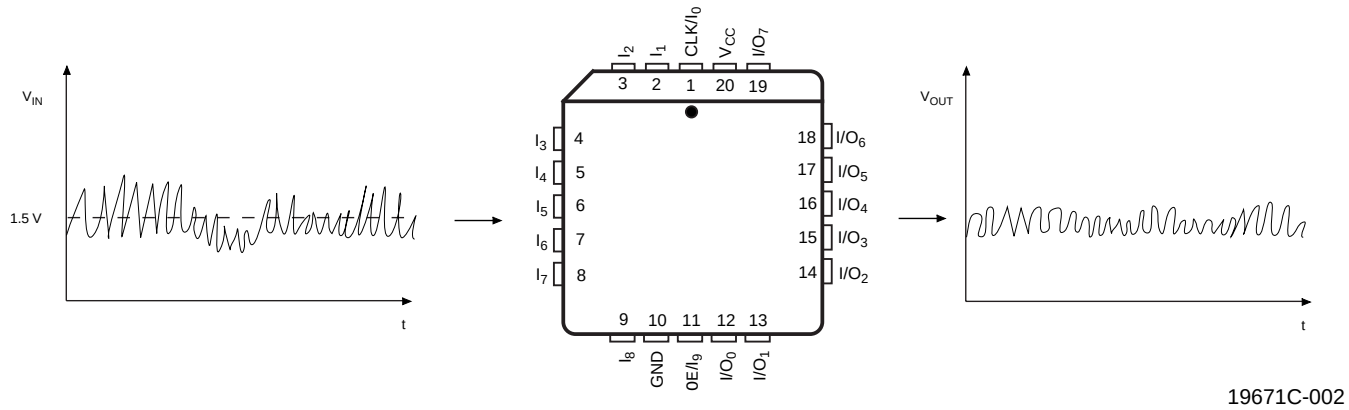


Figure 2. Output Oscillation Due to Noisy Input of an Unbiased "Floating" Input Pin

PULL-UP RESISTOR ENHANCEMENT

The improvement was to add a pull-up resistor to the input and I/Os so that if the pins were left floating, the device could pull its pin voltage to a known voltage state. Figure 3 shows the circuit configuration of the pull-up resistor scheme.

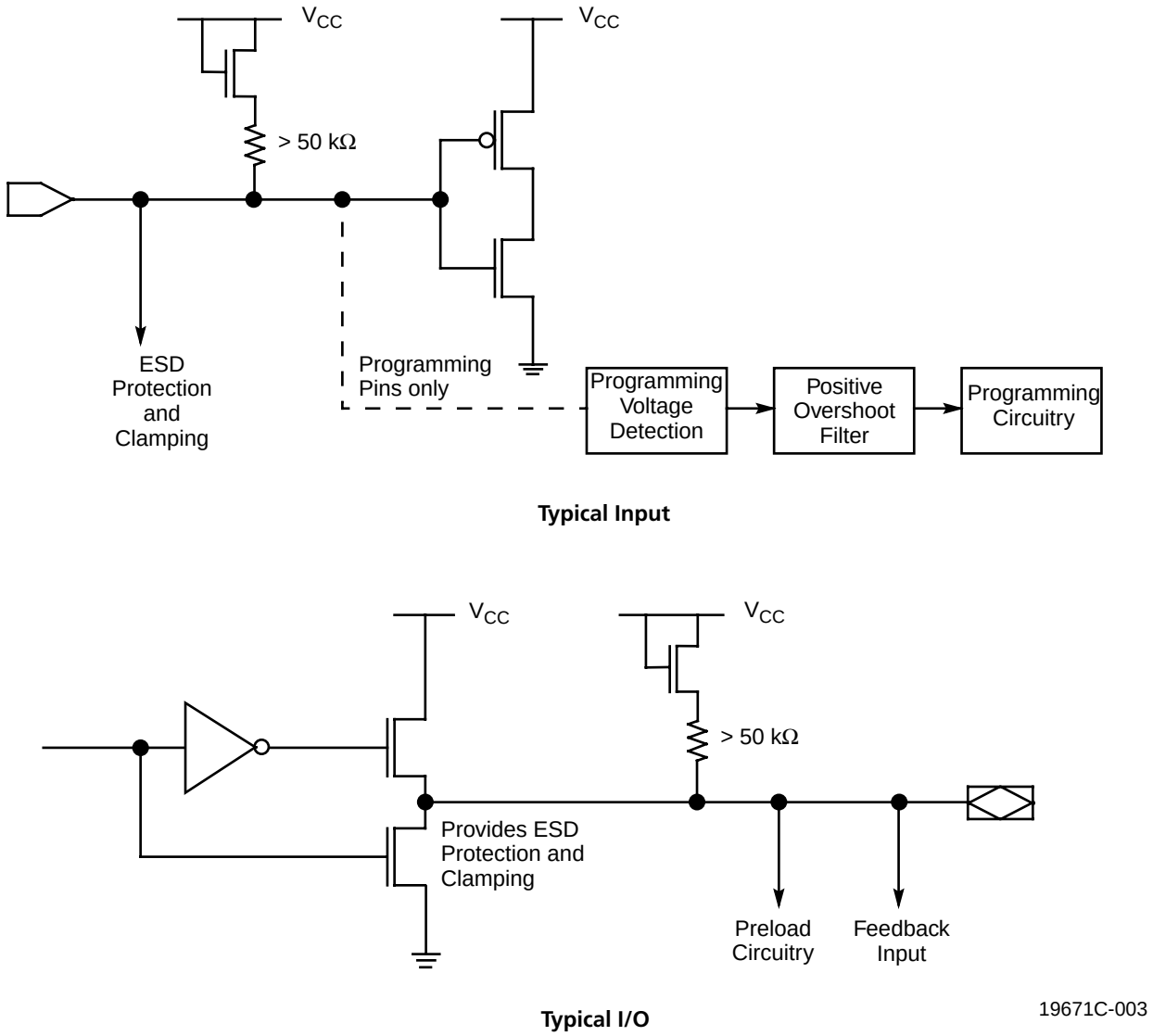
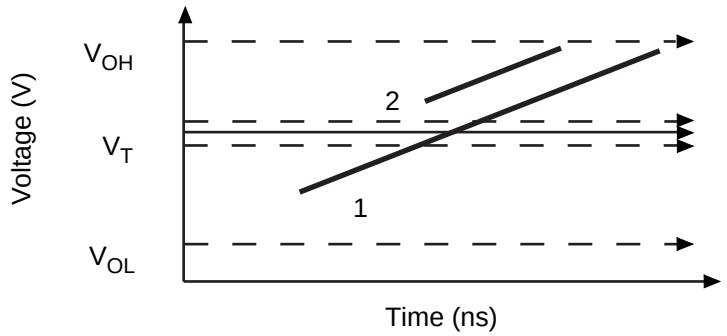


Figure 3. Equivalent Schematic of Pull-up Resistor Scheme

This scheme consists of a 50 kΩ resistor that is connected to a constant current source which is used to hold down any excessive current in the event that the 50 kΩ resistor is disabled. The pull-up resistor scheme pulls the voltage of the pin to about 3.5 V-4.0 V. The 50 kΩ resistor value is used because this value provides a voltage that is easy enough for another driver to overcome when necessary because of the current-limiting effect of the large resistance.

Even though the pin is pulled to a known state, the pull-up scheme can potentially introduce oscillation to a system if the voltage of a tri-state bus is left below the threshold voltage of the PLD. The reason for the potential problem is due to the nature of the pull-up resistor within the PLD. The internal pull-up resistor is only capable of pulling from a low to a high voltage state.

In addition, the slew rate is slow due to the 50 kΩ current-limiting resistor. Thus, when a pin voltage is left below the threshold voltage of the PLD, the pull-up resistor has no other choice but to pull the pin voltage slowly through the threshold voltage region of the PLD. On the contrary, if the voltage of the tri-state bus is at a voltage state higher than the threshold voltage of the PLD, then the PLD will not exhibit oscillation. Note that if some other device overpowers the weak pull-up resistor of the PLD causing the tri-state bus voltage to reside around the threshold voltage of the PLD, then device oscillation is also possible. Both the high and low tri-state bus scenarios are shown in slew rate curves in Figure 4.



Bus Scenario

1 = Tri-State Bus left low with Pull-up scheme
2 = Tri-State Bus left high with Pull-up scheme

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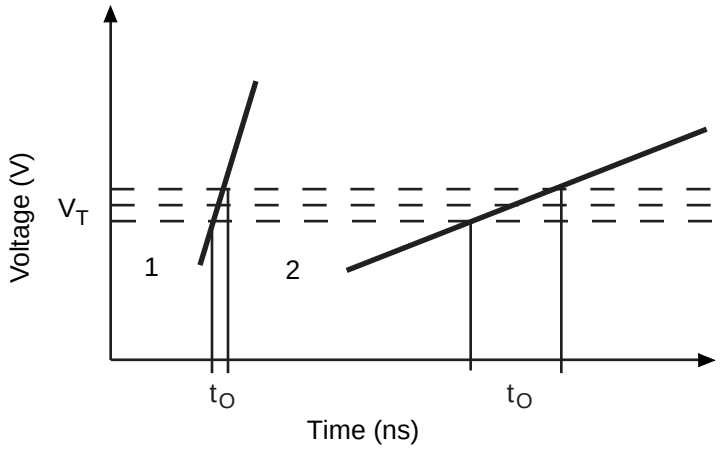
Figure 4. Slew Rate Comparison of Pull-up Scheme Showing Bus Scenarios

DEVICE OSCILLATION

The reason a device oscillates is because of the nature of the threshold voltage of the transistors within the input and I/O buffers of the PLD. Typically, the threshold voltage of an input buffer is 1.5 V. When a pin voltage is around the threshold voltage, the complementary transistor pair does not know whether to switch high or low, thus oscillation is possible at the output. Usually, this fickle nature lasts no more than a few nanoseconds; however, for faster systems this can be significant.

When a large pull-up resistor is used such as those used in the PLD industry, the slow slew rate allows the voltage to reside in the threshold region longer than if a smaller pull-up resistor is used. For comparison, Figure 5 shows the difference in the time of oscillation between a 50 kΩ resistor and a 1 kΩ resistor through slew rate curves.

Because the possibility of device oscillation could occur with the pull-up resistor scheme, another scheme had to be implemented.



1 = Slew rate of 1 kΩ pull-up resistor
2 = Slew rate of 50 kΩ pull-up resistor
t_O = Time of potential oscillation

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Figure 5. Slew Rate Comparison Between a 1 kΩ and 50 kΩ Pull-up Resistor

BUS-FRIENDLY INPUT AND I/O

Bus-Friendly™ inputs and I/Os have the ability to hold the input buffer at either a high or a low depending on the last state of the pin connected to the bus. The scheme is termed "Bus-Friendly" because it allows the bus connected to the PLD to be left at any state (other than the 1.5 V threshold voltage of the input and I/O buffers). For PAL devices, the Bus-Friendly scheme is accomplished by reconfiguring already existing resources of the pull-up scheme as shown in Figure 6.

In MACH® devices, the scheme is configured slightly differently by having a separate circuit perform the "latch" characteristic as shown in Figure 7.

The Bus-Friendly circuitry pulls the voltage at the input buffer to a TTL voltage high or low. This input and I/O scheme is accomplished by a double inverter input buffer which loops back to the input of the PLD through a 100 k**Ω** resistor. This configuration acts as a "latch" because it holds the pin voltage of the PLD at either a TTL level high or low until the pin voltage of the PLD changes state. Bus-Friendly circuitry weakly holds the voltage so that another driver on the bus can overcome the voltage when necessary. Please note that the default state of the pin is no longer a voltage high but is rather dependent on the last driven state of the pin. Designers who need to have the pull-up feature will need to provide an external pull-up resistor rather than depend on the pull-up resistor of the PLD.

The Bus-Friendly scheme provides a solution to the instance where the pull-up scheme could potentially cause input buffer oscillation. As illustrated earlier in Figure 4, the pull-up scheme cannot resolve the case when the tri-state bus connected to the PLD is left at a voltage below the threshold voltage of the PLD. This type of bus scenario promotes undesirable device oscillation. The Bus-Friendly idea is an improvement over the pull-up resistor scheme because

the Bus-Friendly circuitry does not allow the voltage to cross the threshold region of the PLD, thus avoiding the possibility of device oscillation. Figure 8 shows how Bus-Friendly PLDs deal with the same bus scenarios that the pull-up resistor scheme did in Figure 4.

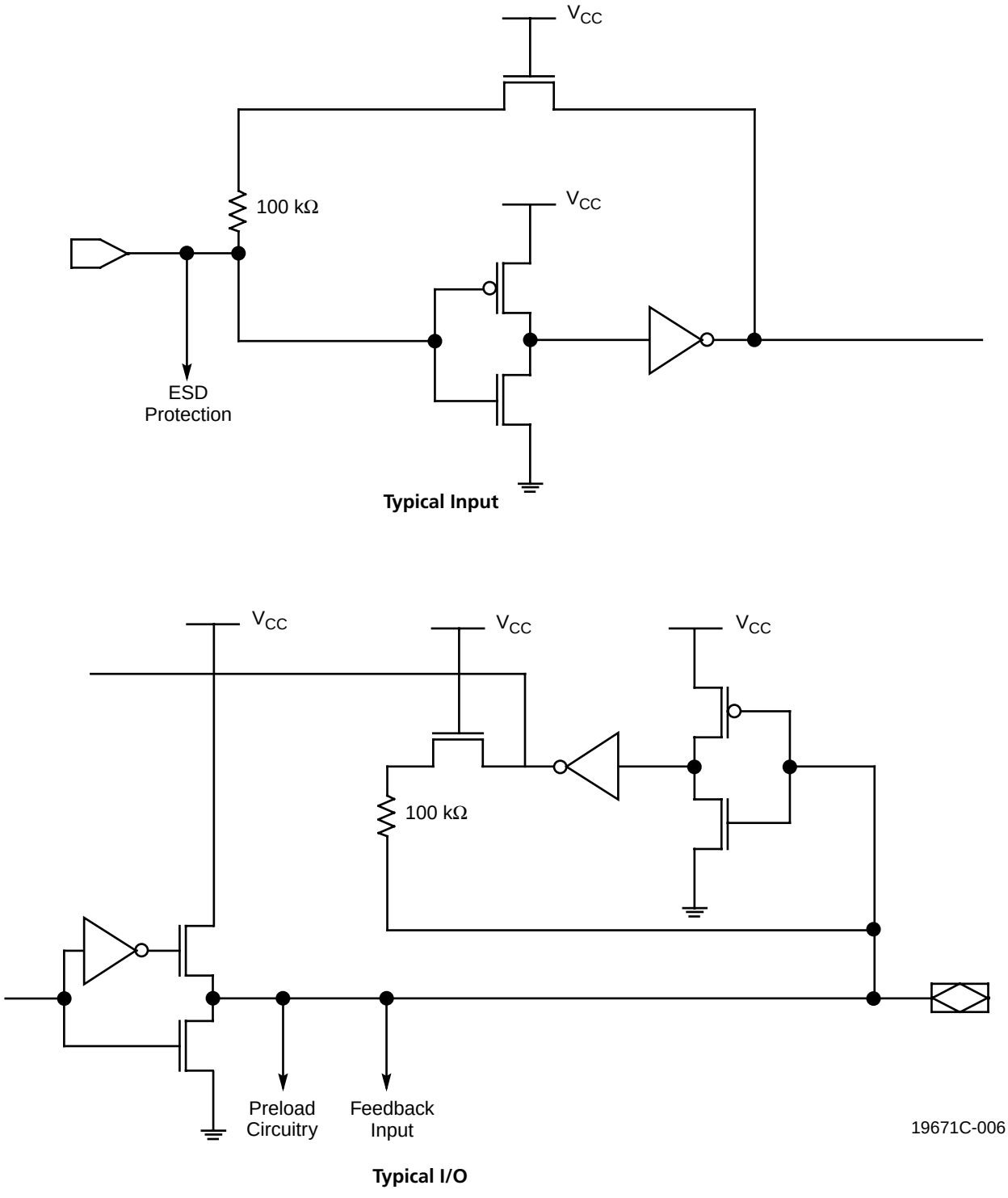

Figure 6. Equivalent Schematic of the Bus-Friendly Input and I/O for PAL Devices

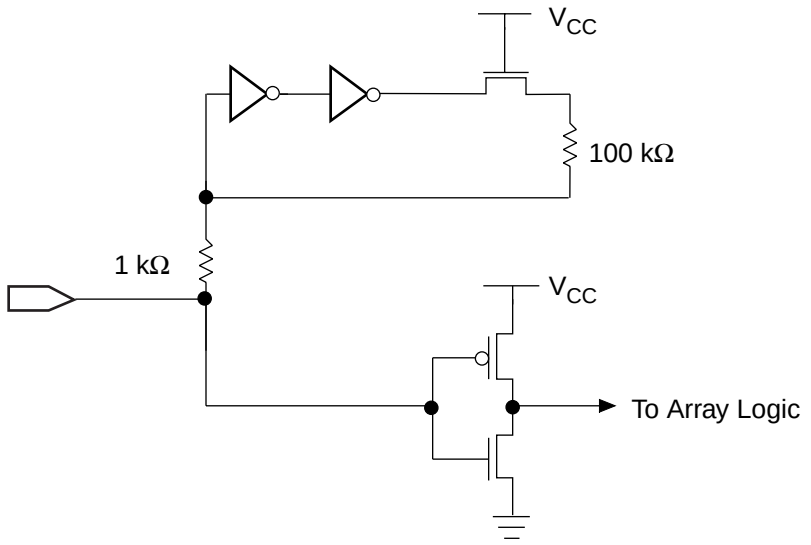

Figure 7. Equivalent Schematic of the Bus-Friendly Input and I/O for MACH CPLDs

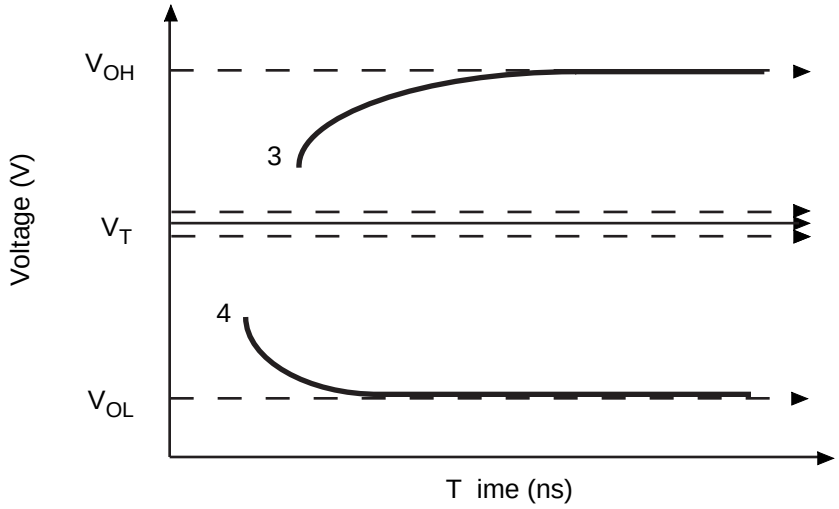

Figure 8. Slew Rate Comparison of Bus-Friendly Scheme Showing Bus Scenarios

Note that if another driver on the bus is forcing the tri-state bus to reside in the threshold voltage region of the PLD, then no matter what type of input and I/O scheme is used, the PLD can oscillate for a few nanoseconds.

The Bus-Friendly enhancement does not affect the existing DC and AC specifications for both the MACH and PAL products which previously had the pull-up resistor enhancement. Bus-Friendly was intended to remedy device oscillation without changing any of the device specifications.

SUMMARY

Just as the computer industry has evolved, so have Vantis' PLDs. The input and I/O circuitry of Vantis PLDs have changed to accommodate the different applications that have emerged due to the evolution of the computer industry. The circuitry has evolved from unbiased to pull-up to Bus-Friendly inputs and I/Os. The unbiased inputs and I/Os have disadvantages due to the nature of the floating input. When left unconnected, unbiased inputs and I/Os "float" and are susceptible to the influence of noise, which can cause the PLD to oscillate. Because of this oscillation, the pull-up resistor became the next link in the PLD input and I/O evolution chain.

The pull-up resistor can bias an unconnected pin to a high voltage state. However, the one-dimensional nature of the large pull-up resistor could not avoid device oscillation in particular situations. As board designs required the tri-state bus to be left low, the current-limiting, internal pull-up resistor would slowly pull the voltage of the pin through the threshold region of the PLD, thus causing device oscillation. Because this situation can potentially occur in different instances other than the low voltage, tri-state bus scenario, it was clear that a new pin bias scheme should be implemented.

Bus-Friendly inputs and I/Os have the ability to hold the last voltage state of the tri-state bus at a discrete TTL voltage level. The advantage of this scheme is that a tri-state bus can be at either a high or a low voltage state without having the PLD oscillate. It is because of this feature the name "Bus-Friendly" was used to describe this pin bias scheme.