VANTIS
BEYOND PERFORMANCE

Metastability

INTRODUCTION

A significant number of digital systems must deal with inputs not synchronized to their own internal clocks. These asynchronous signals can arise from any of the various asynchronous protocols which are often used in bus designs; they can be the result of trying to share signals from systems with different clocks; or they may be the response of a system user, who is of course not synchronized with the system. The result can be metastability, a problem which can plague unwary designers. It is not a newly discovered phenomenon, but is normally dealt with somewhat qualitatively, and, unfortunately, is usually ignored as much as possible.

CAUSES OF METASTABILITY

The flip-flop setup time is the parameter that is most often at the root of metastability. The setup time is a requirement that data be made available at the input to the flip-flop before the clock signal arrives. The data must not only be there, but must also be stable.

In a PLD, the use of an array for the data adds to the setup time. The data passes through the array on its way to the flip-flop (Figure 1). The clock signal, on the other hand, goes directly from the clock pin to the flip-flop. Its path is much shorter than the data path. The setup time is a requirement that the data signal must be given more time to get to the flip-flop before the clock signal.

If the published setup time is satisfied, the data arrives at the flip-flop well before the clock, and the output to the flip-flop will change as desired (Figure 2). If the setup time is violated, then no guarantee can be made about what the output will do. The output could be normal, since the published setup time is a worst-case number. However, if the timing between the clock and data is just right, the output will be unstable for some time before it settles into some state. Neither the time the output remains unstable nor the final state is predictable (Figure 3). This condition is metastability.

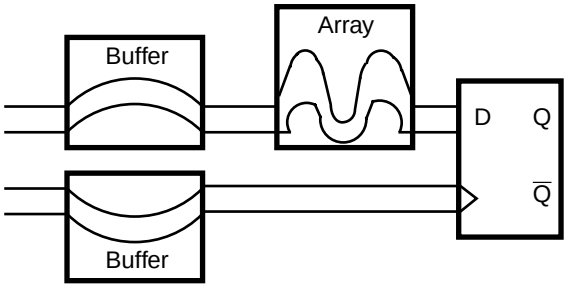

Figure 1. The Clock and Data Paths in a PLD

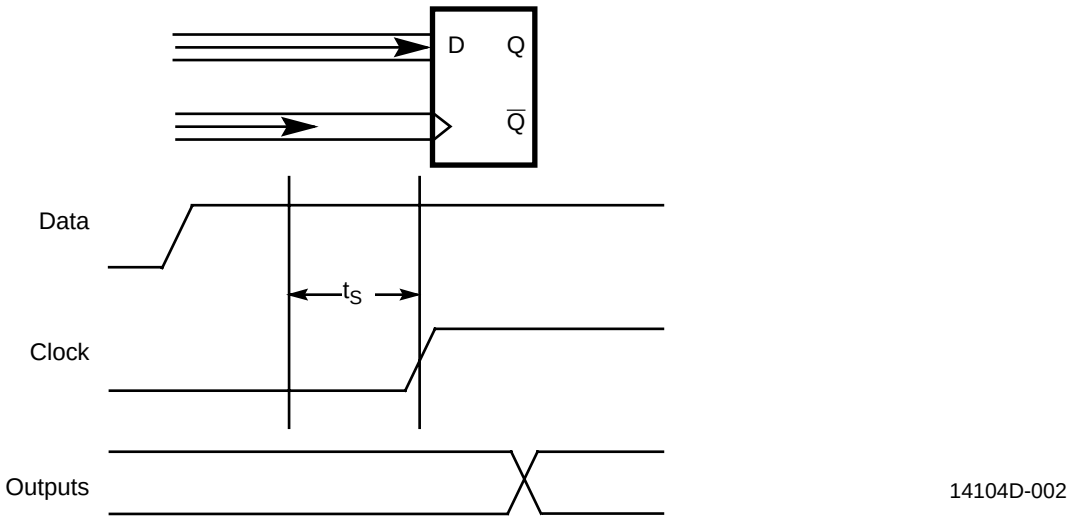

Figure 2. Output Response When the Setup Time Is Satisfied

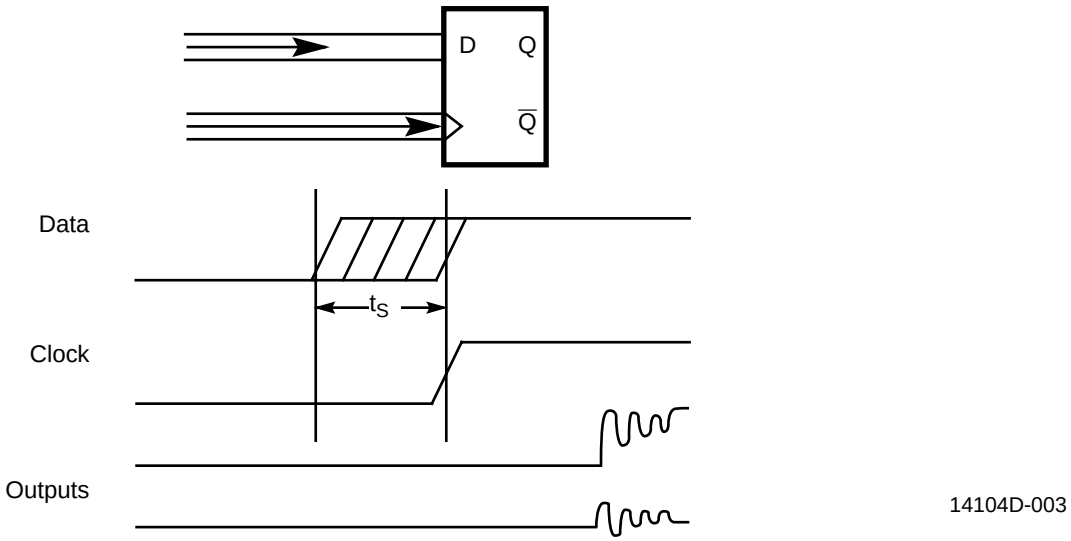

Figure 3. Possible Output Response When the Setup Time Is Violated

SOLUTIONS FOR METASTABILITY

The most common way of dealing with this problem is to synchronize the inputs with an extra flip-flop (Figure 4). If the first flip-flop goes metastable, hopefully the delay between clock pulses will allow the ringing to die down before clocking into the next flip-flop. This improves the chances of having good data in the second flip-flop.

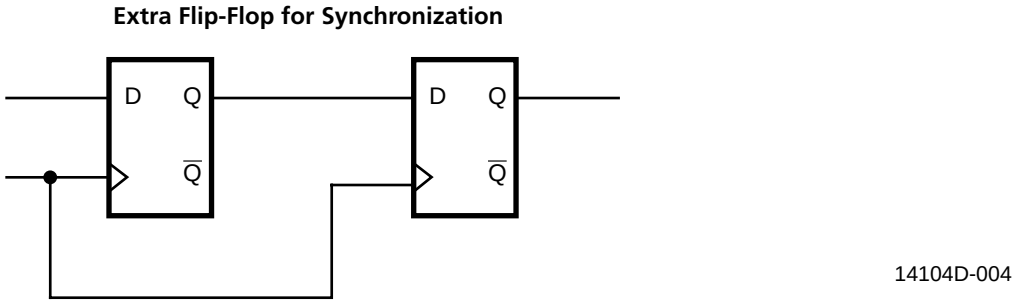

Figure 4. Dual Synchronizer

This method is not without its costs. Each extra stage of flip-flop means an extra clock delay of the data which must be absorbed by the system. Moreover, it is not foolproof. The possibility of metastability is reduced, but not eliminated. A flip-flop can go metastable if the preceding stage does not recover quickly enough.

The best way to avoid metastability is to avoid synchronization when possible. Many applications, such as bus arbitration schemes, use synchronization not because synchronization itself is necessary, but because it provides the only convenient way to store data. This unfortunately takes a system that is inherently asynchronous and adds some synchronizing elements in the middle.

SUMMARY

Metastability can occur in a number of different kinds of asynchronous systems, usually due to the inability to guarantee that the setup time of the flip-flops will be satisfied. In standard synchronous systems where the setup time (along with all other timing requirements) is specifically designed in, metastability will never be a problem.

In some situations, metastability is caused by the need to interface systems with different clocks. In this case, it will never be possible to completely eliminate the possibility of metastability. Instead, the designer must take steps to reduce the probability of a system failure due to metastability.