VANTIS

BEYOND PERFORMANCE

Ground Bounce

INTRODUCTION

The development of fast PLDs has increased the importance of analog considerations the digital designer has been able to overlook in the past. One of these is ground bounce. Ground bounce refers to the ringing on an output signal when one or more outputs on the same device are being switched from HIGH to LOW. This ringing can be in excess of 3 V. The system cannot consider the data valid until the ringing settles to below the V_{IL} of the receiving devices. The ringing in a fast device can last so long that a slower device with less ground bounce could actually be a faster solution.

The phenomenon of ground bounce is associated with the inductance and resistance of the ground connection in the integrated circuit. As there is always some inductance and resistance, ground bounce cannot be totally eliminated; however, it can be reduced to a level tolerable to the system.

This article will discuss the mechanism of ground bounce in CMOS circuitry and the utilization of slew-rate control used by Vantis to minimize ground bounce to reasonable limits.

MECHANISM

Figure 1 shows a schematic of an output driver and load including parasitic elements. The load capacitor is charged to the HIGH-level voltage. When the transistor turns on, the capacitor discharges into the transistor and lead impedance. The resultant RLC circuit will have a damped ringing (Figure 2). The peak amplitude depends on the edge rate of the switch and the RLC values, while the frequency of the ringing and the rate of decay depend only on the RLC values.

Publication# **13090** Rev: **C**
Amendment/**0** Issue Date: **November 1998**

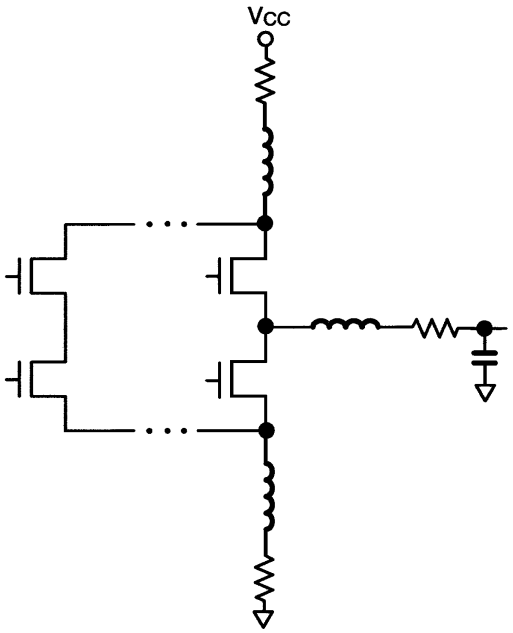

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Figure 1. Simplified Schematic of an Output Driver

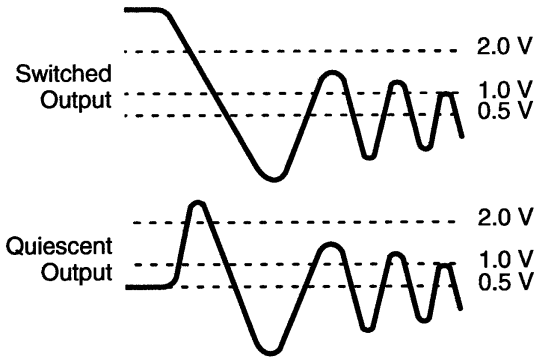

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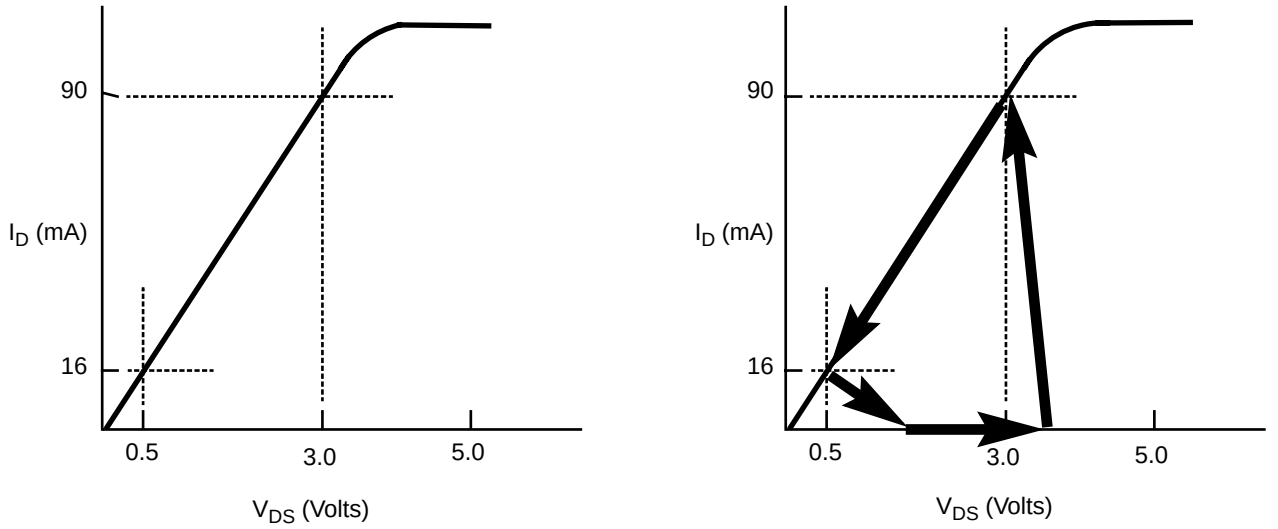
Figure 2. Ground Bounce

The ringing caused by a single output switching is normally below the LOW-threshold voltage. However, the voltage at the ground pad of the device is proportional to the number of outputs switching simultaneously. In addition, the voltage at the ground pad is coupled to any LOW output through its output transistor. Therefore, if enough outputs switch, ringing on the ground pad will be coupled to LOW outputs, causing the detection of false HIGHs.

Most PLDs used today have relatively low output drive current: 16 mA or 24 mA. It is tempting to think that the low current level will somehow limit the switching energy and therefore ground bounce. Actually, even a low-power transistor can pass a relatively large current. The transistor I-V curve in Figure 3a shows that a MOS transistor designed for 16 mA at 0.5 V will pass 90 mA at 3.0 V. Figure 3b shows the V/I path when the output transistor switches between HIGH and LOW. Notice that the transistor switches from 3.5 V at 0 mA to 3.0 V at 90 mA. If eight outputs were to switch simultaneously, 90 mA x 8, or 720 mA, would flow through the ground lead.



a. The DC curve of an output driver transistor

b. The path followed as the transistor switches between the HIGH and LOW levels

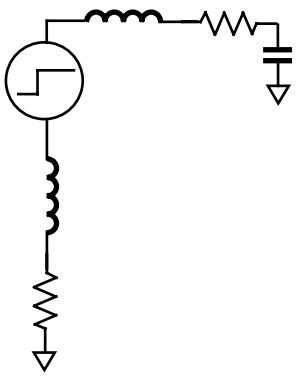
Figure 3. I-V Curves

This sudden current surge is actually self-limiting. As the ground-pad voltage rises due to the high current change, the internal V_{DS} and the available gate bias voltage are reduced, lowering the drive current. However, the ringing can still exceed 3 V.

CONTROLLED EDGE RATE

The parameters that influence ground bounce are the inductances and resistances of the device, the capacitance of the load, and the edge rate. Of these, the only one that the chip manufacturer can directly control is the edge rate.

Turning on the output-driver transistor is equivalent to switching the charged load capacitor to ground. This can be represented by a step-voltage source in series with the capacitor (Figure 4a). Slowing down the rate that the output transistor can turn on changes the voltage source from a step to a ramp (Figure 4b). With a shallower slope, less energy is available for ringing, and the ground bounce amplitude is reduced.



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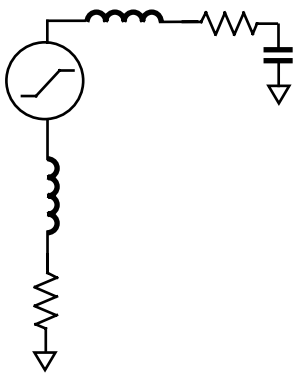
a. Equivalent circuit of an output driver transistor with a capacitive load



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b. Output driver circuit with slew-rate limiting

Figure 4. Schematic Circuitry

A SPICE simulation (Figure 5) illustrates the effect. The device without risetime control will have a very high charging current with a large di/dt: 2.1×10^7 A/s. Risetime control reduces the di/dt about 25%. This will result in a corresponding reduction in the voltage that can develop across the ground inductance.

Vantis has a proprietary technique that slows the edge rate of the output transistor, thereby reducing the amplitude of the ringing. Slowing down the fall time will add approximately one nanosecond to the output delay, but the system speed will still be greatly increased. On a high-capacitance load, a non-edge-rate-controlled device could ring for more than 25 ns. The additional delay required to allow for the ringing would be intolerable.

SYSTEM GROUND BOUNCE SOLUTIONS

There are some things that the system designer can do to reduce the ground bounce to a tolerable level.

1. Use Vantis MACH® devices that incorporate edge rate control. This is the first line of defense against ground bounce-related problems, and the most effective.
2. Use shorter lead packages. The bonding wires in a PLCC are 1/4 the length of the ground bonding wire in a DIP. The inductance is reduced proportionally. Any reduction in inductance will reduce the amplitude of the ringing.
3. Reduce capacitive loading. Capacitive loading in any system should be reduced as much as possible. This may involve consideration of the transmission line characteristics of the layout.
4. Limit the number of outputs switching simultaneously. If the load naturally has high-capacitance, such as a bus or memory board would, ground bounce can be reduced by limiting the number of outputs that can switch simultaneously in a single device. Many system designers consider 4 to be an acceptable upper limit.

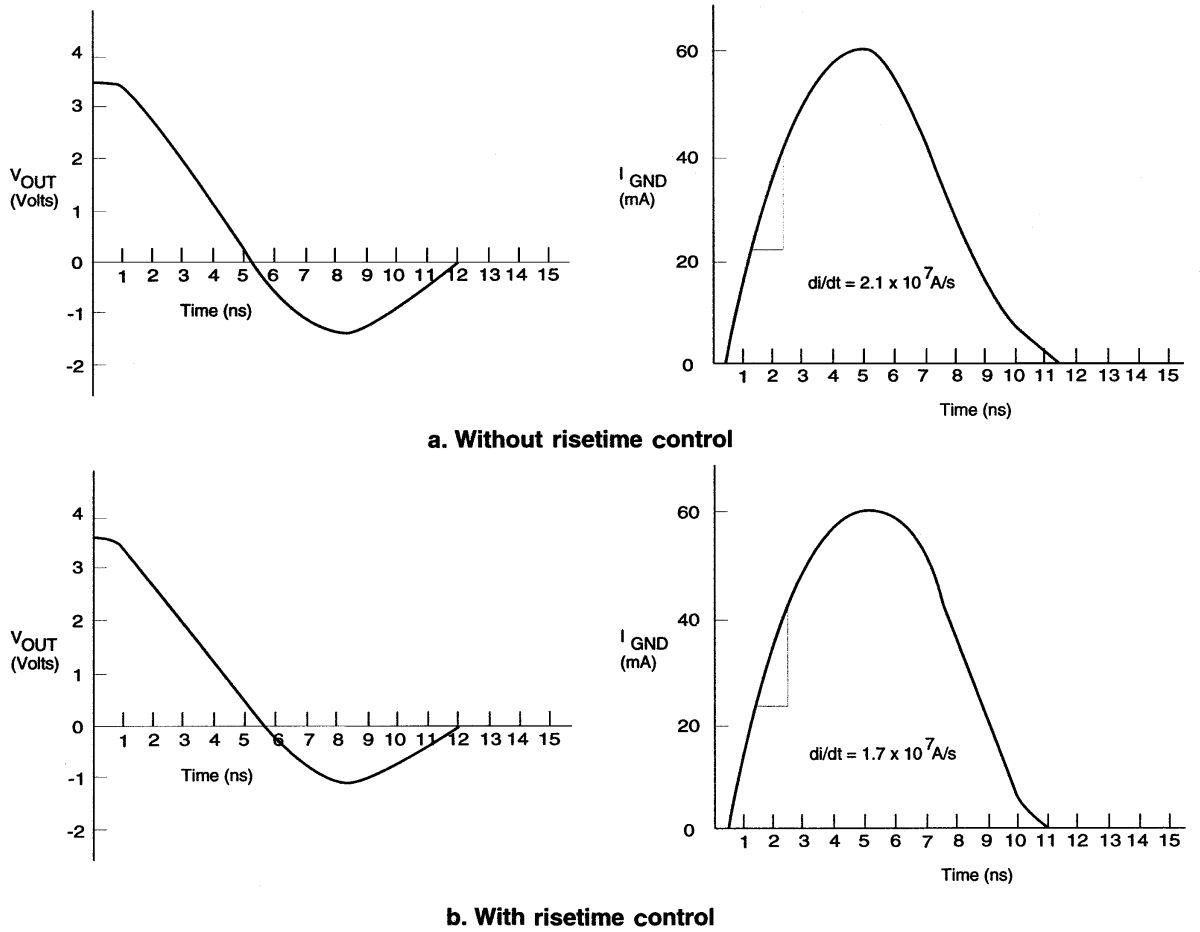

Figure 5. Effect of Risetime Control

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