VANTIS
BEYOND PERFORMANCE

Vantis Device Selector Guide

MACH® 4 FAMILY

Table 1. MACH 4 Devices[1]

Device	Package	Macrocells (PLD Gates)	I/Os	Dedicated Inputs	Output Enables	PT per Output (w/NO speed adder)	Flip-Flops	JTAG-ISP	Commercial		Ind'l [2]			I_{CC} mA (Static)
									t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[3] ns	t_{CO}[4] ns	
M4(LV)-32/32-7	44PLCC, 44TQFP, 48TQFP	32 (1,250)	32	2	32	Up to 20	32	Yes	7.5	111.1	10	5.5	5.5	25
M4(LV)-32/32-10									10	95.2	12	6	6.5	
M4(LV)-32/32-12									12	76.9	14	7	8	
M4(LV)-32/32-15									15	55.6	18	10	10	
M4(LV)-64/32-7	44PLCC, 44TQFP, 48TQFP	64 (2,500)	32	2	32	Up to 20	96	Yes	7.5	111.1	10	5.5	5.5	25
M4(LV)-64/32-10									10	95.2	12	6	6.5	
M4(LV)-64/32-12									12	76.9	14	7	8	
M4(LV)-64/32-15									15	55.6	18	10	10	
M4(LV)-96/48-7	100TQFP	96 (3,750)	48	8	48	Up to 20	144	Yes	7.5	111.1	10	5.5	5.5	50
M4(LV)-96/48-10									10	95.2	12	6	6.5	
M4(LV)-96/48-12									12	76.9	14	7	8	
M4(LV)-96/48-15									15	55.6	18	10	10	
M4(LV)-128N/64-7	84PLCC	128 (5,000)	64	6	64	Up to 20	192	No	7.5	111.1	10	5.5	5.5	70
M4(LV)-128N/64-10									10	95.2	12	6	6.5	
M4(LV)-128N/64-12									12	76.9	14	7	8	
M4(LV)-128N/64-15									15	55.6	18	10	10	
M4(LV)-128/64-7	100PQFP, 100TQFP	128 (5,000)	64	6	64	Up to 20	192	Yes	7.5	111.1	10	5.5	5.5	70
M4(LV)-128/64-10									10	95.2	12	6	6.5	
M4(LV)-128/64-12									12	76.9	14	7	8	
M4(LV)-128/64-15									15	55.6	18	10	10	
M4(LV)-192/96-7	144TQFP	192 (7,500)	96	16	96	Up to 20	288	Yes	7.5	111.1	10	5.5	5.5	85
M4(LV)-192/96-10									10	95.2	12	6	6.5	
M4(LV)-192/96-12									12	76.9	14	7	8	
M4(LV)-192/96-15									15	55.6	18	10	10	
M4(LV)-256/128-7	208PQFP 256BGA	256 (10,000)	128	14	128	Up to 20	384	Yes	7.5	111.1	10	5.5	5.5	100
M4(LV)-256/128-10									10	95.2	12	6	6.5	
M4(LV)-256/128-12									12	76.9	14	7	8	
M4(LV)-256/128-15									15	55.6	18	10	10	

Notes:

1. *M4 devices reflect a new nomenclature. A brief cross reference is provided below:*

OLD OPN	NEW M4 OPN	OLD OPN	NEW M4 OPN
MACH355--->	M4-96/96	MACH446--->	M4-128/64
MACH436--->	M4-128N/64	MACH466--->	M4-256/128

2. *MACH devices are dual-marked with both commercial and industrial speeds while CMOS PAL devices are marked separately.*
3. *Minimum setup time from input, I/O, or feedback to clock.*
4. *Maximum time from clock to output.*

Publication# **10253** Rev: **V**
Amendment/**0** Issue Date: **November 1998**

Table 2. MACH 4A Devices[1]

Device	Package	Macrocells	I/Os	Dedicated inputs	Output Enables	PT per Output	Flip Flops	JTAG-ISP	Commercial		Ind'l [2]		
									t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[3] ns	t_{CO}[4] ns
M4A(3,5)-32/32-50	44PLCC, 44TQFP, 48TQFP	32	32	2	32	Up to 20	32	Yes	5	182	7.5	3	4
M4A(3,5)-32/32-60									6	154	10	4	4.5
M4A(3,5)-32/32-7									7.5	125	10	5.5	5
M4A(3,5)-32/32-10									10	118	12	6	5.5
M4A(3,5)-32/32-12									12	95	14	7	6.5
M4A(3,5)-64/32-50	44PLCC 44TQFP 48TQFP	64	32	2	32	Up to 20	96	Yes	5	182	7.5	3	4
M4A(3,5)-64/32-60									6	154	10	4	4.5
M4A(3,5)-64/32-7									7.5	125	10	5.5	5
M4A(3,5)-64/32-10									10	118	12	6	5.5
M4A(3,5)-64/32-12									12	95	14	7	6.5
M4A(3,5)-96/48-50	100TQFP	96	48	8	48	Up to 20	144	Yes	5	182	7.5	3	4
M4A(3,5)-96/48-60									6	154	10	4	4.5
M4A(3,5)-96/48-7									7.5	125	10	5.5	5
M4A(3,5)-96/48-10									10	118	12	6	5.5
M4A(3,5)-96/48-12									12	95	14	7	6.5
M4A(3,5)-128/64-50	100TQFP, 100PQFP	128	64	6	64	Up to 20	192	Yes	5	182	7.5	3	4
M4A(3,5)-128/64-60									6	154	10	4	4.5
M4A(3,5)-128/64-7									7.5	125	10	5.5	5
M4A(3,5)-128/64-10									10	118	12	6	5.5
M4A(3,5)-128/64-12									12	95	14	7	6.5
M4A(3,5)-192/96-50	144TQFP	192	96	16	96	Up to 20	288	Yes	5	182	7.5	3	4
M4A(3,5)-192/96-60									6	154	10	4	4.5
M4A(3,5)-192/96-7									7.5	125	10	5.5	5
M4A(3,5)-192/96-10									10	118	12	6	5.5
M4A(3,5)-192/96-12									12	95	14	7	6.5
M4A(3,5)-256/128-50	208PQFP 256BGA	256	128	14	128	Up to 20	384	Yes	5	182	7.5	3	4
M4A(3,5)-256/128-60									6	154	10	4	4.5
M4A(3,5)-256/128-7									7.5	125	10	5.5	5
M4A(3,5)-256/128-10									10	118	12	6	5.5
M4A(3,5)-256/128-12									12	95	14	7	6.5

Notes:

1. *Advance Information*
2. *MACH devices are dual-marked with both commercial and industrial speeds while CMOS PAL devices are marked separately.*
3. *Minimum setup time from input, I/O, or feedback to clock.*
4. *Maximum time from clock to output.*

MACH 5 FAMILY

Table 3. MACH 5 Devices

Device	Package	Macrocells (PLD Gates)	I/Os	Dedicated Inputs	Output Enables	PT per Output	JTAG-ISP	Commercial		Ind'l[1]			
								t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
M5LV-128/68-5	100PQFP, 100TQFP	128 (5,000)	68	4	16	Up to 32	Yes	5.5	181.8	7.5	3	4.5	35
M5(LV)-128/68-7								7.5	125	10	4	6	
M5(LV)-128/68-10								10	100	12	5	7	
M5(LV)-128/68-12								12	83.3	15	6	8	
M5-128/68-15								15	62.5	20	8	10	
M5LV-128/74-5	100TQFP	128 (5,000)	74	4	16	Up to 32	Yes	5.5	181.8	7.5	3	4.5	35
M5LV-128/74-7								7.5	125	10	4	6	
M5LV-128/74-10								10	100	12	5	7	
M5LV-128/74-12								12	83.3	15	6	8	
M5LV-128/104-5	144PQFP, 144TQFP	128 (5,000)	104	4	16	Up to 32	Yes	5.5	181.8	7.5	3	4.5	35
M5(LV)-128/104-7								7.5	125	10	4	6	
M5(LV)-128/104-10								10	100	12	5	7	
M5(LV)-128/104-12								12	83.3	15	6	8	
M5-128/104-15								15	62.5	20	8	10	
M5LV-128/120-5	160PQFP	128 (5,000)	120	4	16	Up to 32	Yes	5.5	181.8	7.5	3	4.5	35
M5(LV)-128/120-7								7.5	125	10	4	6	
M5(LV)-128/120-10								10	100	12	5	7	
M5(LV)-128/120-12								12	83.3	15	6	8	
M5-128/120-15								15	62.5	20	8	10	
M5-192/68-7	100PQFP, 100TQFP	192 (7,500)	68	4	24	Up to 32	Yes	7.5	125	10	4	6	45
M5-192/68-10								10	100	12	5	7	
M5-192/68-12								12	83.3	15	6	8	
M5-192/68-15								15	62.5	20	8	10	
M5-192/104-7	144PQFP	192 (7,500)	104	4	24	Up to 32	Yes	7.5	125	10	4	6	45
M5-192/104-10								10	100	12	5	7	
M5-192/104-12								12	83.3	15	6	8	
M5-192/104-15								15	62.5	20	8	10	
M5-192/120-7	160PQFP	192 (7,500)	120	4	24	Up to 32	Yes	7.5	125	10	4	6	45
M5-192/120-10								10	100	12	5	7	
M5-192/120-12								12	83.3	15	6	8	
M5-192/120-15								15	62.5	20	8	10	
M5-192/160-7	208PQFP	192 (7,500)	160	4	24	Up to 32	Yes	7.5	125	10	4	6	45
M5-192/160-10								10	100	12	5	7	
M5-192/160-12								12	83.3	15	6	8	
M5-192/160-15								15	62.5	20	8	10	

Table 3. MACH 5 Devices (Continued)

Device	Package	Macrocells (PLD Gates)	I/Os	Dedicated Inputs	Output Enables	PT per Output	JTAG-ISP	Commercial		Ind'l[1]			
								t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
M5LV-256/68-5	100PQFP, 100TQFP	256 (10,000)	68	4	32	Up to 32	Yes	5.5	181.8	7.5	3	4.5	55
M5(LV)-256/68-7								7.5	125	10	4	6	
M5(LV)-256/68-10								10	100	12	5	7	
M5(LV)-256/68-12								12	83.3	15	6	8	
M5-256/68-15								15	62.5	20	8	10	
M5LV-256/74-5	100TQFP	256 (10,000)	74	4	32	Up to 32	Yes	5.5	181.8	7.5	3	4.5	55
M5LV-256/74-7								7.5	125	10	4	6	
M5LV-256/74-10								10	100	12	5	7	
M5LV-256/74-12								12	83.3	15	6	8	
M5LV-256/104-5	144PQFP, 144TQFP	256 (10,000)	104	4	32	Up to 32	Yes	5.5	181.8	7.5	3	4.5	55
M5(LV)-256/104-7								7.5	125	10	4	6	
M5(LV)-256/104-10								10	100	12	5	7	
M5(LV)-256/104-12								12	83.3	15	6	8	
M5-256/104-15								15	62.5	20	8	10	
M5LV-256/120-5	160PQFP	256 (10,000)	120	4	32	Up to 32	Yes	5.5	181.8	7.5	3	4.5	55
M5(LV)-256/120-7								7.5	125	10	4	6	
M5(LV)-256/120-10								10	100	12	5	7	
M5(LV)-256/120-12								12	83.3	15	6	8	
M5-256/120-15								15	62.5	20	8	10	
M5LV-256/160-5	208PQFP	256 (10,000)	160	4	32	Up to 32	Yes	5.5	181.8	7.5	3	4.5	55
M5(LV)-256/160-7								7.5	125	10	4	6	
M5(LV)-256/160-10								10	100	12	5	7	
M5(LV)-256/160-12								12	83.3	15	6	8	
M5-256/160-15								15	62.5	20	8	10	
M5(LV)-320/120-7	160PQFP	320 (12,500)	120	4	40	Up to 32	Yes	7.5	125	10	4	6	70
M5(LV)-320/120-10								10	100	12	5	7	
M5(LV)-320/120-12								12	83.3	15	6	8	
M5(LV)-320/120-15								15	62.5	20	8	10	
M5(LV)-320/160-7	208PQFP	320 (12,500)	160	4	40	Up to 32	Yes	7.5	125	10	4	6	70
M5(LV)-320/160-10								10	100	12	5	7	
M5(LV)-320/160-12								12	83.3	15	6	8	
M5(LV)-320/160-15								15	62.5	20	8	10	
M5(LV)-320/184-7	240PQFP	320 (12,500)	184	4	40	Up to 32	Yes	7.5	125	10	4	6	70
M5(LV)-320/184-10								10	100	12	5	7	
M5(LV)-320/184-12								12	83.3	15	6	8	
M5(LV)-320/184-15								15	62.5	20	8	10	
M5(LV)-320/192-7	256BGA	320 (12,500)	192	4	40	Up to 32	Yes	7.5	125	10	4	6	70
M5(LV)-320/192-10								10	100	12	5	7	
M5(LV)-320/192-12								12	83.3	15	6	8	
M5(LV)-320/192-15								15	62.5	20	8	10	

Table 3. MACH 5 Devices (Continued)

Device	Package	Macrocells (PLD Gates)	I/Os	Dedicated Inputs	Output Enables	PT per Output	JTAG-ISP	Commercial		Ind'l[1]			
								t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
M5(LV)-384/120-7	160PQFP	384 (15,000)	120	4	48	Up to 32	Yes	7.5	125	10	4	6	75
M5(LV)-384/120-10								10	100	12	5	7	
M5(LV)-384/120-12								12	83.3	15	6	8	
M5(LV)-384/120-15								15	62.5	20	8	10	
M5(LV)-384/160-7	208PQFP	384 (15,000)	160	4	48	Up to 32	Yes	7.5	125	10	4	6	75
M5(LV)-384/160-10								10	100	12	5	7	
M5(LV)-384/160-12								12	83.3	15	6	8	
M5(LV)-384/160-15								15	62.5	20	8	10	
M5(LV)-384/184-7	240PQFP	384 (15,000)	184	4	48	Up to 32	Yes	7.5	125	10	4	6	75
M5(LV)-384/184-10								10	100	12	5	7	
M5(LV)-384/184-12								12	83.3	15	6	8	
M5(LV)-384/184-15								15	62.5	20	8	10	
M5(LV)-384/192-7	256BGA	384 (15,000)	192	4	48	Up to 32	Yes	7.5	125	10	4	6	75
M5(LV)-384/192-10								10	100	12	5	7	
M5(LV)-384/192-12								12	83.3	15	6	8	
M5(LV)-384/192-15								15	62.5	20	8	10	
M5(LV)-512/120-7	160PQFP	512 (20,000)	120	4	64	Up to 32	Yes	7.5	125	10	4	6	100
M5(LV)-512/120-10								10	100	12	5	7	
M5(LV)-512/120-12								12	83.3	15	6	8	
M5(LV)-512/120-15								15	62.5	20	8	10	
M5(LV)-512/160-7	208PQFP	512 (20,000)	160	4	64	Up to 32	Yes	7.5	125	10	4	6	100
M5(LV)-512/160-10								10	100	12	5	7	
M5(LV)-512/160-12								12	83.3	15	6	8	
M5(LV)-512/160-15								15	62.5	20	8	10	
M5(LV)-512/184-7	240PQFP	512 (20,000)	184	4	64	Up to 32	Yes	7.5	125	10	4	6	100
M5(LV)-512/184-10								10	100	12	5	7	
M5(LV)-512/184-12								12	83.3	15	6	8	
M5(LV)-512/184-15								15	62.5	20	8	10	
M5(LV)-512/192-7	256BGA	512 (20,000)	192	4	64	Up to 32	Yes	7.5	125	10	4	6	100
M5(LV)-512/192-10								10	100	12	5	7	
M5(LV)-512/192-12								12	83.3	15	6	8	
M5(LV)-512/192-15								15	62.5	20	8	10	
M5(LV)-512/256-7	352BGA	512 (20,000)	256	4	64	Up to 32	Yes	7.5	125	10	4	6	100
M5(LV)-512/256-10								10	100	12	5	7	
M5(LV)-512/256-12								12	83.3	15	6	8	
M5(LV)-512/256-15								15	62.5	20	8	10	

Notes:

1. *MACH devices are dual-marked with both commercial and industrial speeds while CMOS PAL devices are marked separately.*
2. *Minimum setup time from input, I/O, or feedback to clock.*
3. *Maximum time from clock to output.*

Table 4. MACH 5A Devices[1]

Device	Package	Macrocells	I/Os	Dedicated Inputs	Output Enables	PT per Output	JTAG-ISP	Commercial		Ind'l[2]		
								t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[3] ns	t_{CO}[4] ns
M5A(3,5)-128/68-5	100PQFP	128	68	4	16	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-128/68-7								7.5	125	10	4	6
M5A(3,5)-128/68-10								10	100	12	5	7
M5A(3,5)-128/68-12								12	83.3	15	6	8
M5A(3,5)-128/74-5	100TQFP	128	74	4	16	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-128/74-7								7.5	125	10	4	6
M5A(3,5)-128/74-10								10	100	12	5	7
M5A(3,5)-128/74-12								12	83.3	15	6	8
M5A(3,5)-128/104-5	144TQFP	128	104	4	16	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-128/104-7								7.5	125	10	4	6
M5A(3,5)-128/104-10								10	100	12	5	7
M5A(3,5)-128/104-12								12	83.3	15	6	8
M5A(3,5)-128/120-5	160PQFP	128	120	4	16	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-128/120-7								7.5	125	10	4	6
M5A(3,5)-128/120-10								10	100	12	5	7
M5A(3,5)-128/120-12								12	83.3	15	6	8
M5A(3,5)-192/68-5	100PQFP	192	68	4	24	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-192/68-7								7.5	125	10	4	6
M5A(3,5)-192/68-10								10	100	12	5	7
M5A(3,5)-192/68-12								12	83.3	15	6	8
M5A(3,5)-192/74-5	100TQFP	192	74	4	24	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-192/74-7								7.5	125	10	4	6
M5A(3,5)-192/74-10								10	100	12	5	7
M5A(3,5)-192/74-12								12	83.3	15	6	8
M5A(3,5)-192/104-5	144TQFP	192	104	4	24	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-192/104-7								7.5	125	10	4	6
M5A(3,5)-192/104-10								10	100	12	5	7
M5A(3,5)-192/104-12								12	83.3	15	6	8
M5A(3,5)-192/120-5	160PQFP	192	120	4	24	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-192/120-7								7.5	125	10	4	6
M5A(3,5)-192/120-10								10	100	12	5	7
M5A(3,5)-192/120-12								12	83.3	15	6	8

Table 4. MACH 5A Devices[1] (Continued)

Device	Package	Macrocells	I/Os	Dedicated Inputs	Output Enables	PT per Output	JTAG-ISP	Commercial		Ind'l[2]		
								t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[3] ns	t_{CO}[4] ns
M5A(3,5)-256/68-5	100PQFP	256	68	4	32	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-256/68-7								7.5	125	10	4	6
M5A(3,5)-256/68-10								10	100	12	5	7
M5A(3,5)-256/68-12								12	83.3	15	6	8
M5A(3,5)-256/74-5	100TQFP	256	74	4	32	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-256/74-7								7.5	125	10	4	6
M5A(3,5)-256/74-10								10	100	12	5	7
M5A(3,5)-256/74-12								12	83.3	15	6	8
M5A(3,5)-256/104-5	144TQFP	256	104	4	32	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-256/104-7								7.5	125	10	4	6
M5A(3,5)-256/104-10								10	100	12	5	7
M5A(3,5)-256/104-12								12	83.3	15	6	8
M5A(3,5)-256/120-5	160PQFP	256	120	4	32	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-256/120-7								7.5	125	10	4	6
M5A(3,5)-256/120-10								10	100	12	5	7
M5A(3,5)-256/120-12								12	83.3	15	6	8
M5A(3,5)-256/160-5	208PQFP	256	160	4	32	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-256/160-7								7.5	125	10	4	6
M5A(3,5)-256/160-10								10	100	12	5	7
M5A(3,5)-256/160-12								12	83.3	15	6	8
M5A3-320/120-5	160PQFP	320	120	4	40	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A3-320/120-6								6.5	166.7	10	3	5
M5A3-320/120-7								7.5	125	10	4	6
M5A3-320/120-10								10	100	12	5	7
M5A3-320/120-12								12	83.3	15	6	8
M5A3-320/160-5	208PQFP	320	160	4	40	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A3-320/160-6								6.5	166.7	10	3	5
M5A3-320/160-7								7.5	125	10	4	6
M5A3-320/160-10								10	100	12	5	7
M5A3-320/160-12								12	83.3	15	6	8
M5A3-320/192-5	256BGA	320	192	4	40	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A3-320/192-6								6.5	166.7	10	3	5
M5A3-320/192-7								7.5	125	10	4	6
M5A3-320/192-10								10	100	12	5	7
M5A3-320/192-12								12	83.3	15	6	8

Table 4. MACH 5A Devices[1] (Continued)

Device	Package	Macrocells	I/Os	Dedicated Inputs	Output Enables	PT per Output	JTAG-ISP	Commercial		Ind'l[2]		
								t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[3] ns	t_{CO}[4] ns
M5A3-384/120-5	160PQFP	384	120	4	48	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A3-384/120-6								6.5	166.7	10	3	5
M5A3-384/120-7								7.5	125	10	4	6
M5A3-384/120-10								10	100	12	5	7
M5A3-384/120-12								12	83.3	15	6	8
M5A3-384/160-5	208PQFP	384	160	4	48	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A3-384/160-6								6.5	166.7	10	3	5
M5A3-384/160-7								7.5	125	10	4	6
M5A3-384/160-10								10	100	12	5	7
M5A3-384/160-12								12	83.3	15	6	8
M5A3-384/192-5	256BGA	384	192	4	48	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A3-384/192-6								6.5	166.7	10	3	5
M5A3-384/192-7								7.5	125	10	4	6
M5A3-384/192-10								10	100	12	5	7
M5A3-384/192-12								12	83.3	15	6	8
M5A3-512/120-5	160PQFP	512	120	4	64	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A3-512/120-6								6.5	166.7	10	3	5
M5A3-512/120-7								7.5	125	10	4	6
M5A3-512/120-10								10	100	12	5	7
M5A3-512/120-12								12	83.3	15	6	8
M5A3-512/160-5	208PQFP	512	160	4	64	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A3-512/160-6								6.5	166.7	10	3	5
M5A3-512/160-7								7.5	125	10	4	6
M5A3-512/160-10								10	100	12	5	7
M5A3-512/160-12								12	83.3	15	6	8
M5A3-512/192-5	256BGA	512	192	4	64	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A3-512/192-6								6.5	166.7	10	3	5
M5A3-512/192-7								7.5	125	10	4	6
M5A3-512/192-10								10	100	12	5	7
M5A3-512/192-12								12	83.3	15	6	8
M5A3-512/256-5	352BGA	512	256	4	64	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A3-512/256-6								6.5	166.7	10	3	5
M5A3-512/256-7								7.5	125	10	4	6
M5A3-512/256-10								10	100	12	5	7
M5A3-512/256-12								12	83.3	15	6	8

Notes:

1. *Advance Information*
2. *MACH devices are dual-marked with both commercial and industrial speeds while CMOS PAL devices are marked separately.*
3. *Minimum setup time from input, I/O, or feedback to clock.*
4. *Maximum time from clock to output.*

MACH 1 & 2 FAMILIES

Table 5. MACH 1 Devices

Device	Package	Macrocells (PLD Gates)	I/Os	Dedicated Inputs	Output Enables	PT per Output (w/ NO speed adder)	JTAG-ISP	Commercial		Ind'l[1]				
								t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
MACH111-5	44PLCC, 44TQFP	32 (1250)	32	6	8	Up to 12	No	5	182	7.5	3.5	3.5	40
MACH111-7								7.5	133	10	5.5	5	
MACH111-10								10	100	12	6.5	6	
MACH111-12								12	76.9	14	7	8	
MACH111-15								15	66.6	18	10	10	
MACH131-5	84PLCC	64 (2500)	64	6	16	Up to 12	No	5.5	182	7.5	3.0	4	75
MACH131-7								7.5	133	10	5.5	5	
MACH131-10								10	100	12	6.5	6	
MACH131-12								12	76.9	14	7	8	
MACH131-15								15	66.6	18	10	10	

Table 6. MACH 2 Devices

Device	Package	Macrocells (PLD Gates)	I/Os	Dedicated Inputs	Output Enables	PT per Output (w/ NO speed adder)	JTAG-ISP	Commercial		Ind'l[1]				
								t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
MACH211-7	44PLCC, 44TQFP	64 (2500)	32	6	8	Up to 16	No	7.5	133	10	5.5	4.5	40
MACH211-10								10	100	12	6.5	6	
MACH211-12								12	83.3	14	7	8	
MACH211-15								15	66.6	18	10	10	
MACH221-7	68PLCC	96 (3750)	48	8	16	Up to 16	No	7.5	133	10	5.5	5	70
MACH221-10								10	100	12	6.5	6	
MACH221-12								12	83.3	14	7	8	
MACH221-15								15	66.6	18	10	10	
MACH231-6	84PLCC	128 (5000)	64	6	16	Up to 16	No	6	166	-	5	4	135
MACH231-7								7.5	133	-	5.5	5	
MACH231-10								10	100	12	6.5	6.5	
MACH231-12								12	83.3	14	7	8	
MACH231-15								15	66.6	18	10	10	

Notes:

1. *MACH devices are dual-marked with both commercial and industrial speeds while CMOS PAL devices are marked separately.*
2. *Minimum setup time from input, I/O, or feedback to clock.*
3. *Maximum time from clock to output.*

Table 7. MACH 1SP Devices

Device	Package	Macrocells (PLD Gates)	I/Os	Dedicated Inputs	Output Enables	PT per Output (w/ NO speed adder)	JTAG-ISP	Commercial		Ind'l[1]			I_{CC} mA (Static)
								t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	
MACH111SP-5	44PLCC, 44TQFP	32 (1250)	32	2	8	Up to 12	Yes	5	182	7.5	3.5	3.5	40
MACH111SP-7								7.5	133	10	5.5	5	
MACH111SP-10								10	100	12	6.5	6	
MACH111SP-12								12	76.9	14	7	8	
MACH111SP-15								15	66.6	18	10	10	
MACH131SP-5	100PQFP, 100TQFP	64 (2500)	64	6	16	Up to 12	Yes	5.5	182	7.5	3.0	4	75
MACH131SP-7								7.5	133	10	5.5	5	
MACH131SP-10								10	100	12	6.5	6	
MACH131SP-12								12	76.9	14	7	8	
MACH131SP-15								15	66.6	18	10	10	

Table 8. MACH 2SP Devices

Device	Package	Macrocells (PLD Gates)	I/Os	Dedicated Inputs	Output Enables	PT per Output (w/ NO speed adder)	JTAG-ISP	Commercial		Ind'l[1]			I_{CC} mA (Static)
								t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	
MACH211SP-6	44PLCC, 44TQFP	64 (2500)	32	2	8	Up to 16	Yes	6	166	-	5	4	40
MACH211SP-7								7.5	133	10	5.5	4.5	
MACH211SP-10								10	100	12	6.5	6	
MACH211SP-12								12	83.3	14	7	8	
MACH211SP-15								15	66.6	18	10	10	
MACH221SP-7	100PQFP	96 (3750)	48	8	16	Up to 16	Yes	7.5	133	10	5.5	5	70
MACH221SP-10								10	100	12	6.5	6	
MACH221SP-12								12	83.3	14	7	8	
MACH221SP-15								15	66.6	18	10	10	
MACH231SP-10	100PQFP, 100TQFP	128 (5000)	64	6	16	Up to 16	Yes	10	100	12	6.5	6.5	80
MACH231SP-12								12	83.3	14	7	8	
MACH231SP-15								15	66.6	18	10	10	

Notes:

1. *MACH devices are dual-marked with both commercial and industrial speeds while CMOS PAL devices are marked separately.*
2. *Minimum setup time from input, I/O, or feedback to clock.*
3. *Maximum time from clock to output.*

The MACH110, MACH120, MACH130, MACH210, MACHLV210, MACH215, MACH220 and MACH230 devices are not listed above and are not recommended for new designs. However, they are still supported by Vantis. For technical or sales support, please call your local Vantis sales office or visit our Web site at www.vantis.com for more information.

VF1 FAMILY

Table 9. VF1 Devices

Device	Usable Gates	VGB Array Size	Package	I/Os	Global Clock Pins	RAM Bits	VGB FlipFlops	I/O Flip-Flops	JTAG	Commercial Speed Grades	Industrial Speed Grades
VF1012	12,000	14x14	144TQFP	108	4	3584	784	336	Yes	-1, -2	-1
			160PQFP	124	4	3584	784	336	Yes	-1, -2	-1
			208PQFP	164	4	3584	784	336	Yes	-1, -2	-1
			256BGA	168	4	3584	784	336	Yes	-1, -2	-1
VF1020	20,000	18x18	144TQFP	108	4	4608	1296	432	Yes	-1, -2	-1
			160PQFP	124	4	4608	1296	432	Yes	-1, -2	-1
			208PQFP	164	4	4608	1296	432	Yes	-1, -2	-1
			256BGA	204	4	4608	1296	432	Yes	-1, -2	-1
VF1025	25,000	20x20	208PQFP	164	4	5120	1600	480	Yes	-1, -2	-1
			256BGA	204	4	5120	1600	480	Yes	-1, -2	-1
			352BGA	240	4	5120	1600	480	Yes	-1, -2	-1
VF1036	36,000	24x24	208PQFP	164	4	6144	2304	576	Yes	-1, -2	-1
			256BGA	204	4	6144	2304	576	Yes	-1, -2	-1
			352BGA	288	4	6144	2304	576	Yes	-1, -2	-1

CMOS PAL® FAMILY

Table 10. Universal CMOS 16V8 PAL Devices

Device	Package	I/Os	Dedicated Inputs	PT per Output	Feature	Commercial		Ind'l[1]			
						t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
PALCE16V8H-5	20J	8	10	8	Half Power CMOS PAL Device	5	166	–	3	4	125
PALCE16V8H-7	20P, S, J					7.5	125	–	5	5	115
PALCE16V8H-10						10	71.4	10	7.5	7.5	115
PALCE16V8H-15						15	50	15	12	10	90
PALCE16V8H-25						25	40	25	13	11	90
PALCE16V8Q-10	20P, J	8	10	8	Quarter Power CMOS PAL Device	10	71.4	–	7.5	7.5	55
PALCE16V8Q-15						15	50	15	12	10	55
PALCE16V8Q-20						–	–	20	13	11	65
PALCE16V8Q-25						25	40	25	15	12	55

Table 11. Universal CMOS 20V8 PAL Devices

Device	Package	I/Os	Dedicated Inputs	PT per Output	Feature	Commercial		Ind'l[1]			
						t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
PALCE20V8H-5	28J	8	14	8	Half Power CMOS PAL Device	5	166	–	3	4	125
PALCE20V8H-7	24P, 28J					7.5	125	–	5	5	115
PALCE20V8H-10						10	71.4	–	7.5	7.5	115
PALCE20V8H-15						15	50	15	12	10	90
PALCE20V8H-25						25	40	25	15	12	90
PALCE20V8Q-10	24P, 28 J	8	14	8	Quarter Power CMOS PAL Device	10	71.4	–	7.5	7.5	55
PALCE20V8Q-15						15	50	–	12	10	55
PALCE20V8Q-20						–	–	20	13	11	65
PALCE20V8Q-25						25	40	25	15	12	55

Notes:

1. *MACH devices are dual-marked with both commercial and industrial speeds while CMOS PAL devices are marked separately.*
2. *Minimum setup time from input, I/O, or feedback to clock.*
3. *Maximum time from clock to output.*

Table 12. Universal CMOS 22V10 PAL Devices

Device	Package	I/Os	Dedicated Inputs	PT per Output	Feature	Commercial		Ind'l[1]			
						t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
PALCE22V10H-5	28J	10	12	8 to 16	Half Power Varied Prod Term Distribution Bus-Friendly ™	5	150	–	3	4	125
PALCE22V10H-7	24P, 28 J					7.5	133	–	4.5	4.5	115
PALCE22V10H-10	24P, S, 28J					10	110	10	6	6	120
PALCE22V10H-15	24P, S, 28J					15	58.8	15	10	10	90
PALCE22V10H-20	24P, 28J					–	–	20	12	12	100
PALCE22V10H-25	24P, S, 28J					25	35.7	25	15	15	90
PALCE22V10Q-10	24P, 28J	10	12	8 to 16	Quarter Power Bus-Friendly	10	110	–	6	6	55
PALCE22V10Q-15						15	58.8	–	10	10	55
PALCE22V10Q-25						25	35.7	–	15	15	55

Table 13. Universal CMOS 24V10 PAL Devices

Device	Package	I/Os	Dedicated Inputs	PT per Output	Feature	Commercial		Ind'l[1]			
						t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
PALCE24V10H-15	28P, J	10	12	8 to 16	CMOS PAL Device	15	66	–	10	10	115
PALCE24V10H-25						25	50	–	12	12	115

Table 14. Universal CMOS 26V12 PAL Devices

Device	Package	I/Os	Dedicated Inputs	PT per Output	Feature	Commercial		Ind'l[1]			
						t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
PALCE26V12H-7	28J	12	14	8 to 16	Adv. 22V10 M/C Bus-Friendly	7.5	125	–	3.5	6	115
PALCE26V12H-10	28P, J					10	105	10	5	9	115
PALCE26V12H-15						15	58.8	15	10	10	105
PALCE26V12H-20						20	43	20	13	12	105

Notes:

1. *MACH devices are dual-marked with both commercial and industrial speeds while CMOS PAL devices are marked separately.*
2. *Minimum setup time from input, I/O, or feedback to clock.*
3. *Maximum time from clock to output.*

Table 15. Universal CMOS 29M16 PAL Devices

Device	Package	I/Os	Dedicated Inputs	PT per Output	Feature	Commercial		Ind'l[1]			
						t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
PALCE29M16H-25	24P, 28J	16	5	8 to 16	Adv. Macrocell	25	33.3	–	15	15	100

Table 16. Zero Power CMOS PAL Devices

Family	Device	Package	I/Os	Dedicated Inputs	PT per Output	Feature	Commercial		Ind'l[1]			
							t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
16V8	PALCE16V8Z-12	20P, J	8	10	8	Zero Power CMOS PAL Device	–	–	12	8	8	0.03
	PALCE16V8Z-15						–	–	15	10	10	0.015
	PALCE16V8Z-25	20P, S, J					25	50	25	20	10	0.015
22V10	PALCE22V10Z-15	24P, 28J	10	12	8 to 16	Zero Power	–	–	15	10	10	0.03
	PALCE22V10Z-25	24P, S, 28J					25	35.7	25	15	15	0.03

Table 17. 3.3-V Low Voltage CMOS PAL Devices

Family	Device	Package	I/Os	Dedicated Inputs	PT per Output	Feature	Commercial		Ind'l[1]			
							t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
16V8	PALLV16V8-10	20P, S, J	8	10	8	3.3V	10	83.3	–	7	7	55
	PALLV16V8Z-20	20P, J				3.3V, Zero Power	–	–	20	15	10	0.03
22V10	PALLV22V10-7	28J	10	12	8 to 16	3.3V	7.5	133	–	4.5	5.5	75
	PALLV22V10-10	24P, 28J					10	110	–	5.5	6.5	60
	PALLV22V10-15						15	58.8	15	10	10	60
	PALLV22V10Z-25	24P, 28J				3.3V, Zero Power	–	–	25	15	15	0.03

Table 18. Asynchronous Universal PAL Devices

Family	Device	Package	I/Os	Dedicated Inputs	PT per Output	Feature	Commercial		Ind'l[1]			
							t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
610	PALCE610H-15	24P, 28J	16	4	8	J-K F/F Programmable CLK	15	76.1	–	12	8	90
	PALCE610H-25						25	40	–	15	12	90
20RA10	PALCE20RA10H-7	28J 24P, 28J	10	10	4	Programmable CLK	7.5	100[4]	7.5	2.5	7.5	100
	PALCE20RA10H-10						10	76.9[4]	10	3	10	100
	PALCE20RA10H-15						15	52.6[4]	15	4	15	100
	PALCE20RA10H-20						20	37[4]	20	4	20	90
29MA16	PALCE29MA16H-25	24P, 28J	16	5	4 to 12	Prog. CLK, Adv M/C	25	33.3	–	15	15	100

Notes:

1. *MACH devices are dual-marked with both commercial and industrial speeds while CMOS PAL devices are marked separately.*
2. *Minimum setup time from input, I/O, or feedback to clock.*
3. *Maximum time from clock to output.*
4. *Specified as f_{MAX} (External Feedback)*

This databook contains the PAL device information for the PALCE16V8, PALLV16V8, PALCE20V8, PALCE22V10, and PALLV22V10. For information on other PAL devices, please refer to the datasheets on our Web site at www.vantis.com.