The TPIC1321L is a monolithic gate-protected logic-level power DMOS array that consists of six electrically isolated N-channel enhancement-mode DMOS transistors configured as 3-half H-bridges. Each transistor features integrated high-current zener diodes (ZCXa and ZCXb) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-kΩ resistor.

The TPIC1321L is offered in a 24-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature of –40°C to 125°C.

NOTE A: For correct operation, no terminal may be taken below GND.
absolute maximum ratings over operating case temperature range (unless otherwise noted)†

- Drain-to-source voltage, $V_{DS}$: 60 V
- Output-to-GND voltage: 60 V
- Drain-to-GND voltage: 100 V
- SOURCE4, SOURCE6-to-GND voltage: 60 V
- Gate-to-source voltage range, $V_{GS}$: −9 V to 18 V
- Continuous drain current, each output, $T_C = 25^\circ C$: 1.25 A
- Continuous source-to-drain diode current, $T_C = 25^\circ C$: 1.25 A
- Pulsed drain current, each output, $I_{max}$, $T_C = 25^\circ C$ (see Note 1 and Figure 15): 4 A
- Continuous gate-to-source zener-diode current, $T_C = 25^\circ C$: ±50 mA
- Pulsed gate-to-source zener-diode current, $T_C = 25^\circ C$: ±500 mA
- Single-pulse avalanche energy, $E_{AS}$, $T_C = 25^\circ C$ (see Figures 4 and 16): 96 mJ
- Continuous total dissipation, $T_C = 25^\circ C$ (see Figure 15): 1.39 W
- Operating virtual junction temperature range, $T_J$: −40°C to 150°C
- Operating case temperature range, $T_C$: −40°C to 125°C
- Storage temperature range: −65°C to 150°C
- Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%
### Electrical Characteristics, $T_C = 25^\circ C$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{(BR)DSX}$ Drain-to-source breakdown voltage</td>
<td>$I_D = 250 \mu A$, $V_{GS} = 0$</td>
<td>60</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS(th)}$ Gate-to-source threshold voltage</td>
<td>$I_D = 1 \ mA$, $V_{DS} = V_{GS}$, See Figure 5</td>
<td>1.5</td>
<td>1.75</td>
<td>2.2</td>
<td>V</td>
</tr>
<tr>
<td>$V_{(BR)GS}$ Source-to-gate breakdown voltage</td>
<td>$I_{SG} = 250 \mu A$</td>
<td>18</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{(BR)}$ Reverse drain-to-GND breakdown voltage (across D1, D2, D3, D4, D5)</td>
<td>$I_D = 250 \mu A$, $V_{GS} = 0$</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{(BR)DS(on)}$ Drain-to-source on-state voltage</td>
<td>$I_D = 1.25 A$, $V_{GS} = 5 V$, See Notes 2 and 3</td>
<td>0.44</td>
<td>0.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{F(SD)}$ Forward on-state voltage, source-to-drain</td>
<td>$I_S = 1.25 A$, $V_{GS} = 0 (Z1 - Z6)$, See Notes 2 and 3 and Figure 12</td>
<td>0.9</td>
<td>1.1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{F}$ Forward on-state voltage, GND-to-drain</td>
<td>$I_D = 1.25 A (D1 - D5)$, See Notes 2 and 3</td>
<td>4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_DSS$ Zero-gate-voltage drain current</td>
<td>$V_{DS} = 48 V$, $V_{GS} = 0$</td>
<td>0.05</td>
<td>1</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{GSSF}$ Forward-gate current, drain short circuited to source</td>
<td>$V_{GS} = 15 V$, $V_{DS} = 0$</td>
<td>20</td>
<td>200</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>$I_{GSSR}$ Reverse-gate current, drain short circuited to source</td>
<td>$V_{SG} = 5 V$, $V_{DS} = 0$</td>
<td>10</td>
<td>100</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>$I_{ilkg}$ Leakage current, drain-to-GND</td>
<td>$V_{DGND} = 48 V$, $V_{GS} = 0$</td>
<td>0.05</td>
<td>1</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$r_{DS(on)}$ Static drain-to-source on-state resistance</td>
<td>$V_{GS} = 5 V$, $V_{DS} = 48 V$, $I_D = 625 mA$, See Notes 2 and 3 and Figure 9</td>
<td>0.35</td>
<td>0.4</td>
<td>0.57</td>
<td>0.6</td>
</tr>
<tr>
<td>$g_{fs}$ Forward transconductance</td>
<td>$V_{DS} = 15 V$, $V_{GS} = 0$, See Notes 2 and 3 and Figure 9</td>
<td>1.6</td>
<td>1.74</td>
<td></td>
<td>S</td>
</tr>
<tr>
<td>$C_{iss}$ Short-circuit input capacitance, common source</td>
<td>$V_{DS} = 25 V$, $V_{GS} = 0$, $f = 1 MHz$, See Figure 11</td>
<td>200</td>
<td>250</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$C_{oss}$ Short-circuit output capacitance, common source</td>
<td>$V_{DS} = 25 V$, $V_{GS} = 0$, $f = 1 MHz$, See Figure 11</td>
<td>175</td>
<td>220</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$C_{rss}$ Short-circuit reverse-transfer capacitance, common source</td>
<td>$V_{DS} = 25 V$, $V_{GS} = 0$, $f = 1 MHz$, See Figure 11</td>
<td>40</td>
<td>75</td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

**NOTES:**

2. Technique should limit $T_J - T_C$ to $10^\circ C$ maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

### Source-to-drain and GND-to-drain Diode Characteristics, $T_C = 25^\circ C$

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{fr}$</td>
<td>Reverse-recovery time</td>
<td>$I_S = 625 \ mA$, $V_{GS} = 0$, $dV/dt = 100 \ A/\mu s$, See Figures 1 and 14</td>
<td>45</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_{RR}$</td>
<td>Total diode charge</td>
<td>$V_{DS} = 48 V$, $dI/dt = 100 \ A/\mu s$, Z1, Z2, and Z3</td>
<td>50</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
resistive-load switching characteristics, $T_C = 25^\circ C$

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_d(on)$</td>
<td>Turn-on delay time</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_d(off)$</td>
<td>Turn-off delay time</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_r$</td>
<td>Rise time</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_f$</td>
<td>Fall time</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_g$</td>
<td>Total gate charge</td>
<td></td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>$Q_{gs(th)}$</td>
<td>Threshold gate-to-source charge</td>
<td></td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>$Q_{gd}$</td>
<td>Gate-to-drain charge</td>
<td></td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>$L_D$</td>
<td>Internal drain inductance</td>
<td>5</td>
<td></td>
<td></td>
<td>nH</td>
</tr>
<tr>
<td>$L_S$</td>
<td>Internal source inductance</td>
<td>5</td>
<td></td>
<td></td>
<td>nH</td>
</tr>
<tr>
<td>$R_g$</td>
<td>Internal gate resistance</td>
<td>0.25</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
</tbody>
</table>

thermal resistance

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\theta JA}$</td>
<td>Junction-to-ambient thermal resistance</td>
<td>90</td>
<td></td>
<td></td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{\theta JB}$</td>
<td>Junction-to-board thermal resistance</td>
<td>44.5</td>
<td></td>
<td></td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{\theta JP}$</td>
<td>Junction-to-pin thermal resistance</td>
<td>28</td>
<td></td>
<td></td>
<td>°C/W</td>
</tr>
</tbody>
</table>

NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink.
5. Package mounted on a 24 in², 4-layer FR4 printed-circuit board.
6. Package mounted in intimate contact with infinite heatsink.
7. All outputs with equal power.
PARAMETER MEASUREMENT INFORMATION

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms
PARAMETER MEASUREMENT INFORMATION

Figure 3. Gate-Charge Test Circuit and Voltage Waveform

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

NOTES:  
A. The pulse generator has the following characteristics: $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$, $Z_O = 50 \Omega$.  
B. Input pulse duration ($t_w$) is increased until peak current $I_{AS} = 4 \text{ A}$.  

Energy test level is defined as  
$$E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 96 \text{ mJ}.$$
TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

$$V_{GS(th)} - \text{Gate-to-Source Threshold Voltage} - \text{V}$$

$$V_{DS} = V_{GS}$$

- $$I_D = 1 \text{ mA}$$
- $$I_D = 100 \mu\text{A}$$

JUNCTION TEMPERATURE - $^\circ\text{C}$

Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

$$r_{DS(on)} - \text{Static Drain-to-Source On-State Resistance} - \Omega$$

$$V_{GS} = 4.5 \text{ V}$$

$$V_{GS} = 5 \text{ V}$$

Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

$$r_{DS(on)} - \text{Static Drain-to-Source On-State Resistance} - \Omega$$

$$V_{GS} = 4.5 \text{ V}$$

$$V_{GS} = 5 \text{ V}$$

$$T_J = 25^\circ\text{C}$$

Figure 7

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

$$I_D - \text{Drain Current} - \text{A}$$

$$V_{DS} - \text{Drain-to-Source Voltage} - \text{V}$$

$$\Delta V_{GS} = 0.2 \text{ V}$$

$$V_{GS} = 3 \text{ V}$$

$$T_J = 25^\circ\text{C}$$

Figure 8
TPIC1321L
3-HALF H-BRIDGE GATE-PROTECTED LOGIC-LEVEL
POWER DMOS ARRAY
SLIS042 – NOVEMBER 1994

TYPICAL CHARACTERISTICS

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

- Total Number of Units = 1596
- \( V_{DS} = 15 \text{ V} \)
- \( I_D = 625 \text{ mA} \)
- \( T_J = 25^\circ \text{C} \)

\( g_{fs} \) – Forward Transconductance – S

<table>
<thead>
<tr>
<th>Percentage of Units – %</th>
<th>( g_{fs} ) – Forward Transconductance – S</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>1.800</td>
</tr>
<tr>
<td>20</td>
<td>1.820</td>
</tr>
<tr>
<td>15</td>
<td>1.840</td>
</tr>
<tr>
<td>10</td>
<td>1.860</td>
</tr>
<tr>
<td>5</td>
<td>1.880</td>
</tr>
<tr>
<td>5</td>
<td>1.900</td>
</tr>
<tr>
<td>5</td>
<td>1.920</td>
</tr>
<tr>
<td>5</td>
<td>1.940</td>
</tr>
<tr>
<td>5</td>
<td>1.960</td>
</tr>
<tr>
<td>1</td>
<td>1.980</td>
</tr>
<tr>
<td>1</td>
<td>2.000</td>
</tr>
</tbody>
</table>

\( g_{fs} \) – Forward Transconductance – S

Figure 9

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

\( I_D \) – Drain Current – A

\( V_GS \) – Gate-to-Source Voltage – V

- \( T_J = -40^\circ \text{C} \)
- \( T_J = 25^\circ \text{C} \)
- \( T_J = 75^\circ \text{C} \)
- \( T_J = 125^\circ \text{C} \)
- \( T_J = 150^\circ \text{C} \)

Figure 10

CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

\( V_GS = 0 \)

\( f = 1 \text{ MHz} \)

\( T_J = 25^\circ \text{C} \)

\( C_{iss}(0) = 307 \text{ pF} \)

\( C_{oss}(0) = 437 \text{ pF} \)

\( C_{rss}(0) = 141 \text{ pF} \)

\( V_{DS} \) – Drain-to-Source Voltage – V

\( C_{iss} \)

\( C_{oss} \)

\( C_{rss} \)

Figure 11

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

\( I_{SD} \) – Source-to-Drain Diode Current – A

\( V_{SD} \) – Source-to-Drain Voltage – V

- \( T_J = 25^\circ \text{C} \)
- \( T_J = -40^\circ \text{C} \)
- \( T_J = 75^\circ \text{C} \)
- \( T_J = 150^\circ \text{C} \)
- \( T_J = 125^\circ \text{C} \)

Figure 12
TYPICAL CHARACTERISTICS

DRAIN-TO-SOURCE VOLTAGE AND GATE-TO-SOURCE VOLTAGE

\[ V_{DS} \text{ – Drain-to-Source Voltage – V} \]
\[ V_{GS} \text{ – Gate-to-Source Voltage – V} \]

\[ Q_{g} \text{ – Gate Charge – nC} \]

\[ V_{DD} = 30 \text{ V} \]
\[ V_{DD} = 20 \text{ V} \]
\[ V_{DD} = 48 \text{ V} \]

\[ I_{D} = 625 \text{ mA} \]
\[ T_{J} = 25^\circ \text{C} \]

See Figure 3

Figure 13

REVERSE-RECOVERY TIME

\[ t_{rr} \text{ – Reverse-Recovery Time – ns} \]

\[ \text{REVERSE } di/dt \]

\[ Z_{1}, Z_{2}, \text{ and } Z_{3} \]

\[ V_{DS} = 48 \text{ V} \]
\[ V_{GS} = 0 \]
\[ I_{S} = 625 \text{ mA} \]
\[ T_{J} = 25^\circ \text{C} \]

See Figure 1

Figure 14
MAXIMUM DRAIN CURRENT

vs

DRAIN-TO-SOURCE VOLTAGE

MAXIMUM PEAK AVALANCHE CURRENT

vs

TIME DURATION OF AVALANCHE

† Less than 2% duty cycle
‡ Device mounted on FR4 printed-circuit board with no heatsink.
.§ Device mounted in intimate contact with infinite heatsink.

Figure 15

Figure 16

See Figure 4
THERMAL INFORMATION

DW PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
VS
PULSE DURATION

† Device mounted on 24 in², 4-layer FR4 printed-circuit board with no heatsink.
NOTE A: $Z_{θJB}(t) = r(t)⋅R_{θJB}$
$tw$ = pulse duration
$tc$ = cycle time
d = duty cycle = $tw/tc$

d = 0.01 0.02 0.05 0.1 0.2 0.5

DC Conditions

Single Pulse

Figure 17
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