Title	***Engineering Prototype Report (EPR-00010)*** ***15W, Universal Input, Single Output, Isolated Converter with TOP233Y (EP-10)***
Recipients	
Application	Battery Charger
Author	S. L.
Date	14-November-2000

Abstract

This document presents the specification, schematic & BOM, transformer calculation, test data, wave forms and EMI scan for a low cost, isolated converter for a battery charger application.

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Contents

1.0 Introduction

This document presents the specification, schematic & BOM, transformer calculation, test data, wave forms and EMI scan for a low cost, isolated converter for a battery charger application. The converter is designed with TOP233Y(TOPSwitch-FX family) which brings the following benefits at no extra cost:

-low component stress (soft start)
-overload protection (auto-restart)
-remote ON/OFF(computer interface; not used in the current design)
-undervoltage and overvoltage protection (lockout -UVLO/OVLO)
-over-temperature protection (hysteretic thermal shutdown)
-energy saving (cycle skipping at low load)
-EMI standard met with a low cost transformer, without shield winding and flux band (frequency jitter).
-small size magnetics (132kHz switching frequency)
-high efficiency (73% max. duty cycle and reduced-programmable current limit; not used in the current design)

2.0 Power Supply Requirements Specification

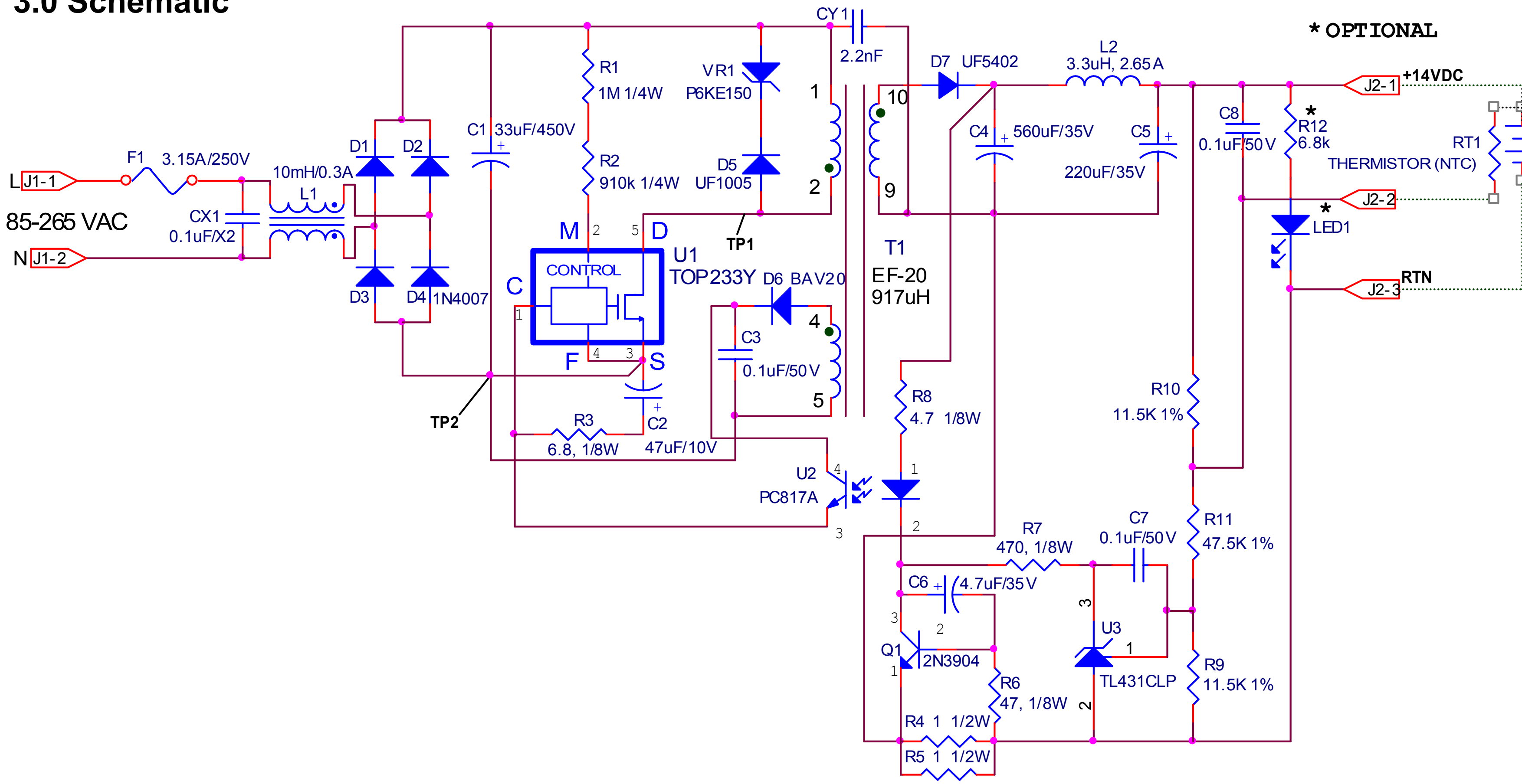
Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Normal Operating Input Voltage	Vin	85		265	Vac	50/60Hz
Abnormal Input Voltage*	Vin			300	Vac	50/60Hz
No load input power				390	mW	Vin=265Vac, 60Hz
Output						Green LED indicator
Output Voltage**	Vout		14		Vdc	+/-5% Total
Output Ripple Voltage	Vout ripple			200	mV	Peak to Peak
Output Current Limit***	Iout	0.02		1.2	A	
Power Output						
Continuous Output Power****	Pout		15		W	@ Full Load
Power supply efficiency	η		75		%	@ Full Load
Environmental						
Temperature	Tamb	0		50	°C	
Safety						IEC950/UL1950
Surge (differential, 2 ohm)	Line-Line		1		kV	IEC/UL 1000-4-5 Class 3
Surge (common mode, 12 ohm)	Line-Earth		2		kV	IEC/UL 1000-4-5 Class 3
EMI-Conducted *****						CISPR22B

*Under voltage lockout: Power supply ON@ >70Vac, OFF@ <50Vac & loss of regulation (load dependent).
Over voltage lockout: Power supply OFF @ >307Vac and back ON @ <290Vac.

**Can be adjusted by changing the U3-1voltage (TL431).
Battery charging voltage temperature compensation input available for external thermistor, NTC. (Floating/trickle charge: -3.9mV/degC; -20mV/degC and –30mV/degC are also common).

***Current limit set/programmable with a sense resistor.
****Power output derated if no heat sink is used at Tamb >40degC.
***** Output load not grounded

3.0 Schematic



Title	14V/15W Charger		
Size A	Document Number EP-10		Rev K
Date:	Tuesday, January 16, 2001	Sheet 1 of 1	

4.0 Circuit Description

Specific features of this circuit (page 4) are:
settable under voltage/over voltage protection, extended input voltage range(85-300Vac), settable battery charging current limit and charging voltage with correction for battery temperature.

The AC input is rectified (D1-D4) and filtered (C1) to create a high voltage DC buss which is connected to T1-1. The primary current is modulated by U1 (TOP233Y) at 130kHz(U1-4 connected to U1-3). The secondary induced voltage(T-7,8) is rectified and filtered by D7, C4 with additional filtering provided by L2, C5 to give the 14Vdc output.

The input fuse F1 is sized to resist the capacitor C1 charging current and isolates the line from a potential rectifier bridge (D1-D4) failure. Inductor L1 reduces the common mode noise and its leakage inductance together with CX1, the differential mode noise. The frequency jitter in TOP233Y (U1) allows the unit to meet worldwide conducted EMI standards using a common mode choke (L1) in combination with small value capacitors (CX1and CY1) and a proper PCB layout. The input filter is optimized when the EMI requirements are met with the lowest L1 (leak)*CX1 product value. Resistors R1+ R2 value (1.91Mohm) sets the under voltage (UVLO) and the overvoltage (OVLO) lock out voltage levels.
The TOP233Y (U1-2) UV/OV threshold currents are 50/225uA, with 10uA hysteresis, going down, for 225uA (215uA threshold). UVLO= 50uA* 1.91Mohm= 95.5 Vdc (~75Vac), OVLO=225uA* 1.91Mohm= 430Vdc (~307Vac). On the rising input voltage, turn ON occurs at > 50uA (UVLO=95.5Vdc) and turn OFF at >225uA (OVLO=430Vdc). On the falling input voltage, turn ON occurs < 215uA (OVLO= 411Vdc) and turn OFF at <50uA and loss of regulation. The power supply turns off automatically when it loses the regulation at a given output load. VR1 and D5 form a clamp circuit that limits the turn-off voltage spike to a safe level on U1-5 (DRAIN) pin.

There are two output control loops, both feeding back into the control pin (U1-1). The current input is supplied by the bias winding (T1-3,4) and modulated by the optocoupler (U2-3,4) phototransistor. The optocoupler (U2-1,2) photodiode current is controlled by:
1- The voltage control loop (U3, R7, R9,10, 11, RT1) in the constant voltage mode.
2- The current control loop (Q1, R4,5,6) in the constant current mode.

1.The 14Vdc output voltage is controlled by the sum of the voltage drops across the opto-coupler U2 and the voltage regulator U3. Resistor R8 (AC gain of the circuit) limits the current through U2, improving its response time. Resistor R7 sets the bias current for and C7 provides compensation for U3.
Different output voltages can be selected by changing R9, R10, R11 and RT1 according to this formula:

Vout= 2.5Vdc(1+(R11+(R10*RT1/R10+RT1))/R9), R10=11.5k 1%

If RT1 is not used: Vout= 2.5Vdc(1+(R11+R10)/R9), R10 must be 11.5k/2
(install a 11.5k 1% in parallel with existing R10).

2.The output current is limited to Iout~ 1.2A=0.6V/0.5ohm(Q1 Vce(sat)/R4, R5 parallel resistance).
The accuracy of Iout is limited by the Vce variation with the temperature and the precision of the current shunt R4, R5.

The primary-to-secondary isolation is provided by using parts/materials (opto/transformer insulation) with the correct level of isolation and creepage distances (opto slot/transformer bobbin). Also the CY1 value (while allowing common mode noise current path) has to keep the leakage current below the standard (IEC950) accepted value.

The 14Vdc monitoring light emitting diode (LED1) and 6.8k R12 are optional, and have been included in this circuit for troubleshooting convenience.

5.0 Layout

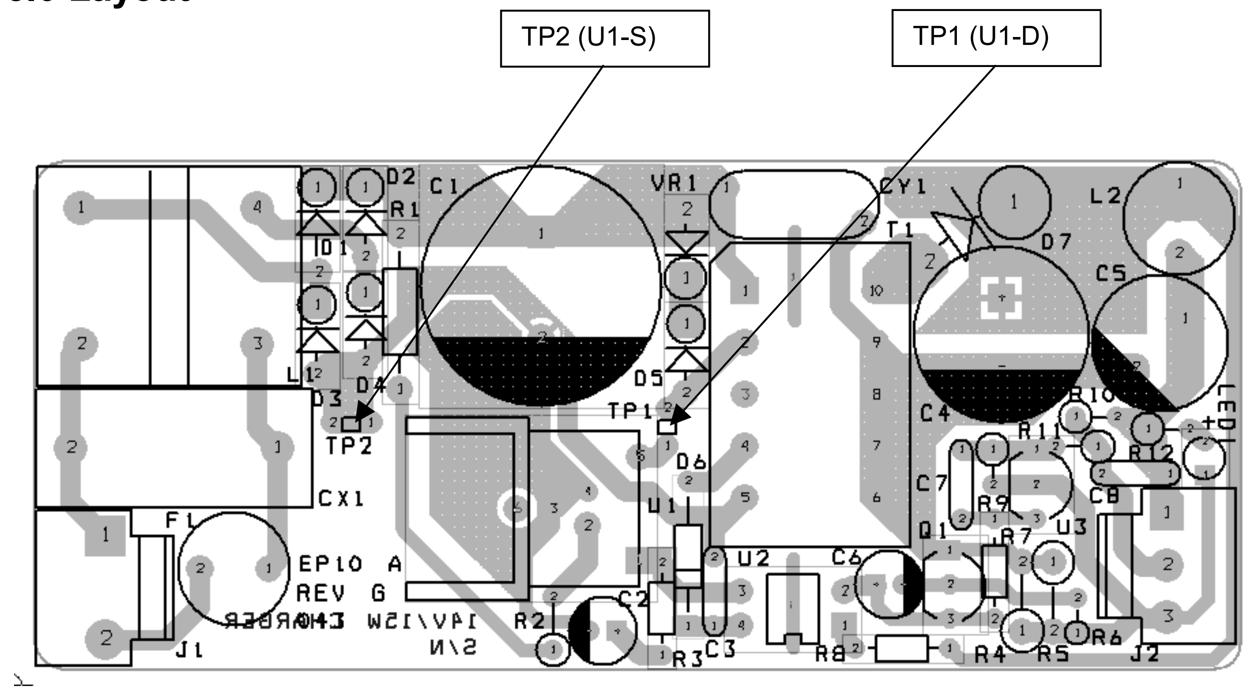


Fig.5.1. Board size: L90mm x W37mm x H28mm

Test points TP2 (U1 SOURCE) and TP1 (U1 DRAIN) are provided for ease of monitoring Vds. TP1 jumper can be replaced with a longer one to allow a current probe insertion for Id monitoring.

For the drain-to-source voltage waveforms, connect the high voltage probe tip to TP1 and the probe ground to test point TP2.
For switching current waveforms, replace jumper TP1 with a wire loop and use a Tektronix A6302 current probe and AM503 current probe amplifier (with TM501 power module) or equivalent.

6.0 Bill of Materials

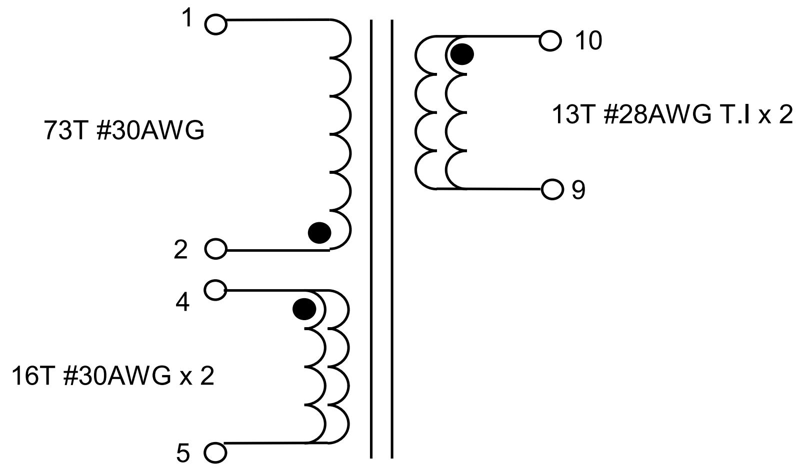
Item	Qty.	Ref.	Description	Part number	Manufacturer
1	1	CX1	0.1uF/X2, (250VAC)	F1772-410-2000	Vishay
2	1	CY1	2.2nF/Y1 (125/250VAC)	440LD22	Cera-mite
3	1	C1	33uF/450V	EEU-EB2W330S	Panasonic
4	1	C2	47uF/10V	ECE-A1-AV470	Panasonic SU
5	3	C3	0.1uF/50V	RPE121Z5U104M50V	Murata
6		C7	0.1uF/50V		
7		C8	0.1uF/50V		
8	1	C4	560uF/35V	ECA-1VFQ561	Panasonic
9	1	C5	220uF/35V	ECE-A1VGE221	Panasonic
10	1	C6	4.7uF/35V	ECE-A1VU 4R7	Panasonic SU
11	4	D1	1A, 1000V	1N4007	Generic
12		D2		1N4007	
13		D3		1N4007	
14		D4		1N4007	
15	1	D5	1A, 600V, 75nsec	UF1005	Vishay
16	1	D6	0.5W,200V, 4nsec	BAV20	Vishay
17	1	D7	3A, 200V, 50nsec	UF5402(UF3003)	Generic (Vishay)
18	1	F1	3.15A/250V	19372K, 3.15A	Wickman
19	2	J1	Header (0.156" spacing, 3pos.)	26-48-1035	Molex
20		J2			
21	1	LED1	GRN, low current	LG3369	Siemens
22	1	L1	10mH/0.3A	SU10V-03100	Tokin
23	1	L2	3.3uH, 2.65A	622LY-3R3M	Toko
24	1	Q1	Switching, 200MHz (NPN, TO92)	2N3904	
25	1	RT1	THERMISTOR (NTC)*	ERT-D2FHL462S	Panasonic
26	1	R1	1M, 1/4W		
27	1	R2	910k 1/4W		
28	1	R3	6.8, 1/8W		
29	2	R4	1, 1%, 1/2W		
30		R5			
31	1	R6	47, 1/8W		
32	1	R7	470, 1/8W		
33	1	R8	4.7 1/8W		
34	2	R9	11.5k, 1%, 1/4W		
35		R10			
36	1	R11	47.5k, 1%, 1/4W		
37	1	R12	6.8k, 1/4W		
38	1	T1	EF20, 917uH, 3 windings	Transformer,custom	Cooper
39	1	U1	TOPSwitch-FX	TOP233Y	Power Integrations
40	1	U2	Optocoupler	PC817A	Sharp
41	1	U3	Adjustable Shunt Regulator, TO-92	TL431CLP	Generic
42	1	VR1	150V, Tranzorb	P6KE150	GI/Vishay
43	1	HS1	Heat sink, TO-220, Vertical	S704	IERC/Digikey
44	1		Screw, No.3x8mm Pan Phil	H743-ND	Digikey
45	1		Split Lock Washer, No.3	H772-ND	Digikey
46	1		Hex Nut, No.3	H762-ND	Digikey

*Attaches to the battery (not part of the power supply).

7.0 Transformer

7.1 Transformer drawing

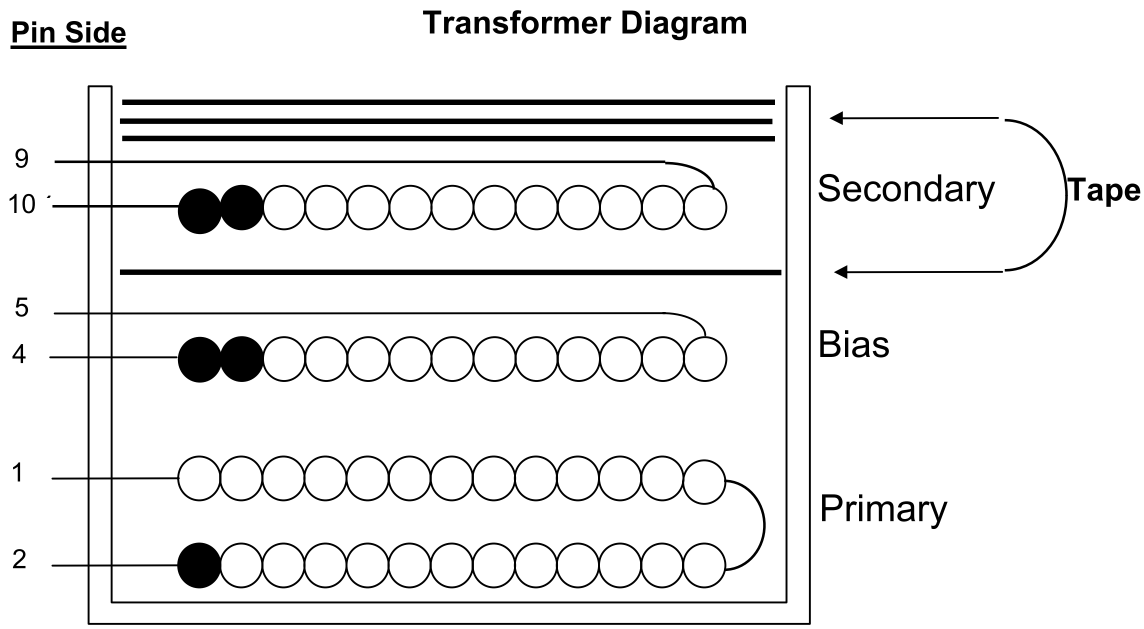
T1 schematic



Electrical Specifications:

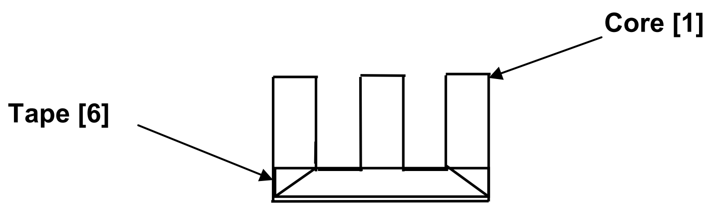
Electrical Strength	60Hz 1minute, from Pins 1-5 to Pins 6-10	3000 Vac
Primary Inductance	Between pins 1, 2, all other open, @100kHz	917uH +/- 10%
Resonant Frequency	Between pins 1, 2, all other open.	.7 MHz (Min.)
Primary Leakage Inductance	Between pins 1, 2, all other shorted, @100kHz	<15uH

Transformer Diagram



Transformer Construction:

Double Primary Layer	Start at Pin 2. Wind 40 turns of item [3] from left to right. Wind in a single layer. Wind remaining 33 turns (73 total) in the next layer from right to left. Finish on Pin 1.
Bias Winding	Start at Pin 4. Wind 16 turns Parallel Bifilar of item [3] from left to right. Wind uniformly, in a single layer, across entire width of bobbin. Finish on Pin 5.
Reinforced Insulation	1 Layer of tape [5] for insulation.
+14V Winding	Start at Pin 10. Wind 13 turns Parallel Bifilar of item [4] from left to right. Wind uniformly, in a single layer, across entire width of bobbin. Finish on Pin 9.
Outer Insulation	3 Layers of tape [5] for insulation.
Core Preparation	Wrap bottom of E core [1] with 2 layers of tape [6] as shown.
Final Assembly	Assemble and secure core halves. Impregnate uniformly [7].



Materials

Item	Description
[1]	Core: EPCOS (Siemens) E 20/10/6,B66311-G-X167, or equivalent. Gapped A_{LG} of 171 nH/T
[2]	Bobbin: EPCOS (Siemens) B66206-J1110-T1, or equivalent.
[3]	Magnet Wire: #30AWG Heavy Nyleze.
[4]	Triple Insulated Wire: # 28 AWG .
[5]	Tape: 3M 1298 Polyester Film (white) 12.2mm wide by 2.2 mils thick.
[6]	Tape: 3M 1298 Polyester Film (white) 15.7mm wide by 2.2 mils thick.
[7]	Varnish.

7.2 Transformer spreadsheet

Application Variables

VACMIN	85	Volts	Minimum AC Input Voltage
VACMAX	300	Volts	Maximum AC Input Voltage
FL	50	Hertz	AC Main Frequency
FS	124000	Hertz	Device switching Frequency
VO	15.00	Volts	Main Output Voltage
PO	15.00	Watts	Total Output Power
N	85.0	%	Efficiency Estimate
Z	0.49		Loss Allocation Factor
VB	19.00	Volts	Bias Voltage
TC	3	mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	33.0	uFarads	Input Filter Capacitor

Device Variables

Device	TOP233		Device Name
VOR	90.00	Volts	Reflected Output Voltage
KRPKDP	0.66		Ripple to Peak Current Ratio
KI	1.00		External Current Limit Ratio
ILIMITEXT	0.93	Amps	Device Current Limit, External Minimum
ILIMITMIN	0.93	Amps	Device Current Limit, Minimum
ILIMITMAX	1.07	Amps	Device Current Limit, Maximum
VDS	10.0	Volts	Device On-State Drain to Source Voltage
VO1	15.00	Volts	Output Voltage
VD1	1.0	Volts	Output Winding Diode Forward Voltage Drop
VDB	1.0	Volts	Bias Winding Diode Forward Voltage Drop

Transformer Core/ Construction Variables

Core/Bobbin	EF20		Core and Bobbin Type
AE	0.32	cm^2	Core Effective Cross Section Area
LE	4.63	cm	Core Effective Path Length
AL	1350	nH/T^2	Ungapped Core Effective Inductance
BW	12.50	mm	Bobbin Physical Winding Width
M	0.0	mm	Safety Margin Width
L	2.0		Number of Primary Layers
NS	13		Number of Main Turns

DC Input Voltage Parameters

VMIN	83	Volts	Minimum DC Input Voltage
VMAX	424	Volts	Maximum DC Input Voltage

Current Waveform Shape Parameters

DMAX	0.55		Maximum Duty Cycle
IAVG	0.21	Amps	Average Primary Current
IP	0.57	Amps	Peak Primary Current
IR	0.38	Amps	Primary Ripple Current
IRMS	0.30	Amps	Primary RMS Current

Transformer Primary Design Parameters

LP	905	uHenries	Primary Inductance
NP	73		Primary Winding Number of Turns
NB	16.25		Bias Winding Number of Turns
ALG	169	nH/T^2	Gapped Core Effective Inductance
BM	2216	Gauss	Maximum Operating Flux Density
BP	4137	Gauss	Peak Flux Density (Bp < 4200)
BAC	731	Gauss	AC Flux Density for Core Curves
UR	1554		Relative Permeability of Ungapped Core
LG	0.21	mm	Gap Length (Lg > 0.051 for TOP22X, Lg > 0.1 for TOP23X)
BWE	25.0	mm	Effective Bobbin Width
OD	0.34	mm	Maximum Primary Diameter including Insulation
INS	0.06	mm	Estimated Total Insulation Thickness
DIA	0.29	mm	Bare Conductor Diameter
AWG	30	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM	102	Cmils	Bare Conductor Effective Area in Circular Mils
CMA	343	Cmils/A	Primary Winding Current Capacity (200 < CMA < 500)

Transformer Secondary Design Parameters

ISP1	3.22	Amps	Peak Secondary Current
ISRMS1	1.51	Amps	Secondary RMS Current
IO1	1.000	Amps	Power Supply Output Current
IRIPPLE1	1.13	Amps	Output Capacitor RMS Ripple Current
CMS1	516	Cmils	Secondary Bare Conductor Minimum Circular Mils
AWGS1	22	AWG	Secondary Wire Gauge (Rounded to next smaller standard AWG value)
DIAS1	0.65	mm	Secondary Minimum Bare Conductor Diameter
ODS1	0.72	mm	Secondary Maximum Insulated Wire Outside Diameter
INSS1	0.07	mm	Maximum Secondary Insulation Wall Thickness
NS1	13.00		Secondary Number of Turns

Voltage Stress Parameters

VDRAIN	633	Volts	Maximum Drain Voltage Estimate (Includes Effect of Leakage Inductance)
PIVS1	90	Volts	Output Rectifier Maximum Peak Inverse Voltage
PIVB	113	Volts	Bias Rectifier Maximum Peak Inverse Voltage

8.0 Performance Data

TEST EQUIPMENT

INPUT: VOLTECH (PM100) AC POWER ANALYSER.
Power Line Meter (EPD Inc.)
OUTPUT: KIKUSUI (PLZ153W) ELECTRONIC LOAD.

8.1 Efficiency

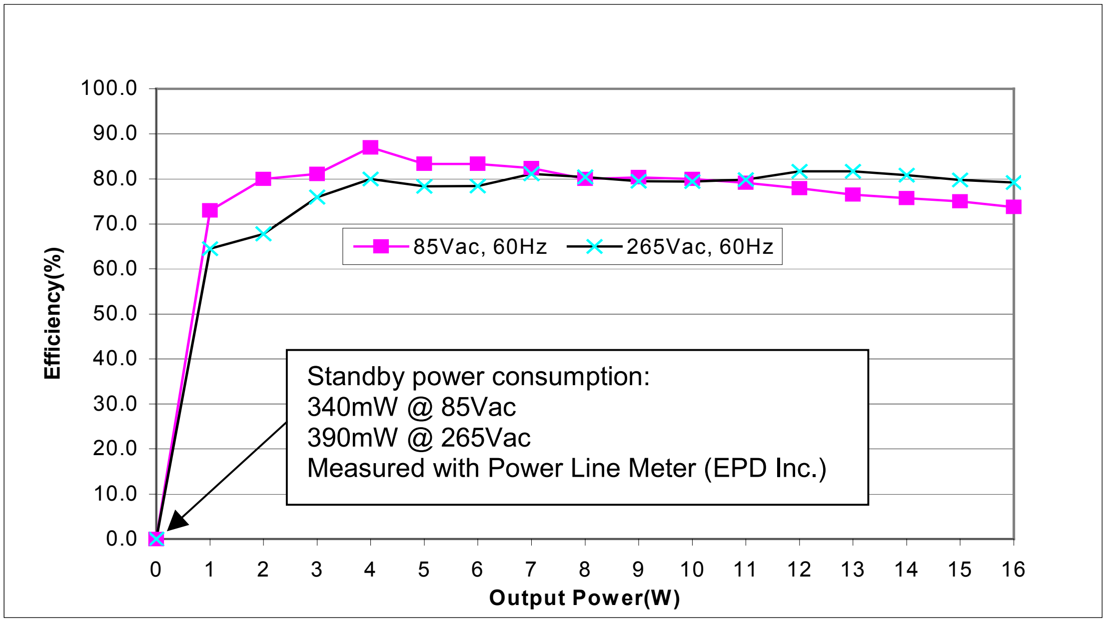


Figure 8.1.1. Efficiency vs output power at 25C, 60Hz.

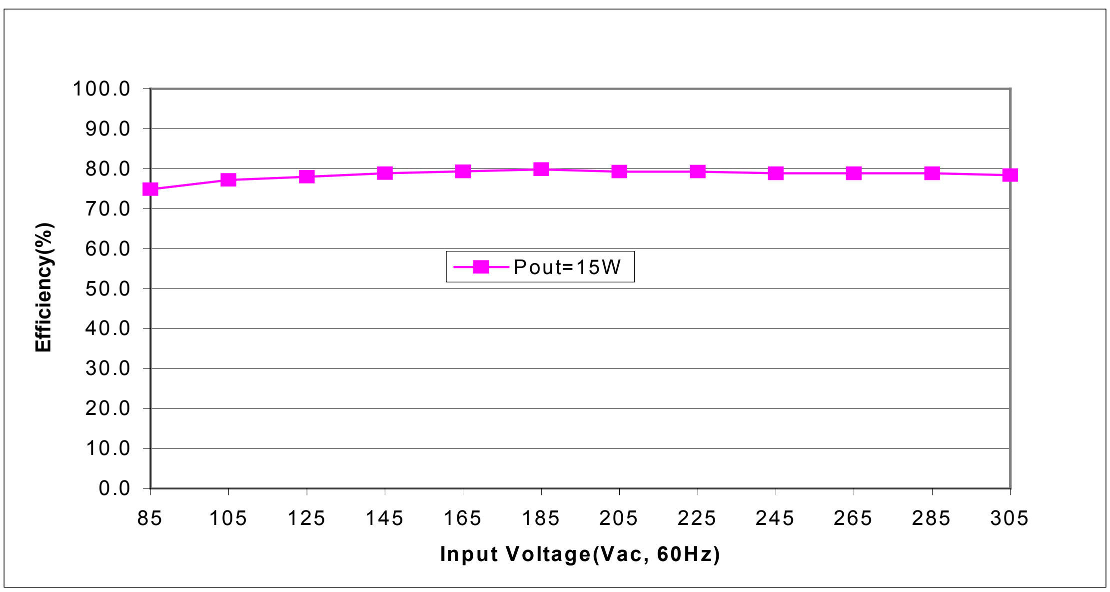


Figure 8.1.2. Efficiency vs input voltage at 25C, 60Hz.

8.2 Regulation

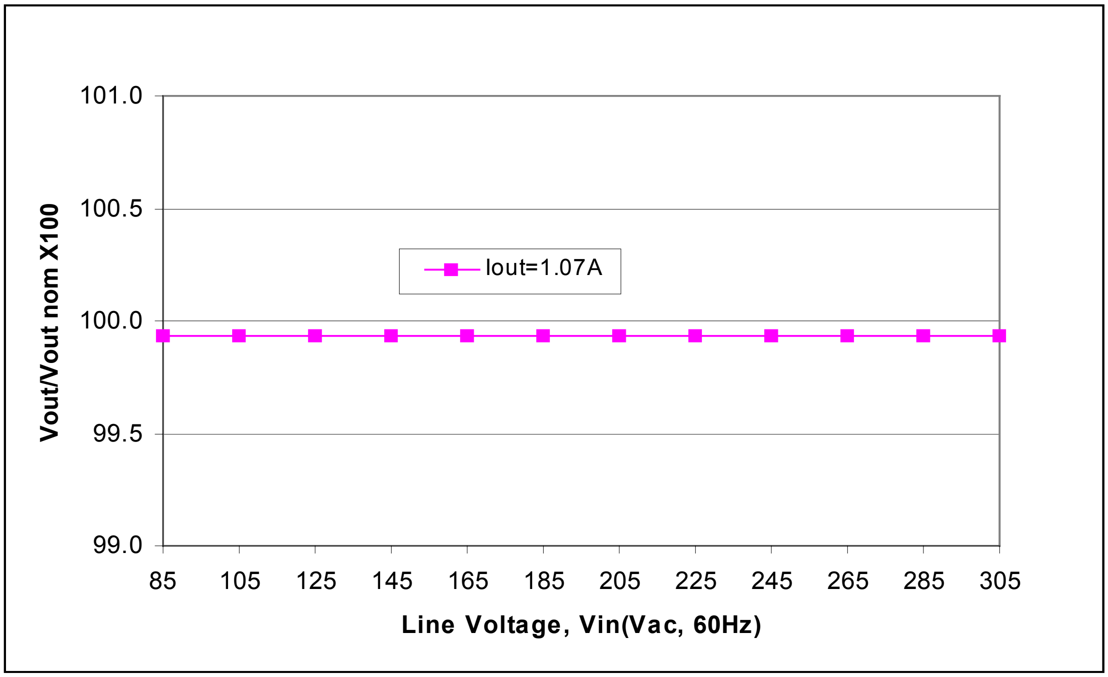


Figure 8.2.1 Regulation vs input voltage at full load @ 25C ambient.

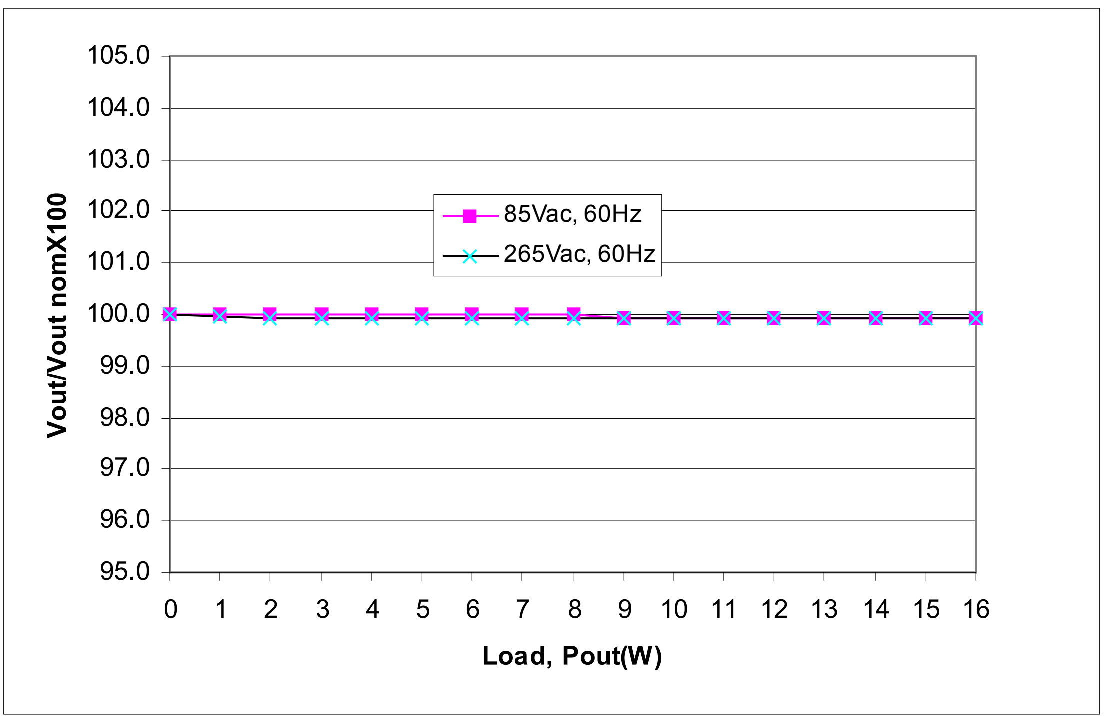


Figure 8.2.2 Regulation vs load @ 25C ambient.

8.3 Vout vs Iout

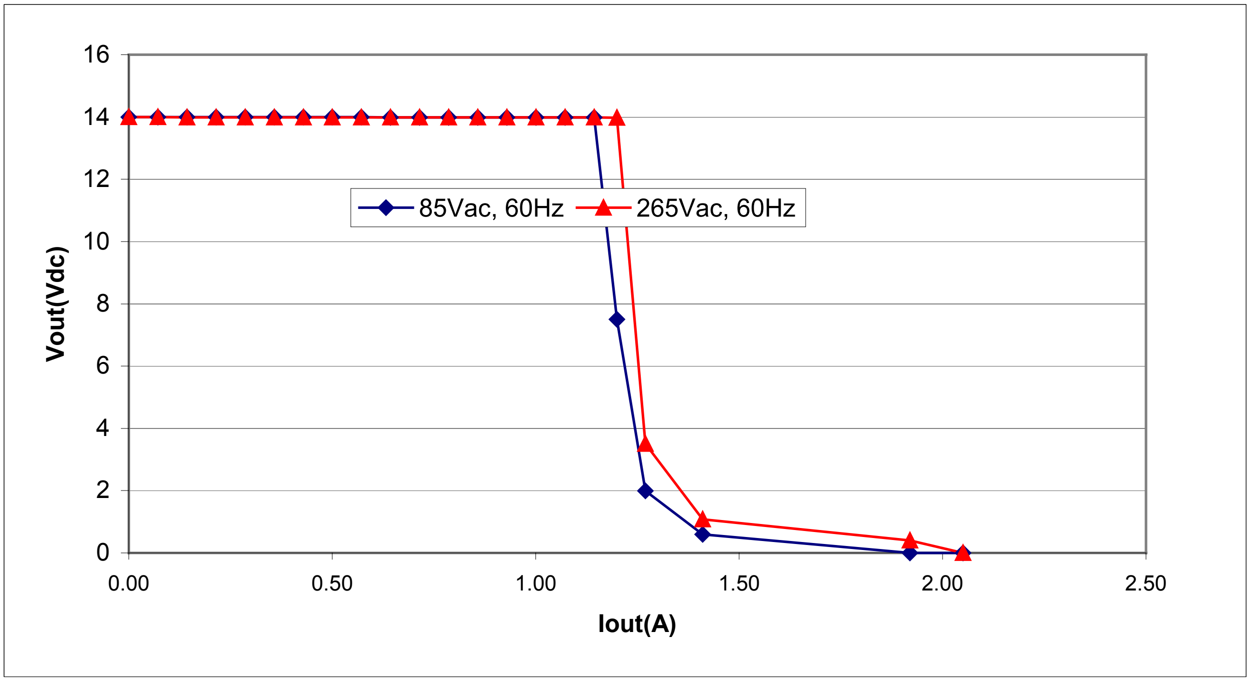


Figure 8.3.1 Vout vs Iout

8.4 Temperature

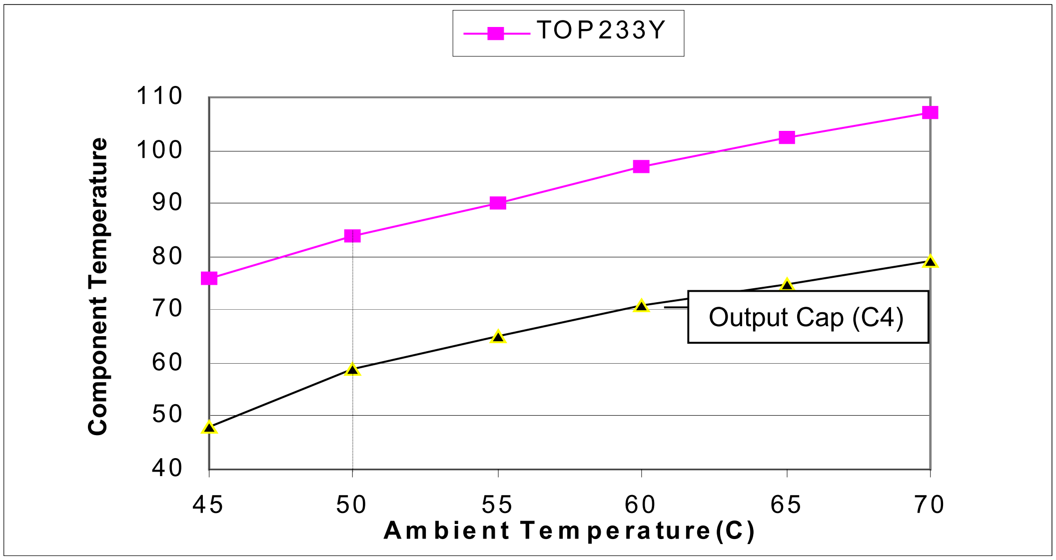


Figure 8.4.1. Maximum component temperature at 85Vac,full load.

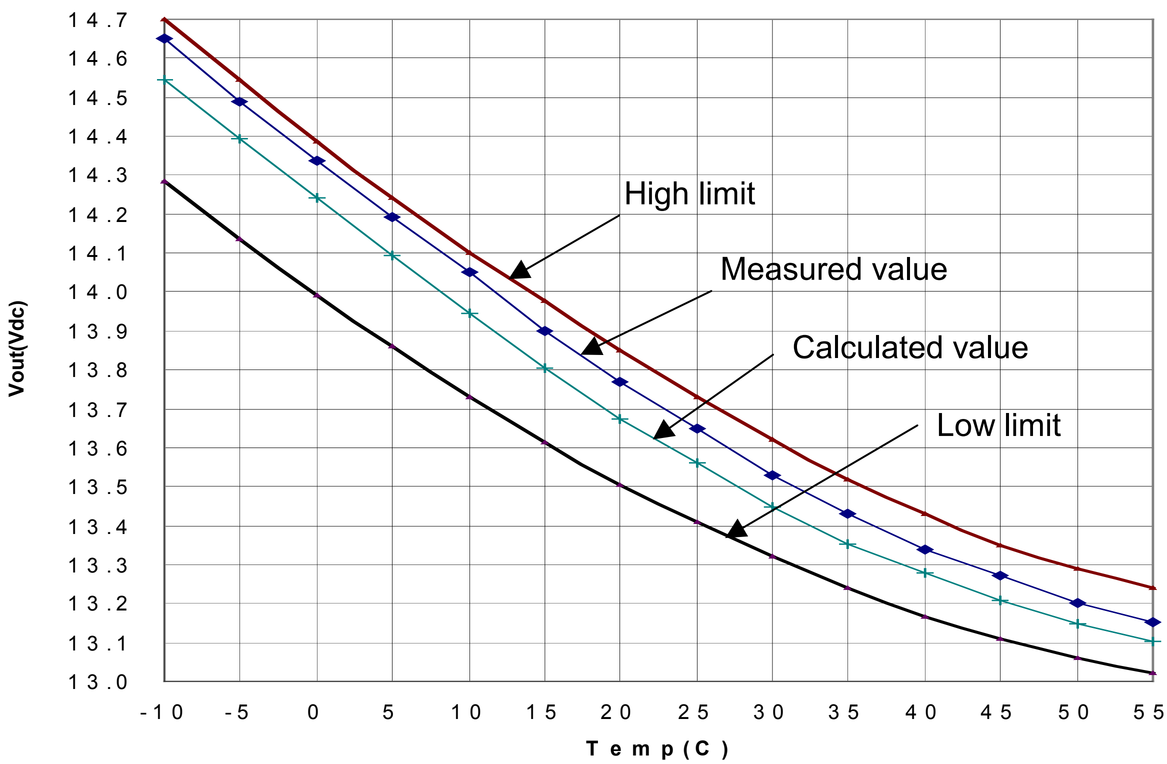


Figure 8.4.2. Power Supply Vout vs Battery Temperature (TR1 installed).

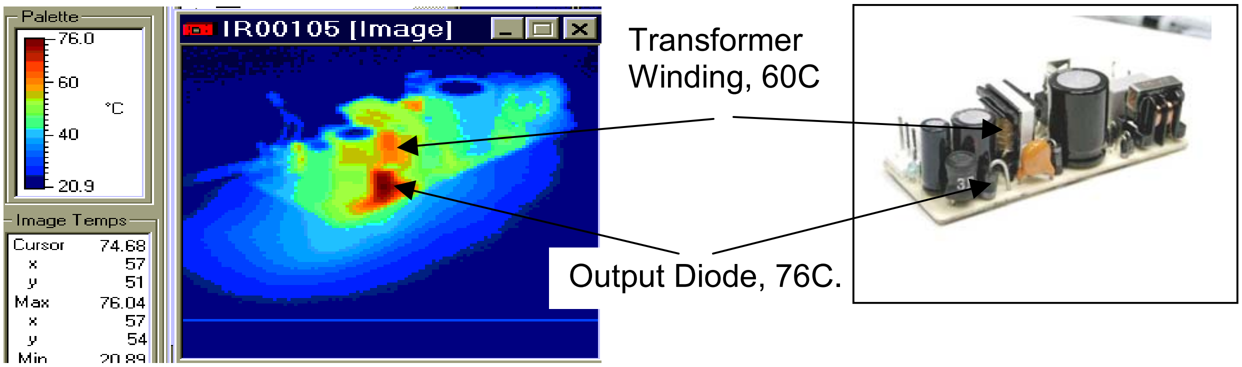


Figure 8.4.3 Infrared Scan at room temperature.
Output side view.

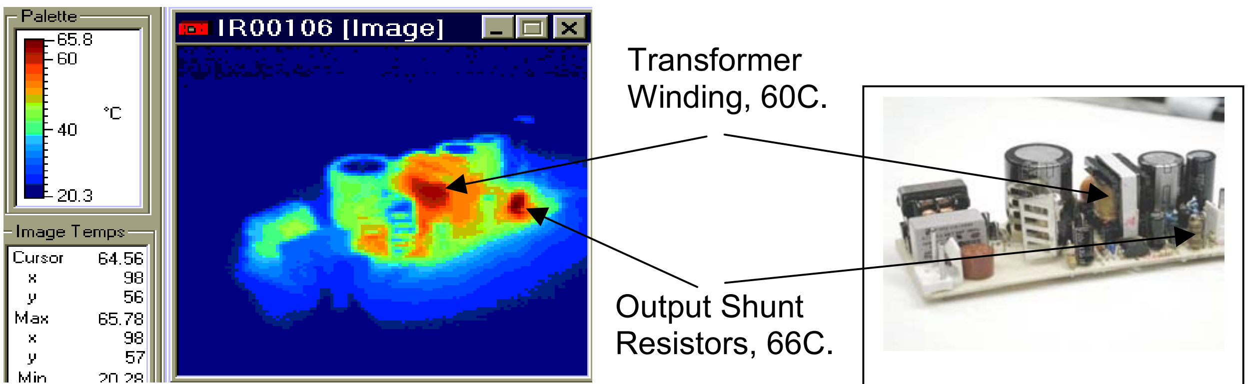


Figure 8.4.4 Infrared Scan at room temperature.
Input side view.

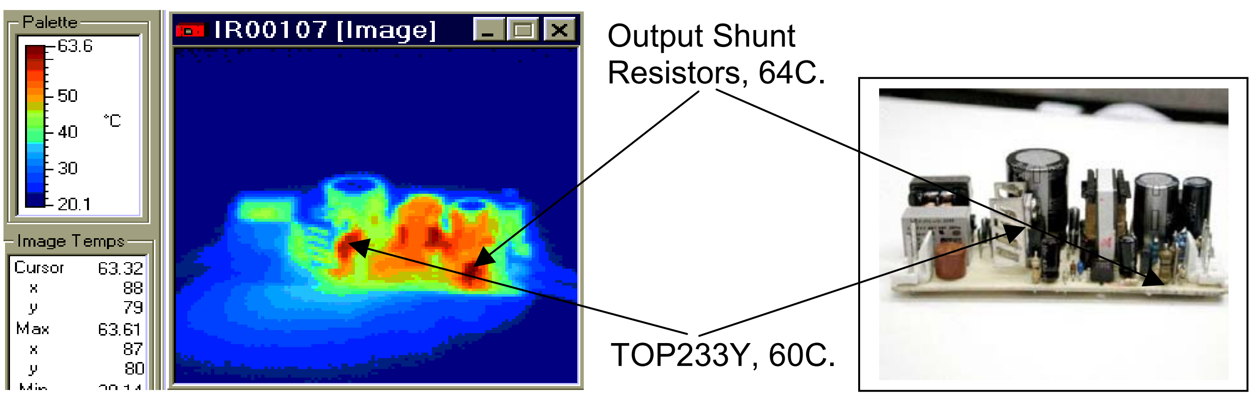


Figure 8.4.4 Infrared Scan at room temperature.
Lateral view.

8.5 Waveforms

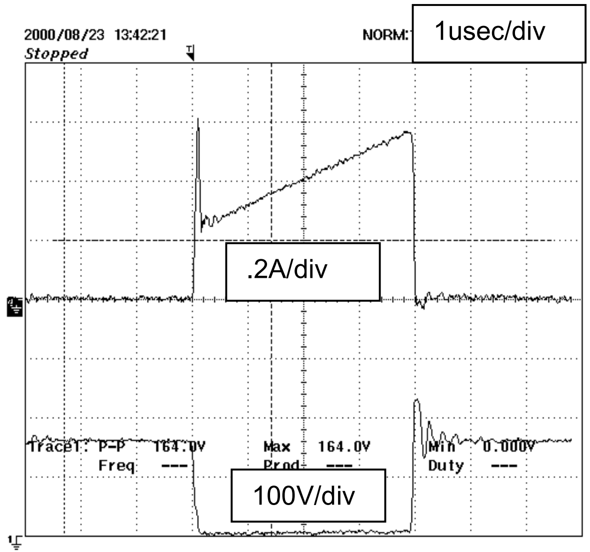


Figure 8.5.1 Drain current and drain-to-source voltage 85Vac, full load.

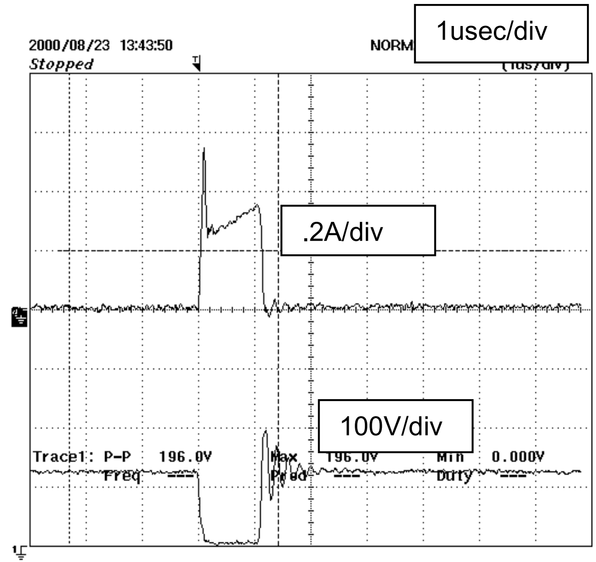


Figure 8.5.2 Drain current and drain-to-source voltage 85Vac, short.

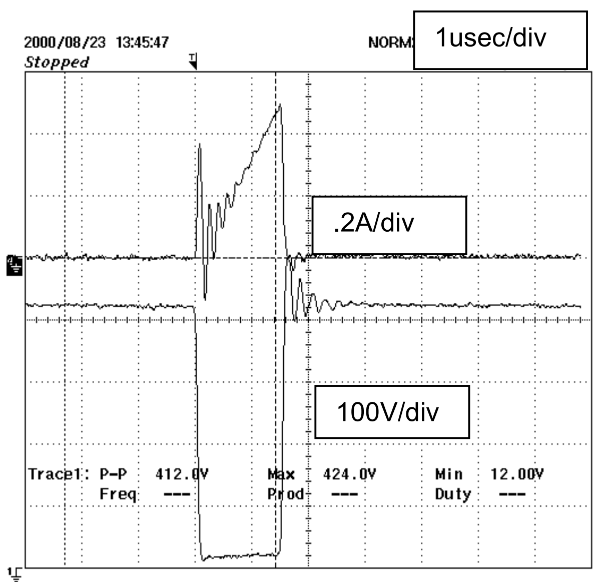


Figure 8.5.3 Drain current and drain-to-source voltage 265Vac, full load

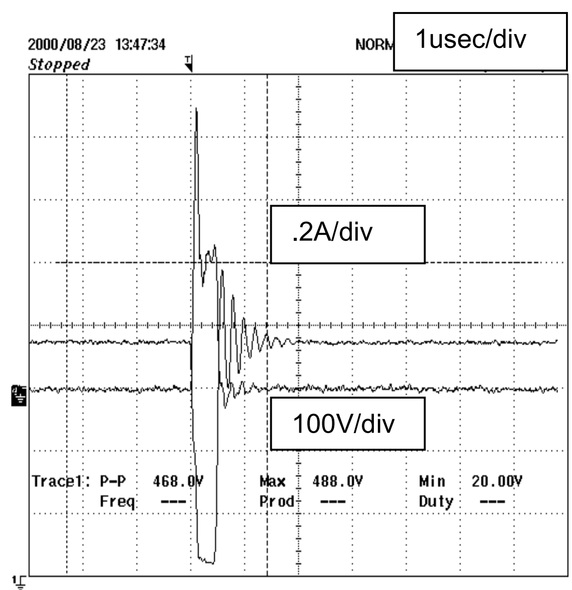


Figure 8.5.4 Drain current and drain-to-source voltage 265Vac, short.

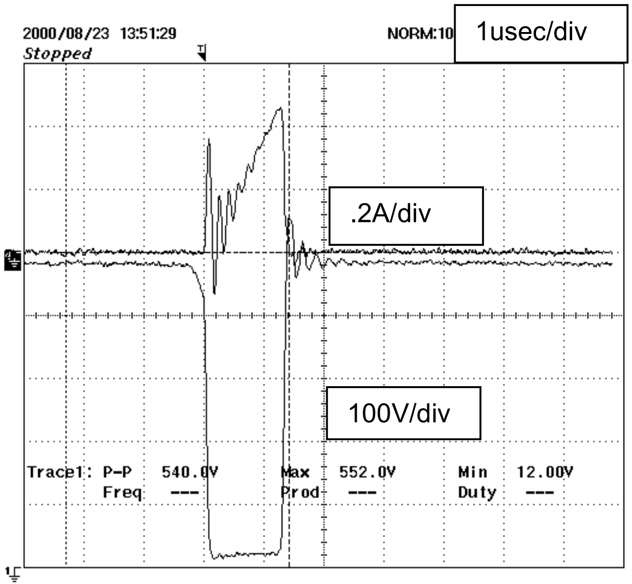


Figure 8.5.5 Drain current and drain-to-source voltage 300Vac full load.

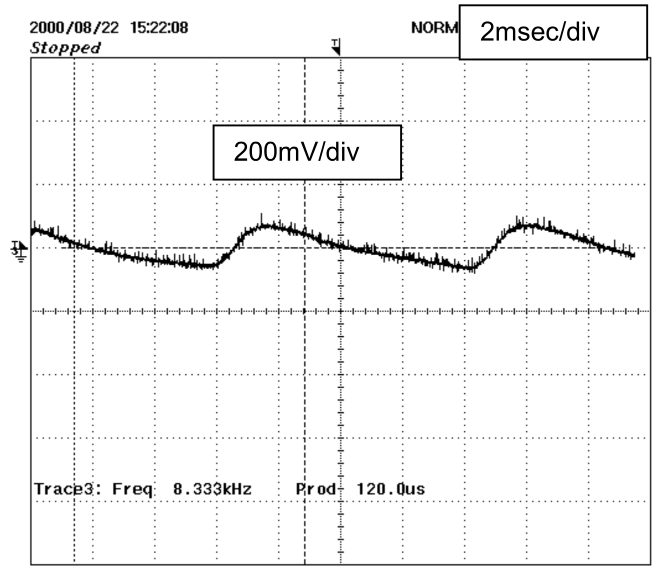


Figure 8.5.6 Output voltage ripple at 85VAC, full load, Line frequency 60Hz.

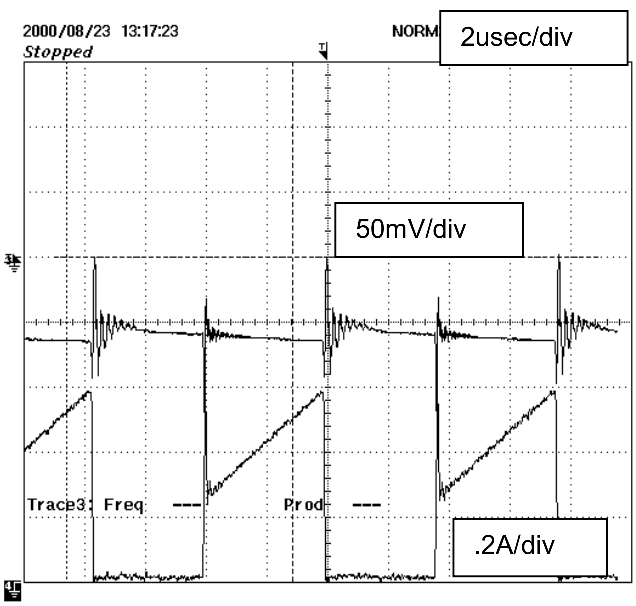


Figure 8.5.7 Output voltage ripple at 85Vac, full load Switching frequency 132kHz, High DC bus voltage.

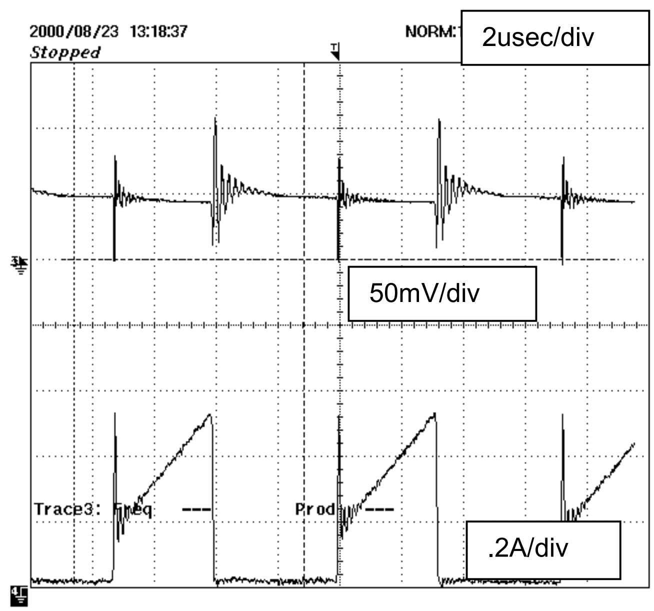


Figure 8.5.8 Output voltage ripple at 85Vac, full load Switching frequency 132kHz, Low DC bus voltage.

8.6 Transient response

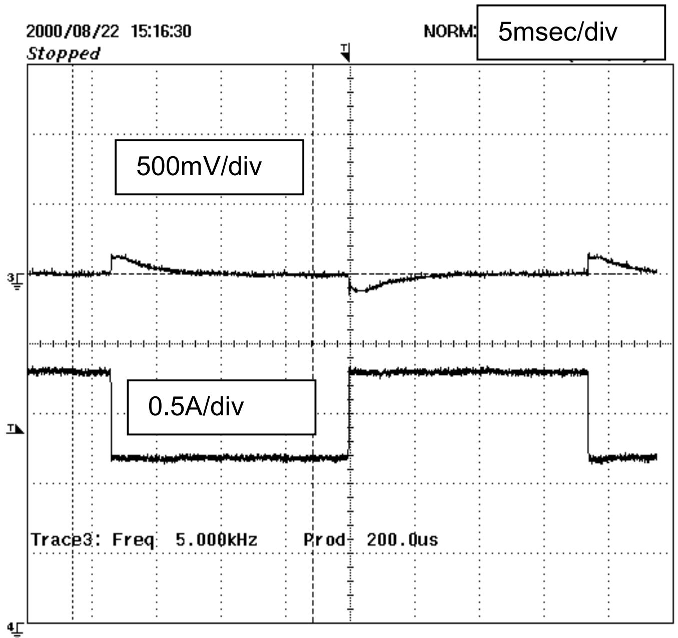


Figure 8.6.1 Transient response, Vin=85Vac, 50-75% load change

8.7 Conducted EMI Scans

The attached plots show worst-case EMI performance for EP10 as compared to CISPR22B conducted emissions limits.
For EMI and safety techniques refer to PI application note AN15 (Figure 6 shows a typical test set up).

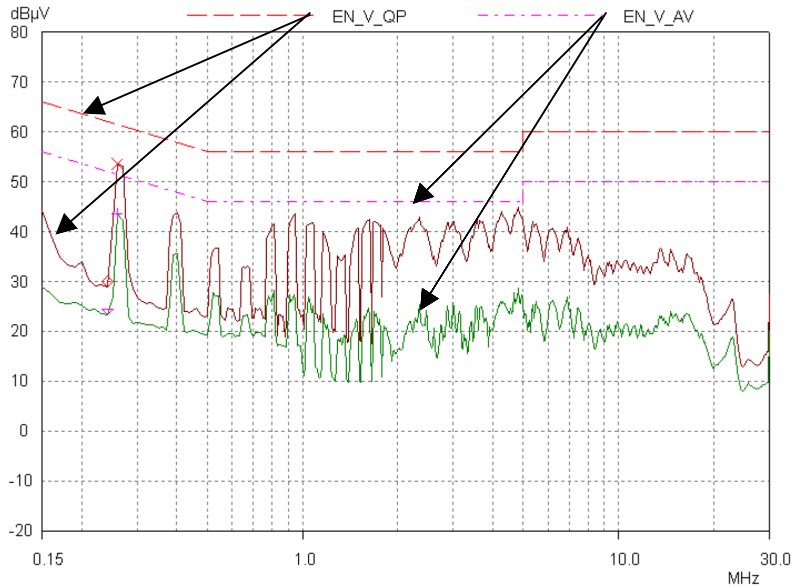


Figure 8.7.1. Quasi-peak and average scans at 230Vac, L , full load, output floating.

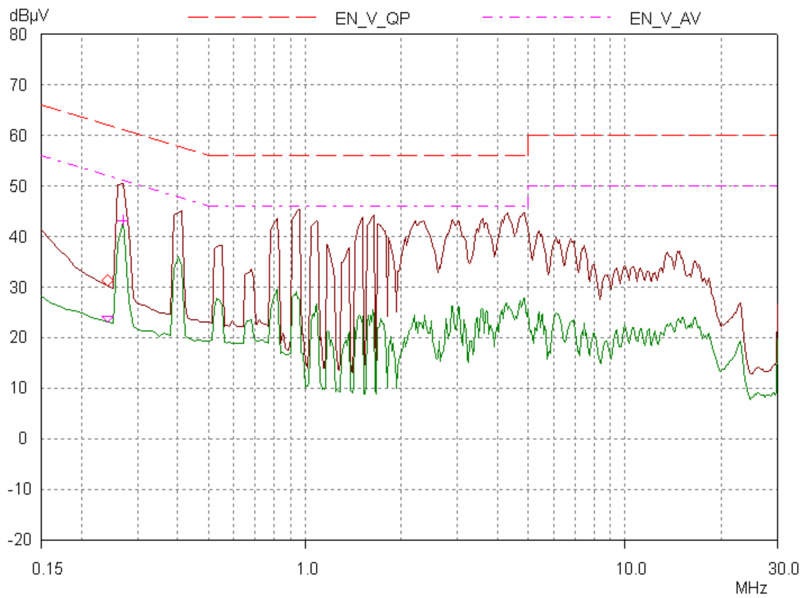


Figure 8.7.2. Quasi-peak and average scans at 230Vac, N , full load, output floating.

8.8 Surge Voltage

8.8.1 Differential = line-to-line (L-N), 2 ohm source impedance.

The unit exceeded the 1kV IEC/UL 1000-4-5 Class 3 requirement (meets Class 4, 2kV).
The CX1 capacitor failed after more than 20 2.5kV surges.
During the 2.5kV surge, the unit turns off for approximately 1.8 seconds.

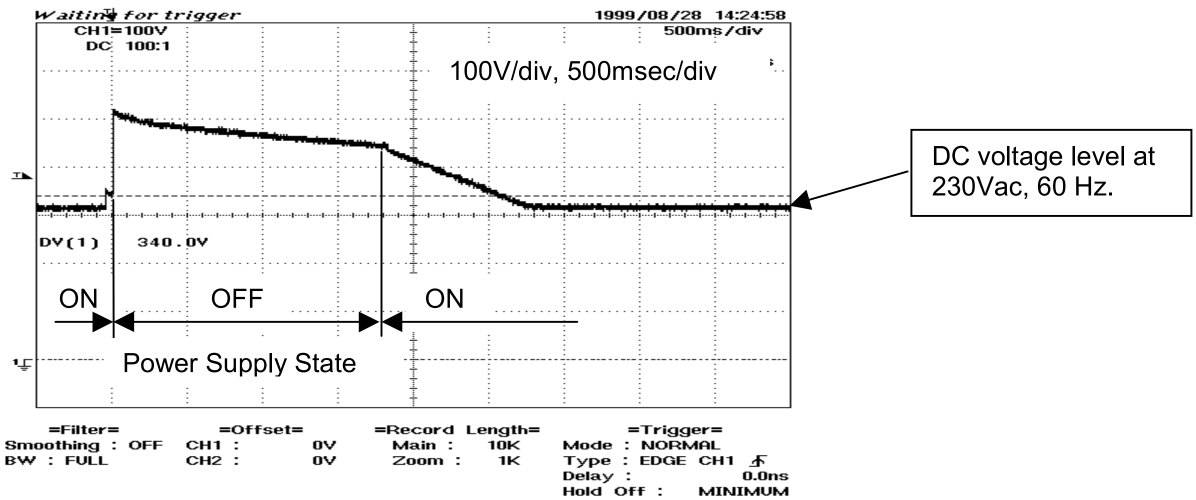


Figure 8.8.1 C1 (DC bus) voltage after the 2.5kV surge.

8.8.2 Common mode = line-to-ground (L-GND, N-GND), 12 ohm source impedance

The unit exceeded the IEC/UL 1000-4-5 Class 3, 2kV and Class 4, 4kV requirements. The maximum test voltage was 6kV. During the 6kV surges, the unit continues to operate. The unit was centered on the insulation side of a 6 in x 4 in single sided copper clad board (1/16 in insulation), to avoid surface or insulation breakdown during the voltage surges. The voltage was applied between the input terminals of the unit (L or N) and the copper clad ground plane (GND), in the following sequence:

L(+6kV) to GND , 5 times
L(-6kV) to GND , 5 times
N(+6kV) to GND , 5 times
N(-6kV) to GND , 5 times

Revisions

Author	Date	Rev	Description
S.L..	7.31.00	1	First Draft
	8.22.00	2	Second Draft
	8.29.00	3	Third Draft
	8.31.00	4	Fourth Draft
	10.26.00	5	Release
	11.14.00	6	Changed title from EP10A to EP10
	01.31.01	7	Changed from EPR-10 to EPR-00010

Notes

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