# TOP221-227

## *TOPSwitch®-II* Family

### Three-terminal Off-line PWM Switch

## Product Highlights

- Lowest cost, lowest component count switcher solution
- Cost competitive with linears above 5W
- Very low AC/DC losses-up to 90% efficiency
- Built-in Auto-restart and Current limiting
- Latching Thermal shutdown for system level protection
- Implements Buck, Boost, Flyback or Forward topology
- Works with primary or opto feedback
- Stable in discontinuous or continuous conduction mode
- Source connected tab for low EMI
- Ease of design, technical support material reduce time-to-market

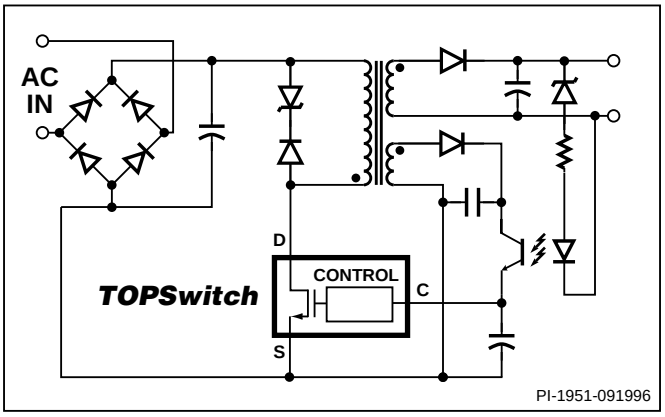



*Figure 1. Typical Application.*

## Description

The second generation *TOPSwitch-II* family is more cost effective and provides several enhancements to the first generation *TOPSwitch* family. The *TOPSwitch-II* family extends the power range from 100W to 150W for 100/115/230 VAC input and from 50W to 90W for 85-265 VAC universal input. This brings *TOPSwitch* technology advantages to many new applications, i.e. TV, Monitor, Audio amplifiers, etc. Many significant circuit enhancements that reduce the sensitivity to board layout and line transients now make the design even easier. The standard 8L PDIP package option reduces cost in lower power, high efficiency applications. The internal lead frame of this package uses six of its pins to transfer heat from the chip directly to the board eliminating the cost of a heat sink. *TOPSwitch* incorporates all functions necessary for a switched mode control system into a three terminal monolithic IC: power MOSFET, PWM controller, high voltage start up circuit, loop compensation and fault protection circuitry.

**OUTPUT POWER TABLE**

| TO-220 PACKAGE[1] | | | 8L PDIP PACKAGE[2] | | |
|---|---|---|---|---|---|
| PART ORDER NUMBER | Single Voltage Input[3] 100/115/230 VAC ±15% $P_{MAX}$[4,6] | Wide Range Input 85 to 265 VAC $P_{MAX}$[4,6] | PART ORDER NUMBER | Single Voltage Input[3] 100/115/230 VAC ±15% $P_{MAX}$[5,6] | Wide Range Input 85 to 265 VAC $P_{MAX}$[5,6] |
| TOP221Y | 12 W | 7 W | TOP221P | 9 W | 6 W |
| TOP222Y | 25 W | 15 W | TOP222P | 15 W | 10 W |
| TOP223Y | 50 W | 30 W | TOP223P | 24 W | 15 W |
| TOP224Y | 75 W | 45 W | TOP224P | 31 W | 19 W |
| TOP225Y | 100 W | 60 W | | | |
| TOP226Y | 125 W | 75 W | | | |
| TOP227Y | 150 W | 90 W | | | |

Notes: **1**. Package outline: YO3A **2**. Package Outline: PO8A **3.** 100/115 VAC with doubler input **4**. Assumes appropriate heat sinking to keep the maximum *TOPSwitch* junction temperature below 100˚ C. **5**. 50˚ C ambient, soldered to 0.36 sq. in.( 232 $mm^2$), 2 oz. copper clad **6**. $P_{MAX}$ is the maximum practical continuous power output level for conditions shown. The continuous power capability in a given application depends on thermal environment, transformer design, efficiency required, minimum specified input voltage, input storage capacitance, etc.

April 1997

# *PRELIMINARY*

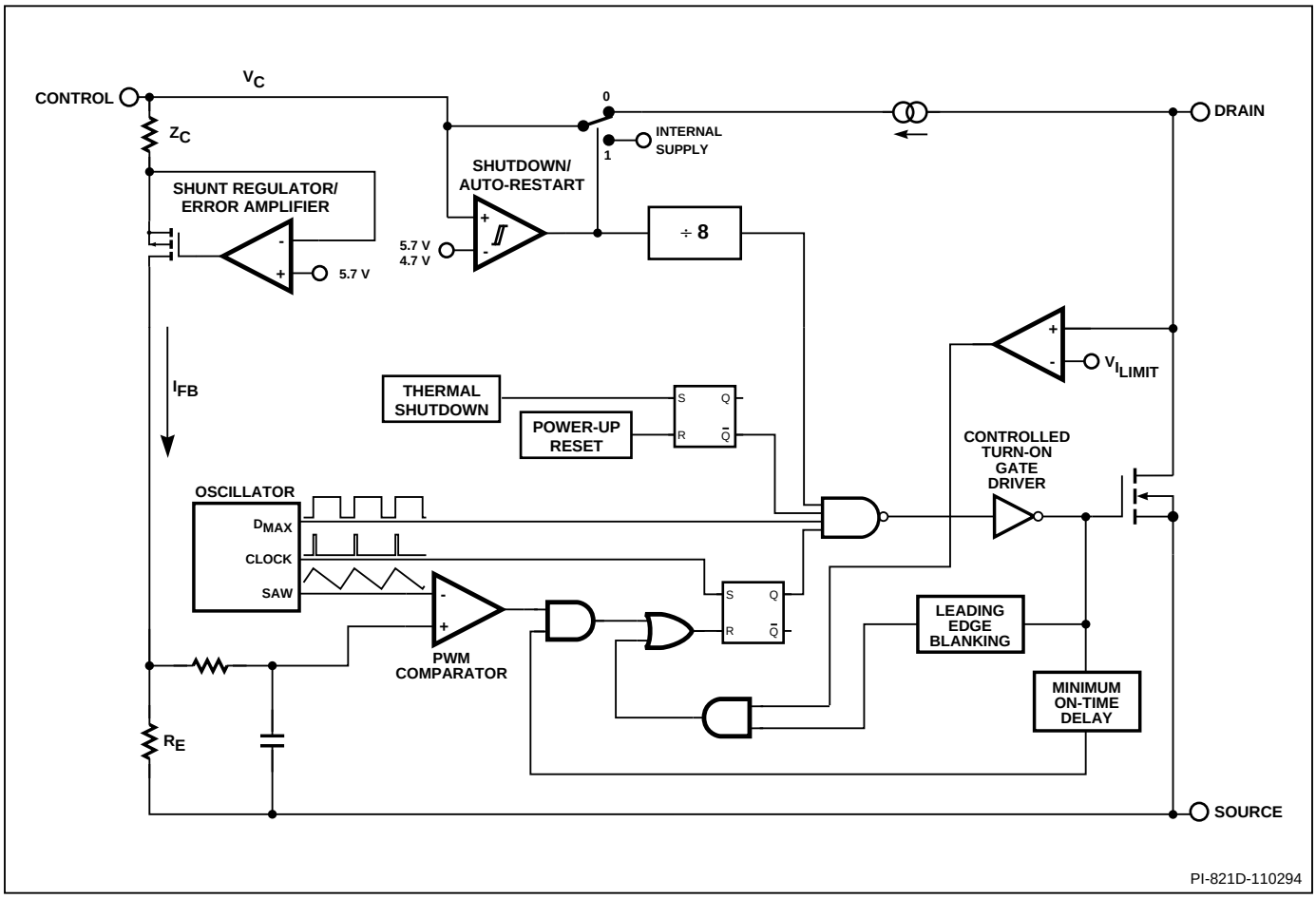



*Figure 2. Functional Block Diagram.*

## Pin Functional Description

**DRAIN Pin:**
Output MOSFET drain connection. Provides internal bias current during start-up operation via an internal switched high-voltage current source. Internal current sense point.

**CONTROL Pin:**
Error amplifier and feedback current input pin for duty cycle control. Internal shunt regulator connection to provide internal bias current during normal operation. It is also used as the connection point for the supply bypass and auto-restart/ compensation capacitor.

**SOURCE Pin:**
Y - Output MOSFET source connection for high voltage power return. Primary side circuit common and reference point.

P - Primary side control circuit common and reference point.

**SOURCE (HV RTN) Pin: (P only)**
Output MOSFET source connection for high voltage power return.

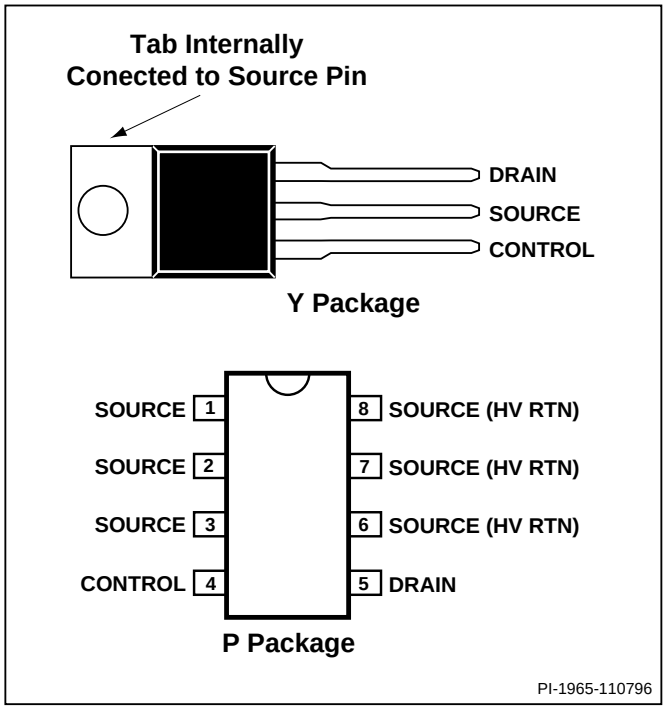



*Figure 3. Pin Configuration.*

## *TOPSwitch* Family Functional Description

*TOPSwitch* is a self biased and protected linear control current-to-duty cycle converter with an open drain output. High efficiency is achieved through the use of CMOS and integration of the maximum number of functions possible. CMOS process significantly reduces bias currents as compared to bipolar or discrete solutions. Integration eliminates external power resistors used for current sensing and/or supplying initial start-up bias current.

During normal operation, the internal output MOSFET duty cycle linearly decreases with increasing CONTROL pin current as shown in Figure 4. To implement all the required control, bias, and protection functions, the DRAIN and CONTROL pins each perform several functions as described below. Refer to Figure 2 for a block diagram and to Figure 6 for timing and voltage waveforms of the *TOPSwitch* integrated circuit.

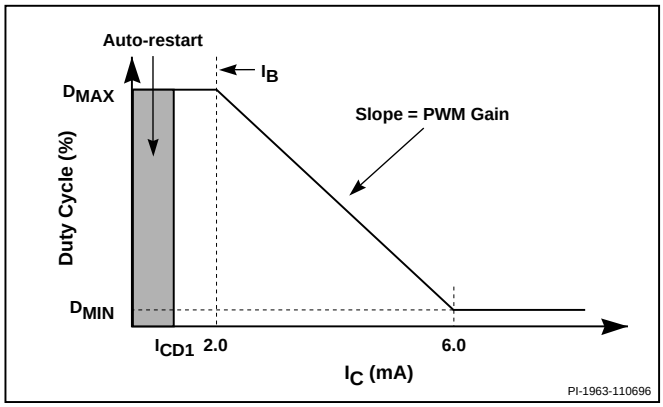



*Figure 4. Relationship of Duty Cycle to CONTROL Pin Current.*

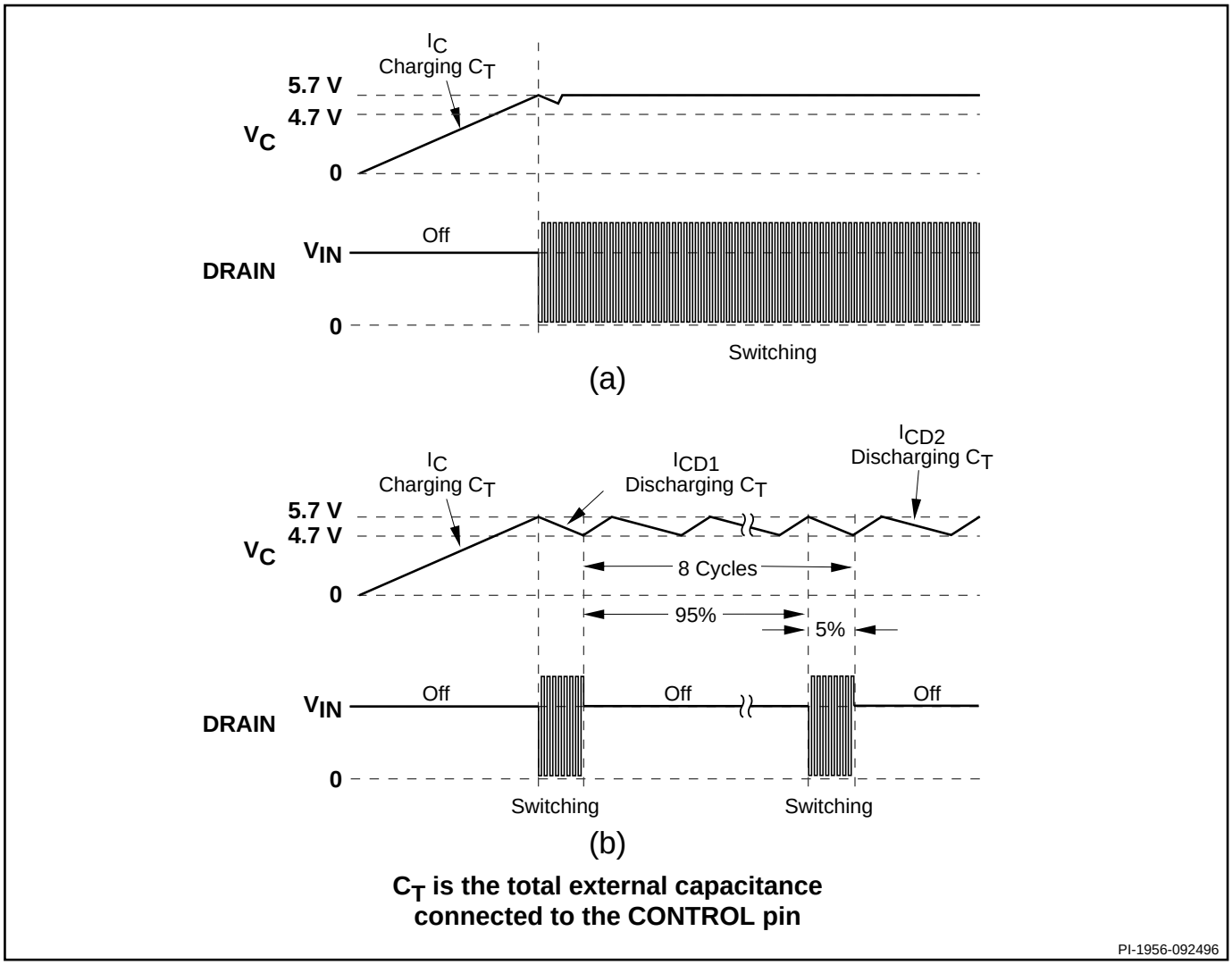



*Figure 5. Start-up Waveforms for (a) Normal Operation and (b) Auto-restart.*

## *TOPSwitch* Family Functional Description (cont.)

**Control Voltage Supply**
CONTROL pin voltage $V_C$ is the supply or bias voltage for the controller and driver circuitry. An external bypass capacitor closely connected between the CONTROL and SOURCE pins is required to supply the gate drive current. The total amount of capacitance connected to this pin ($C_T$) also sets the auto-restart timing as well as control loop compensation. $V_C$ is regulated in either of two modes of operation. Hysteretic regulation is used for initial start-up and overload operation. Shunt regulation is used to separate the duty cycle error signal from the control circuit supply current. During start-up, CONTROL pin current is supplied from a high-voltage switched current source connected internally between the DRAIN and CONTROL pins. The current source provides sufficient current to supply the control circuitry as well as charge the total external capacitance ($C_T$).

The first time $V_C$ reaches the upper threshold, the high-voltage current source is turned off and the PWM modulator and output transistor are activated, as shown in Figure 5(a). During normal operation (when the output voltage is regulated) feedback control current supplies the $V_C$ supply current. The shunt regulator keeps $V_C$ at typically 5.7 V by shunting CONTROL pin feedback current exceeding the required DC supply current through the PWM error signal sense resistor $R_E$. The low dynamic impedance of this pin ($Z_C$) sets the gain of the error amplifier when used in a primary feedback configuration. The dynamic impedance of the CONTROL pin together with the external resistance and capacitance determines the control loop compensation of the power system.

If the CONTROL pin external capacitance ($C_T$) should discharge to the lower threshold, then the output MOSFET is turned off and the control circuit is placed in a low-current standby mode. The high-voltage current source turns on and charges the external capacitance again. Charging current is shown with a negative polarity and discharging current is shown with a positive polarity in Figure 6. The hysteretic auto-restart comparator keeps $V_C$ within a window of typically 4.7 to 5.7 V by turning the high-voltage current source on and off as shown in Figure 5(b). The auto-restart circuit has a divide-by-8 counter which prevents the output MOSFET from turning on again until eight discharge-charge cycles have elapsed. The counter effectively limits *TOPSwitch* power dissipation by reducing the auto-restart duty cycle to typically 5%. Auto-restart continues to cycle until output voltage regulation is again achieved.

**Bandgap Reference**
All critical *TOPSwitch* internal voltages are derived from a temperature-compensated bandgap reference. This reference is also used to generate a temperature-compensated current source which is trimmed to accurately set the oscillator frequency and MOSFET gate drive current.

**Oscillator**
The internal oscillator linearly charges and discharges the internal capacitance between two voltage levels to create a sawtooth waveform for the pulse width modulator. The oscillator sets the pulse width modulator/current limit latch at the beginning of each cycle. The nominal frequency of 100 kHz was chosen to minimize EMI and maximize efficiency in power supply applications. Trimming of the current reference improves oscillator frequency accuracy.

**Pulse Width Modulator**
The pulse width modulator implements a voltage-mode control loop by driving the output MOSFET with a duty cycle inversely proportional to the current flowing into the CONTROL pin which generates a voltage error signal across $R_E$. The error signal across $R_E$ is filtered by an RC network with a typical corner frequency of 7 kHz to reduce the effect of switching noise. The filtered error signal is compared with the internal oscillator sawtooth waveform to generate the duty cycle waveform. As the control current increases, the duty cycle decreases. A clock signal from the oscillator sets a latch which turns on the output MOSFET. The pulse width modulator resets the latch, turning off the output MOSFET. The maximum duty cycle is set by the symmetry of the internal oscillator. The modulator has a minimum ON-time to keep the current consumption of the *TOPSwitch* independent of the error signal. Note that a minimum current must be driven into the CONTROL pin before the duty cycle begins to change.

**Gate Driver**
The gate driver is designed to turn the output MOSFET on at a controlled rate to minimize common-mode EMI. The gate drive current is trimmed for improved accuracy.

**Error Amplifier**
The shunt regulator can also perform the function of an error amplifier in primary feedback applications. The shunt regulator voltage is accurately derived from the temperature compensated bandgap reference. The gain of the error amplifier is set by the CONTROL pin dynamic impedance. The CONTROL pin clamps external circuit signals to the $V_C$ voltage level. The CONTROL pin current in excess of the supply current is separated by the shunt regulator and flows through $R_E$ as a voltage error signal.

**Cycle-By-Cycle Current Limit**
The cycle by cycle peak drain current limit circuit uses the output MOSFET ON-resistance as a sense resistor. A current limit comparator compares the output MOSFET ON-state drain-source voltage, $V_{DS(ON),}$ with a threshold voltage. High drain current causes $V_{DS(ON)}$ to exceed the threshold voltage and turns

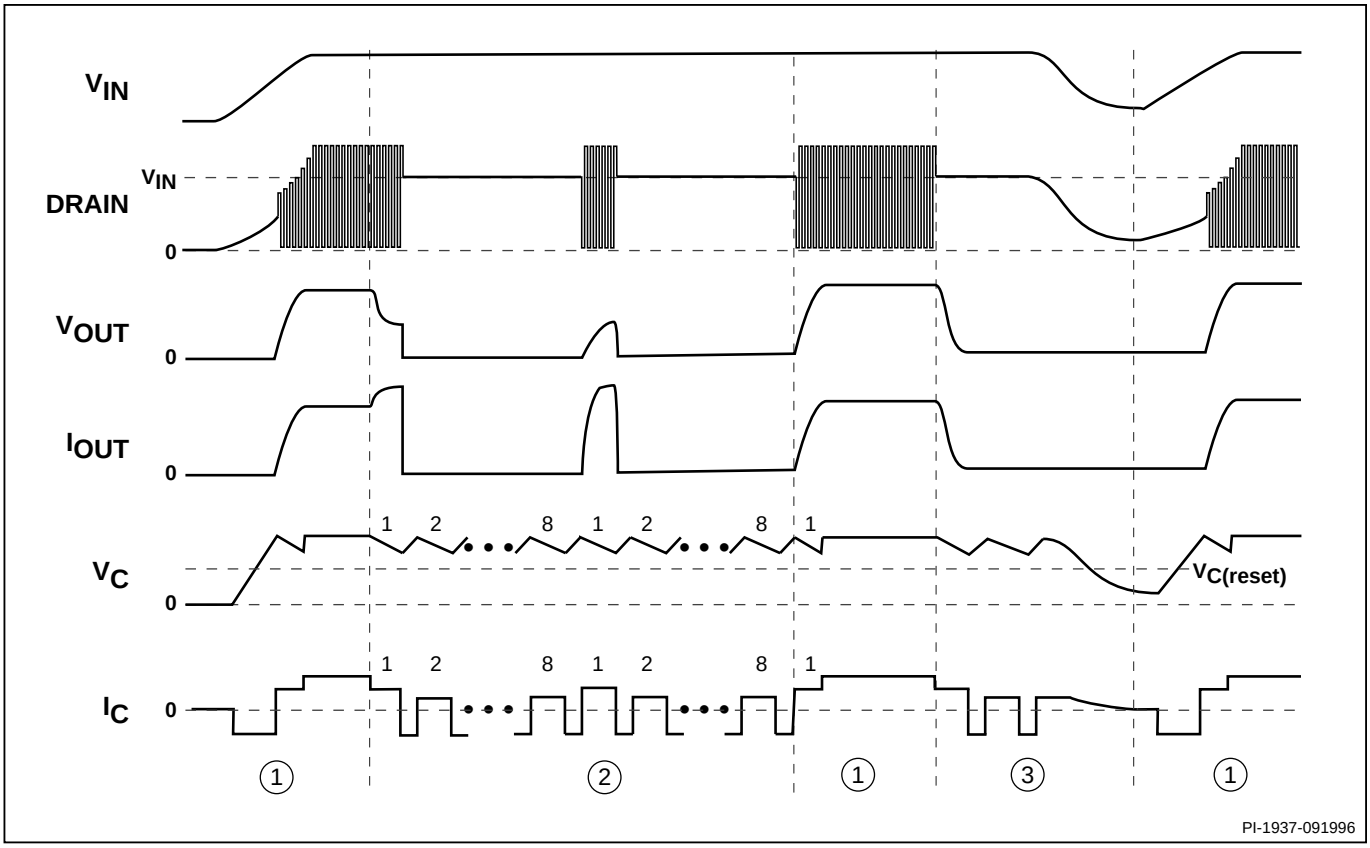



*Figure 6. Typical Waveforms for (1) Normal Operation, (2) Auto-restart, and (3) Power Down Reset.*

the output MOSFET off until the start of the next clock cycle. The current limit comparator threshold voltage is temperature compensated to minimize variation of the effective peak current limit due to temperature related changes in output MOSFET $R_{DS(ON)}$.

The leading edge blanking circuit inhibits the current limit comparator for a short time after the output MOSFET is turned on. The leading edge blanking time has been set so that current spikes caused by primary-side capacitances and secondary-side rectifier reverse recovery time will not cause premature termination of the switching pulse.

The current limit can be lower for a short period after the leading edge blanking time as shown in Figure 12. This is due to dynamic characteristics of the MOSFET. To avoid triggering the current limit in normal operation, the drain current waveform should stay within the envelope shown.

**Shutdown/Auto-restart**

To minimize *TOPSwitch* power dissipation, the shutdown/auto-restart circuit turns the power supply on and off at an auto-restart duty cycle of typically 5% if an out of regulation condition persists. Loss of regulation interrupts the external current into the CONTROL pin. $V_C$ regulation changes from shunt mode to the hysteretic auto-restart mode described above. When the fault condition is removed, the power supply output becomes regulated, $V_C$ regulation returns to shunt mode, and normal operation of the power supply resumes.

**Overtemperature Protection**

Temperature protection is provided by a precision analog circuit that turns the output MOSFET off when the junction temperature exceeds the thermal shutdown temperature (typically 135°C). Activating the power-up reset circuit by removing and restoring input power or momentarily pulling the CONTROL pin below the power-up reset threshold resets the latch and allows *TOPSwitch* to resume normal power supply operation. $V_C$ is regulated in hysteretic mode and a 4.7 V to 5.7 V (typical) sawtooth waveform is present on the CONTROL pin when the power supply is latched off.

**High-voltage Bias Current Source**

This current source biases *TOPSwitch* from the DRAIN pin and charges the CONTROL pin external capacitance ($C_T$) during start-up or hysteretic operation. Hysteretic operation occurs during auto-restart and overtemperature latched shutdown. The current source is switched on and off with an effective duty cycle of approximately 35%. This duty cycle is determined by the ratio of CONTROL pin charge ($I_C$) and discharge currents ($I_{CD1}$ and $I_{CD2}$). This current source is turned off during normal operation when the output MOSFET is switching.

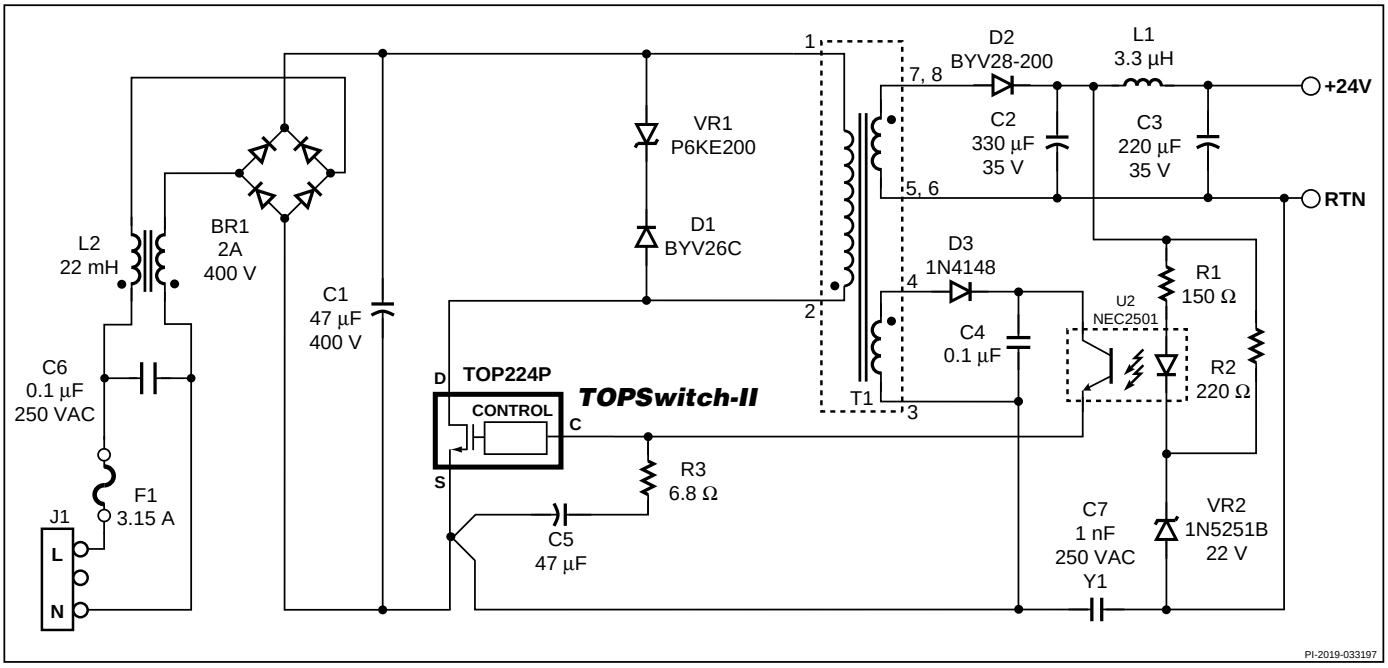



*Figure 7. Schematic Diagram of a 20 W Universal Input TOPSwitch Power Supply using an 8 lead PDIP without heat sink.*

## Application Examples

Following are just two of the many possible *TOPSwitch* implementations. Refer to the Data Book and Design Guide for additional examples.

### 20W Universal Supply using 8 Lead PDIP

Figure 7 shows a 24V, 20W secondary regulated flyback power supply using the TOP224P *TOPSwitch* in eight lead PDIP package and operating from universal 85 to 265 VAC input voltage. This example demonstrates the advantage of the higher power 8 pin leadframe used with the *TOPSwitch-II* family. This low cost package allows heat to be transfered to the board through six source pins eliminating the heatsink and the associated cost. Efficiency is typically 80% at low line input which is the worst case. Output voltage is directly sensed by optocoupler U2 and Zener diode VR2. The output voltage is determined by the Zener diode (VR2) voltage and the voltage drops across the optocoupler (U2) photodiode and resistor R1. Other output voltages are possible by adjusting the transformer turns ratio and value of Zener diode VR2.

AC power is rectified and filtered by BR1 and C1 to create the high voltage DC bus applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated *TOPSwitch* high-voltage MOSFET. D1 and VR1 clamp leading-edge voltage spikes caused by transformer leakage inductance. The power secondary winding is rectified and filtered by D2, C2, L1, and C3 to create the 24V output voltage. R2 and VR2 provide a slight pre-load on the 24V output to improve load regulation at light loads. The bias winding is rectified and filtered by D3 and C4 to create a *TOPSwitch* bias voltage. L2 and Y1-safety capacitor C7 attenuate common mode emission currents caused by high voltage switching waveforms on the Drain side of the primary winding and the primary to secondary capacitance. Leakage inductance of L2 and C6 attenuate differential-mode emission currents caused by the fundamental and harmonics of the trapezoidal or triangular primary current waveform. C5 filters internal MOSFET gate drive charge current spikes on the CONTROL pin, determines the auto-restart frequency, and together with R1 and R3, compensate the control loop.

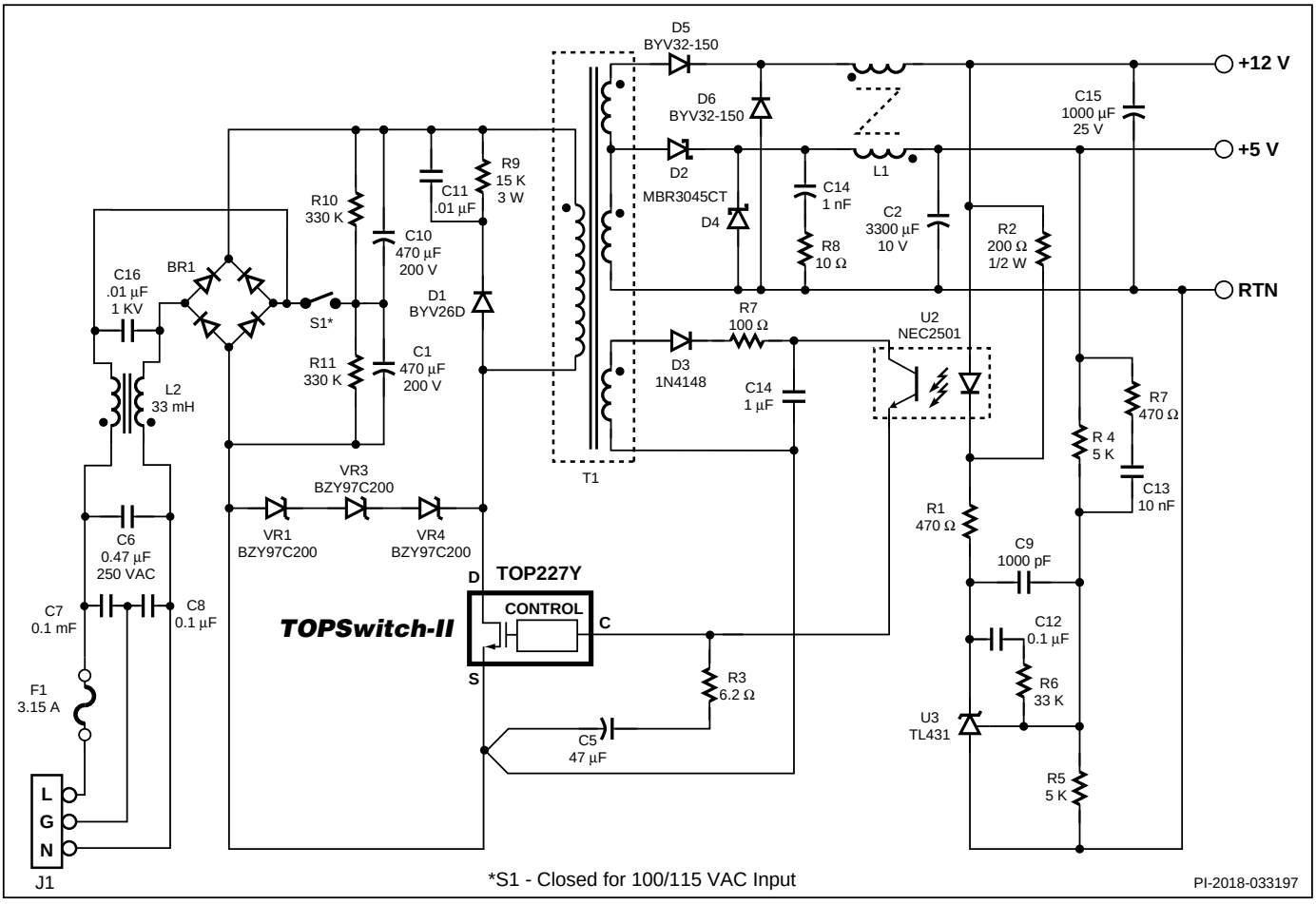



*Figure 8. Schematic Diagram of a 150 W TOPSwitch PC Main Power Supply.*

### 150W Foward Converter

Figure 8 shows a 5/12V, 150W forward power supply using the TOP227Y *TOPSwitch* in a TO-220 Package operating from 110/115/230 VAC input voltage. Efficiency is typically 80% at low line input which is the worst case. Output voltage is directly sensed and accurately regulated by a secondary referenced error amplifier. Error amplifier U3 drives a current error signal through optocoupler U2 into the *TOPSwitch* CONTROL pin to directly control *TOPSwitch* duty cycle. Output voltage can be fine-tuned by adjusting divider resistors R4 and R5. Other output voltages are possible by adjusting the transformer turns ratio.

AC input is doubled and/or rectified by BR1 and S1 to charge energy storage capacitors C1 and C10 which creates a high voltage DC bus applied to the primary winding of T1. R10 and R11 bleed off charge on these capacitors when AC power is turned off. The other side of the transformer primary is driven by the integrated *TOPSwitch* high-voltage MOSFET. D1, R9, C11, VR1, VR3, and VR4 provide transformer reset and clamp leading-edge voltage spikes caused by transformer leakage inductance when *TOPSwitch* turns off. The 5V power secondary winding is rectified and filtered by D2, D4, C2, and L1. The 12V power secondary winding is rectified and filtered by D5, D6, C15, and a second winding on L1. R8 and C14 damp ringing across D4. The bias winding is rectified and filtered by D3, R7, and C4 to create a *TOPSwitch* bias voltage. L2 and Y2-safety capacitors C7 and C8 attenuate common mode emission currents caused by high voltage switching waveforms on the Drain side of the primary winding and the primary to secondary capacitance. Leakage of L2 , C6, and C16 attenuate differential-mode emission currents caused by the fundamental and harmonics of the trapezoidal or triangular primary current waveform. C5 filters internal MOSFET gate drive charge current spikes on the CONTROL pin, determines the auto-restart frequency, and together with R1 and R3, help compensate the control loop.

The TL431 shunt regulator (U3) integrates an accurate 2.5V bandgap reference, op amp, and driver into a single device used as a secondary-referenced error amplifier. Output voltage is sensed, divided by R4 and R5, and compared with the internal reference. C9, R4, and R6 determine error amplifier frequency

response. R1 limits U2 LED current and sets overall control loop AC gain. R2 provides minimum loading to improve output voltage regulation under light load conditions. C9 rolls off error amplifier gain at high frequencies. R7 and C13 reduce turn on overshoot and improve transient response.

## Key Application Considerations

There is no external latching shutdown function (available only on earlier *TOPSwitch* devices.)

Keep the SOURCE pin length very short. Use a Kelvin connection to the SOURCE pin for the CONTROL pin bypass capacitor. Use single point grounding techniques at the SOURCE pin as shown in Figure 9.

Minimize peak voltage and ringing on the DRAIN voltage at turn-off. Use a Zener or TVS Zener diode to clamp the DRAIN voltage below the breakdown voltage rating of *TOPSwitch* under all conditions.

Do not plug *TOPSwitch* into a "hot" IC socket during test. External CONTROL pin capacitance may be charged to excessive voltage and causes *TOPSwitch* damage.

While performing *TOPSwitch* device tests, do not exceed maximum CONTROL pin voltage of 9 V or maximum CONTROL pin current of 100 mA.

Under some conditions, externally provided bias or supply current driven into the CONTROL pin can hold the *TOPSwitch* in one of the 8 auto-restart cycles indefinitely and prevent starting. To avoid this problem when doing bench evaluations, it is recommended that the $V_C$ power supply be turned on before the DRAIN voltage is applied. *TOPSwitch* can also be reset by shorting the CONTROL pin to the SOURCE pin momentarily.

CONTROL pin currents during auto-restart operation are much lower at low input voltages (< 20 V) which increases the auto-restart cycle time (see the $I_C$ vs. Drain Voltage Characteristic curve).

Short interruptions of AC power may cause *TOPSwitch* to enter the 8-count auto-restart cycle before starting again. This is because the input energy storage capacitors are not completely discharged and the CONTROL pin capacitance has not discharged below the internal power-up reset voltage.

In some cases, minimum loading may be necessary to keep a lightly loaded or unloaded output voltage within the desired range due to the minimum ON-time.

For additional applications information regarding the *TOPSwitch* family, refer to AN-14 through AN-20.

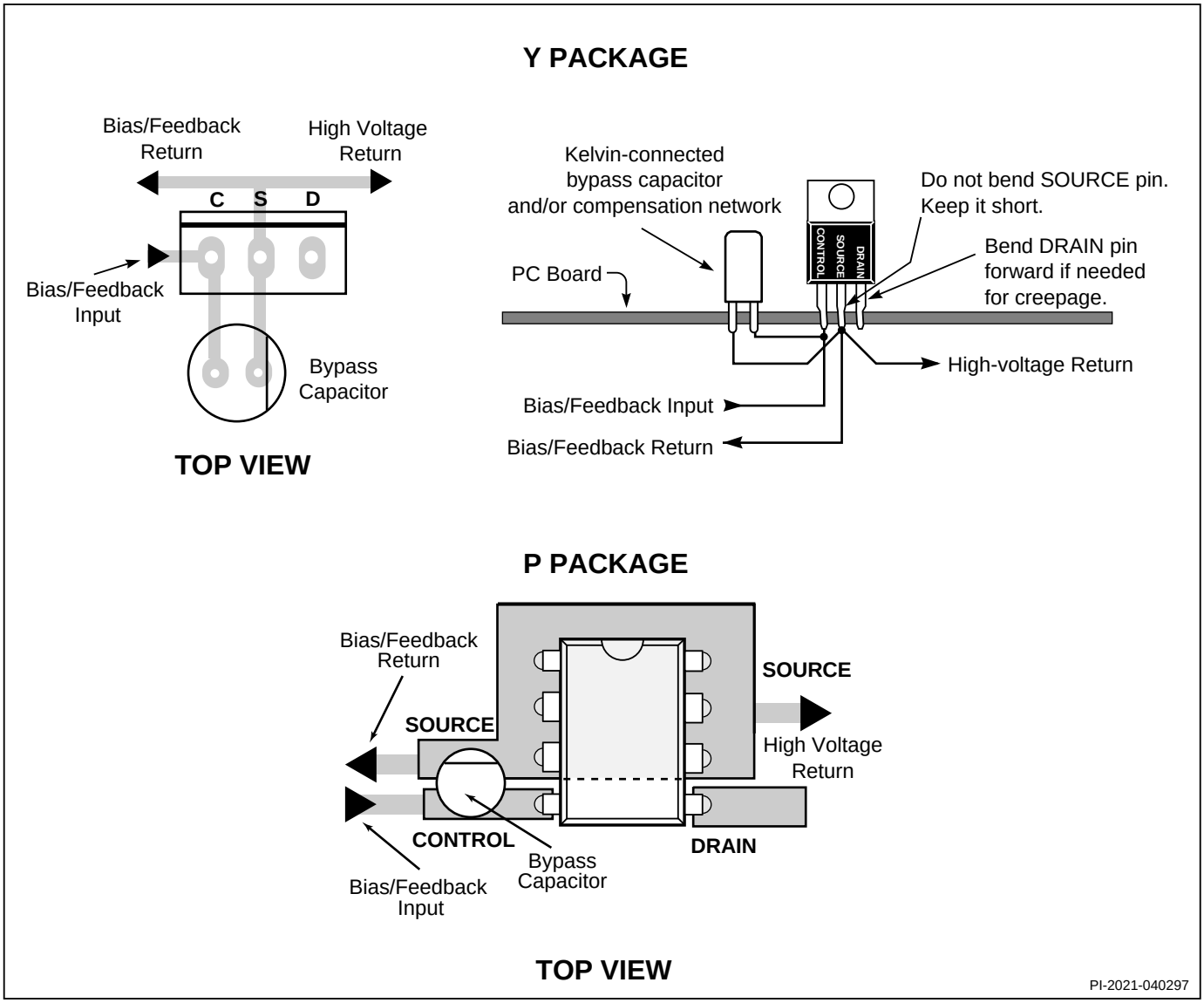



*Figure 9. Recommended TOPSwitch Layout.*

## ABSOLUTE MAXIMUM RATINGS(1)

DRAIN Voltage ..... -0.3 to 700 V
DRAIN Current Change in 100ns except during blanking time ..... 0.1 x $I_{LIMIT(MAX)}$ (2)
CONTROL Voltage ..... - 0.3 V to 9 V
CONTROL Current ..... 100 mA
Storage Temperature ..... -65 to 125°C
Operating Junction Temperature(3) ..... -40 to 150°C
Lead Temperature(4) ..... 260°C
Thermal Impedance: Y Package ($\theta_{JA}$)..... 70°C/W
($\theta_{JC}$)(5)..... 2°C/W
P Package ($\theta_{JA}$)(6)..... 35°C/W
($\theta_{JA}$)(7)..... 30°C/W

1. All voltages referenced to SOURCE, $T_A$ = 25°C.
2. See Figure 12.
3. Normally limited by internal circuitry.
4. 1/16" from case for 5 seconds.
5. Measured at tab closest to plastic interface.
6. Soldered, 0.36 square inch (232mm$^2$), 2 oz. copper clad.
7. Soldered, 1 square inch (645mm$^2$), 2 oz. copper clad.

| Parameter | Symbol | Conditions (Unless Otherwise Specified) See Figure 13 SOURCE = 0 V $T_j$ = -40 to 125°C | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **CONTROL FUNCTIONS** | | | | | | | |
| Output Frequency | $f_{OSC}$ | $I_C$ = 4 mA, $T_j$ = 25°C | | 90 | 100 | 110 | kHz |
| Maximum Duty Cycle | $D_{MAX}$ | $I_C = I_{CD1}$ + 0.5 mA, See Figure 10 | | 64 | 67 | 70 | % |
| Minimum Duty Cycle | $D_{MIN}$ | $I_C$ = 10 mA, See Figure 10 | | 0.7 | 1.7 | 2.7 | % |
| PWM Gain | | $I_C$ = 4 mA, $T_j$ = 25°C See Figure 4 | | -21 | -16 | -11 | %/mA |
| PWM Gain Temperature Drift | | See Note 1 | | | -0.05 | | %/mA/°C |
| External Bias Current | $I_B$ | See Figure 4 | | 0.8 | 2.0 | 3.3 | mA |
| Dynamic Impedance | $Z_C$ | $I_C$ = 4 mA, $T_j$ = 25°C See Figure 11 | | 10 | 15 | 22 | Ω |
| Dynamic Impedance Temperature Drift | | | | | 0.18 | | %/°C |
| **SHUTDOWN/AUTO-RESTART** | | | | | | | |
| CONTROL Pin Charging Current | $I_C$ | $T_j$ = 25°C | $V_C$ = 0 V | -2.4 | -1.9 | -1.2 | mA |
| | | | $V_C$ = 5 V | -2 | -1.5 | -0.8 | |
| Charging Current Temperature Drift | | See Note 1 | | | 0.4 | | %/°C |

| Parameter | Symbol | Conditions (Unless Otherwise Specified) See Figure 13 SOURCE = 0 V $T_j$ = -40 to 125°C | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **SHUTDOWN/AUTO-RESTART (cont.)** | | | | | | | |
| Auto-restart Threshold Voltage | $V_{C(AR)}$ | S1 open | | | 5.7 | | V |
| UV Lockout Threshold Voltage | | S1 open | | 4.4 | 4.7 | 5.0 | V |
| Auto-restart Hysteresis Voltage | | S1 open | | 0.6 | 1.0 | | V |
| Auto-restart Duty Cycle | | S1 open | | 2 | 5 | 8 | % |
| Auto-restart Frequency | | S1 open | | | 1.2 | | Hz |
| **CIRCUIT PROTECTION** | | | | | | | |
| Self-protection Current Limit | $I_{LIMIT}$ | di/dt = 40 mA/µs, $T_j$ = 25°C | TOP221Y<br>TOP221P | 0.23 | 0.25 | 0.276 | A |
| | | di/dt = 80 mA/µs, $T_j$ = 25°C | TOP222Y<br>TOP222P | 0.45 | 0.5 | 0.55 | |
| | | di/dt = 160 mA/µs, $T_j$ = 25°C | TOP223Y<br>TOP223P | 0.90 | 1.0 | 1.1 | |
| | | di/dt = 240 mA/µs, $T_j$ = 25°C | TOP224Y<br>TOP224P | 1.35 | 1.5 | 1.65 | |
| | | di/dt = 320 mA/µs, $T_j$ = 25°C | TOP225Y | 1.80 | 2.0 | 2.2 | |
| | | di/dt = 400 mA/µs, $T_j$ = 25°C | TOP226Y | 2.25 | 2.5 | 2.75 | |
| | | di/dt = 480 mA/µs, $T_j$ = 25°C | TOP227Y | 2.70 | 3.0 | 3.3 | |
| Initial Current Limit | $I_{INIT}$ | See Figure 12 Tj = 25°C | 85 VAC (Rectified Line Input) | 0.75 x $I_{LIMIT(MIN)}$ | | | A |
| | | | 265 VAC (Rectified Line Input) | 0.6 x $I_{LIMIT(MIN)}$ | | | |
| Leading Edge Blanking Time | $t_{LEB}$ | $I_C$ = 4 mA | | | 180 | | ns |

| Parameter | Symbol | Conditions (Unless Otherwise Specified) See Figure 13 SOURCE = 0 V $T_j$ = -40 to 125°C | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **CIRCUIT PROTECTION (cont.)** | | | | | | | |
| Current Limit Delay | $t_{ILD}$ | $I_C$ = 4 mA | | | 100 | | ns |
| Thermal Shutdown Temperature | | $I_C$ = 4 mA | | 125 | 135 | | °C |
| Power-up Reset Threshold Voltage | $V_{C(RESET)}$ | S2 open | | 2.0 | 3.3 | 4.2 | V |
| **OUTPUT** | | | | | | | |
| ON-State Resistance | $R_{DS(ON)}$ | TOP221 | $T_j$ = 25°C | | 31.2 | 36.0 | Ω |
| | | $I_D$ = 25 mA | $T_j$ = 100°C | | 51.4 | 60.0 | |
| | | TOP222 | $T_j$ = 25°C | | 15.6 | 18.0 | |
| | | $I_D$ = 50 mA | $T_j$ = 100°C | | 25.7 | 30.0 | |
| | | TOP223 | $T_j$ = 25°C | | 7.80 | 9.00 | |
| | | $I_D$ = 100 mA | $T_j$ = 100°C | | 12.9 | 15.0 | |
| | | TOP224 | $T_j$ = 25°C | | 5.20 | 6.00 | |
| | | $I_D$ = 150 mA | $T_j$ = 100°C | | 8.60 | 10.0 | |
| | | TOP225 | $T_j$ = 25°C | | 3.90 | 4.50 | |
| | | $I_D$ = 200 mA | $T_j$ = 100°C | | 6.40 | 7.50 | |
| | | TOP226 | $T_j$ = 25°C | | 3.10 | 3.60 | |
| | | $I_D$ = 250 mA | $T_j$ = 100°C | | 5.20 | 6.00 | |
| | | TOP227 | $T_j$ = 25°C | | 2.60 | 3.00 | |
| | | $I_D$ = 300 mA | $T_j$ = 100°C | | 4.30 | 5.00 | |
| OFF-State Current | $I_{DSS}$ | See Note 2 $V_{DS}$ = 560 V, $T_A$ = 125°C | | | | 250 | µA |
| Breakdown Voltage | $BV_{DSS}$ | See Note 2 $I_D$ = 100 µA, $T_A$ = 25°C | | 700 | | | V |
| Rise Time | $t_r$ | Measured in a Typical Flyback Converter Application. | | | 100 | | ns |
| Fall Time | $t_f$ | | | | 50 | | ns |

| Parameter | Symbol | Conditions (Unless Otherwise Specified) See Figure 13 SOURCE = 0 V $T_j$ = -40 to 125°C | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **OUTPUT (cont.)** | | | | | | | |
| DRAIN Supply Voltage | | See Note 3 | | 36 | | | V |
| Shunt Regulator Voltage | $V_{C(SHUNT)}$ | $I_C$ = 4 mA | | 5.4 | 5.7 | 6.0 | V |
| Shunt Regulator Temperature Drift | | | | | ±50 | | ppm/°C |
| CONTROL Supply/ Discharge Current | $I_{CD1}$ | Output MOSFET enabled | TOP221-224 | 0.6 | 1.2 | 1.6 | mA |
| | | | TOP225-227 | 0.7 | 1.4 | 1.8 | |
| | $I_{CD2}$ | Output MOSFET Disabled | | 0.5 | 0.8 | 1.1 | |

**NOTES:**

1. For specifications with negative values, a negative temperature coefficient corresponds to an increase in magnitude with increasing temperature, and a positive temperature coefficient corresponds to a decrease in magnitude with increasing temperature.

2. The breakdown & leakage measurements can be accomplished as shown in Figure 14 by using the following sequence:

   a. The curve tracer should initially be set at 0 V. The base output should be adjusted through a voltage sequence of 0 V, 6.5 V, 4.2 V, and 6.5 V, as shown. The base current from the curve tracer should not exceed 100 mA. This Control Pin sequence interrupts the Auto Restart sequence and locks the *TOPSwitch* internal MOSFET in the OFF State.
   b. The breakdown and the leakage measurements can now be taken with the curve tracer. The maximum voltage from the curve tracer must be limited to 700 V under all conditions.

.

3. It is possible to start up and operate *TOPSwitch* at DRAIN voltages well below 36 V. However, the CONTROL pin charging current is reduced, which affects start-up time, auto-restart frequency, and auto-restart duty cycle. Refer to the characteristic graph on CONTROL pin charge current ($I_C$) vs. DRAIN voltage for low voltage operation characteristics.

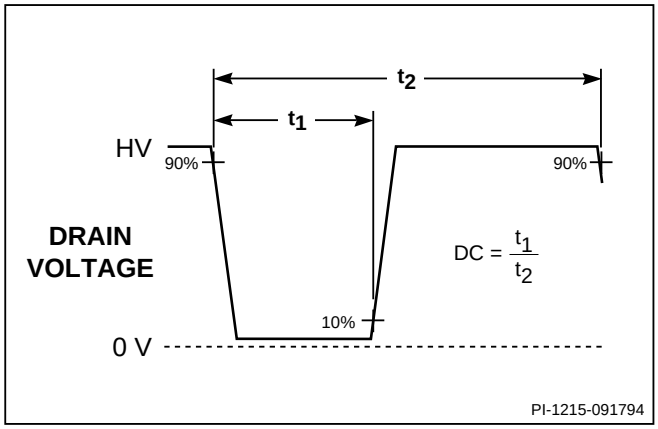



*Figure 10. TOPSwitch Duty Cycle Measurement.*

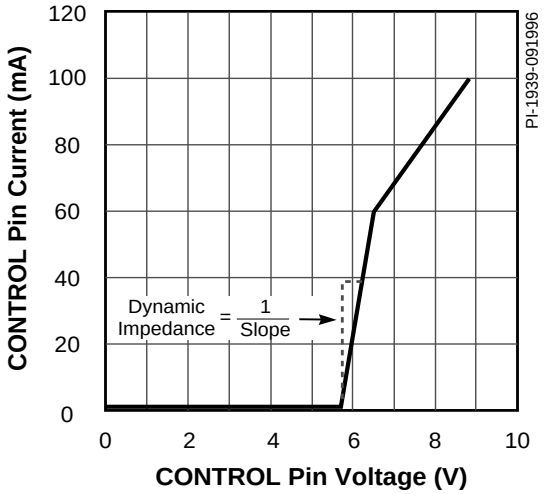



*Figure 11. TOPSwitch CONTROL Pin I-V Characteristic.*

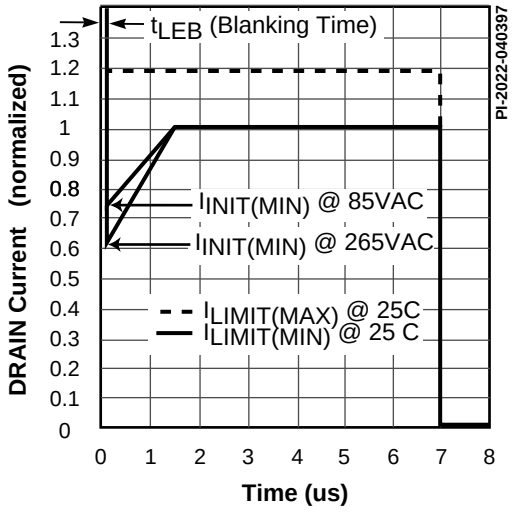



*Figure 12. Drain Current Operating Envelope.*

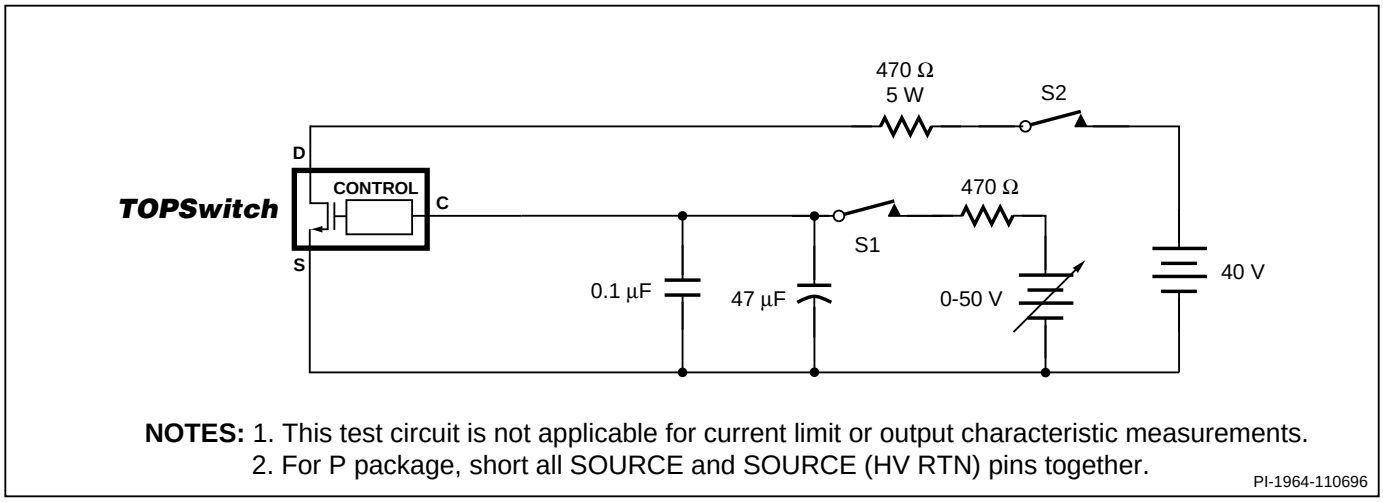



*Figure 13. TOPSwitch General Test Circuit.*

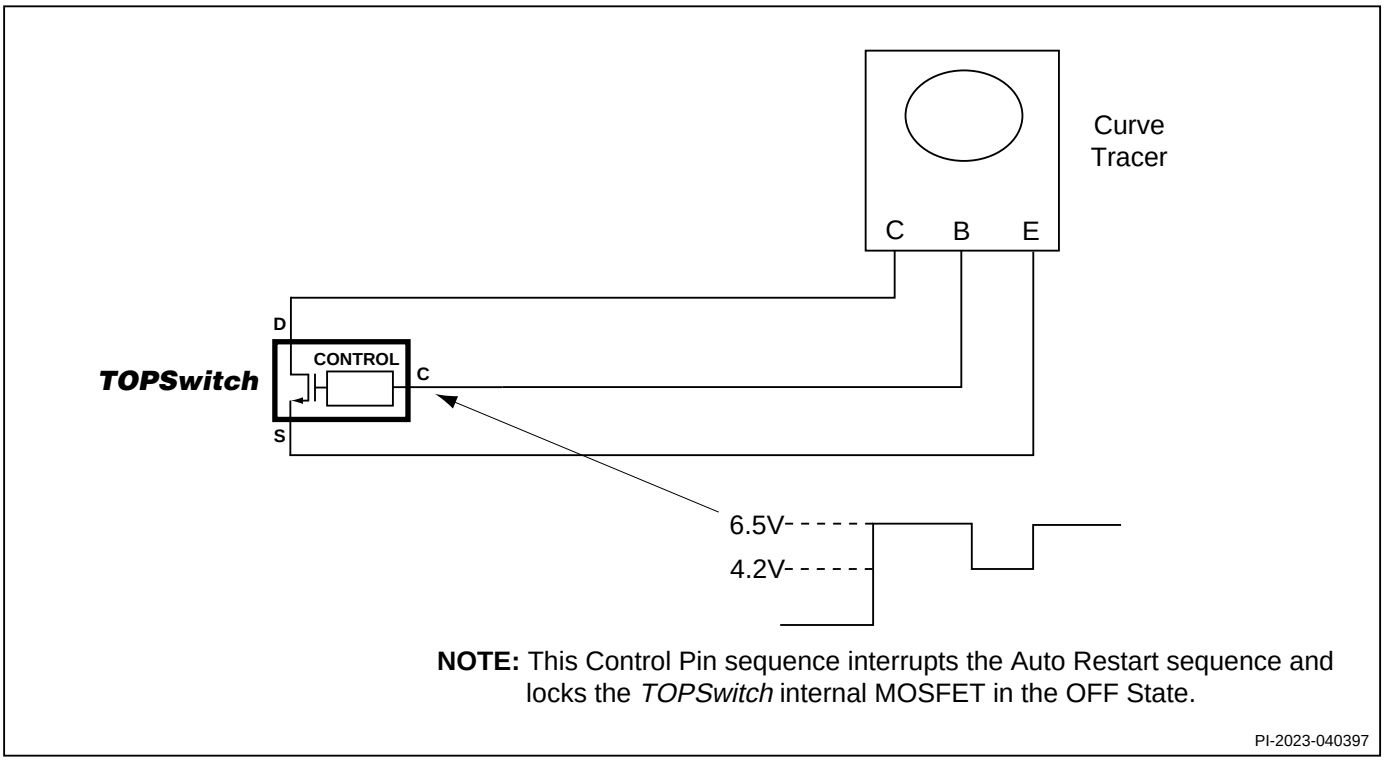



*Figure 14. Breakdown and Leakage Measurement Test Circuit.*

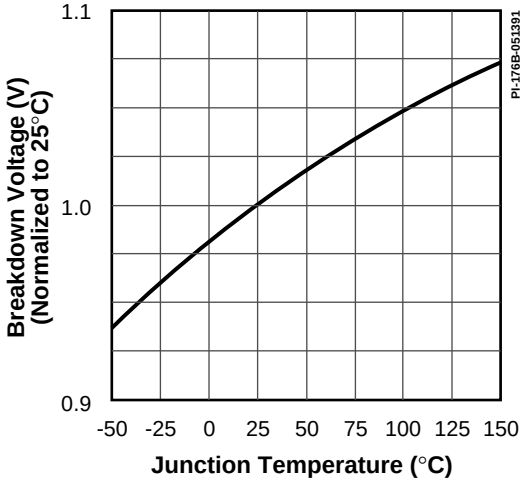
## BENCH TEST PRECAUTIONS FOR EVALUATION OF ELECTRICAL CHARACTERISTICS

The following precautions should be followed when testing *TOPSwitch* by itself outside of a power supply. The schematic shown in Figure 12 is suggested for laboratory testing of *TOPSwitch*.

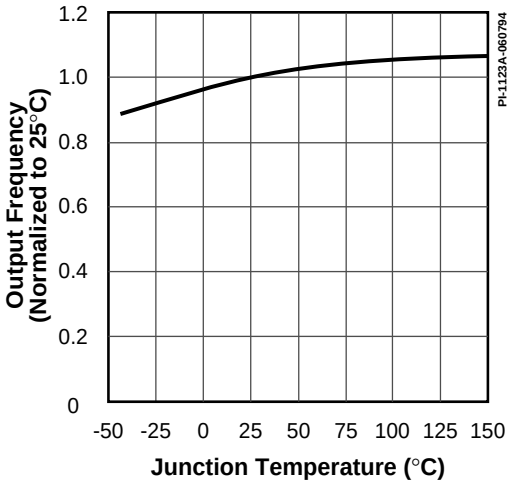
When the DRAIN supply is turned on, the part will be in the auto-restart mode. The control pin voltage will be oscillating at a low frequency from 4.7 to 5.7 V and the DRAIN is turned on every eighth cycle of the CONTROL pin oscillation. If the CONTROL pin power supply is turned on while in this auto-restart mode, there is only a 12.5% chance that the control pin oscillation will be in the correct state (DRAIN active state) so that the continuous DRAIN voltage waveform may be observed. It is recommended that the $V_C$ power supply be turned on first and the DRAIN power supply second if continuous drain voltage waveforms are to be observed. The 12.5% chance of being in the correct state is due to the 8:1 counter. Temporarily shorting the CONTROL pin to the SOURCE pin will reset *TOPSwitch* which then comes up in the current state.

## Typical Performance Characteristics

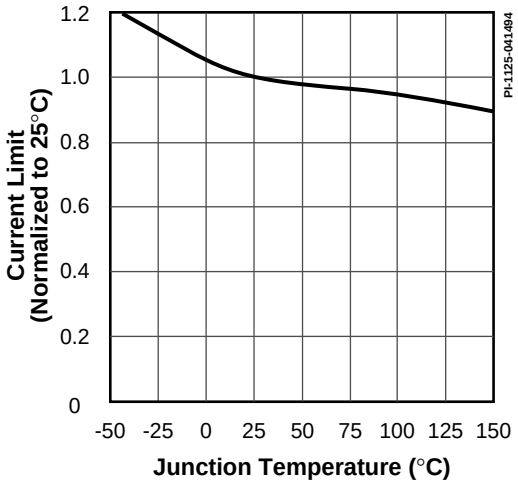
**BREAKDOWN vs. TEMPERATURE**



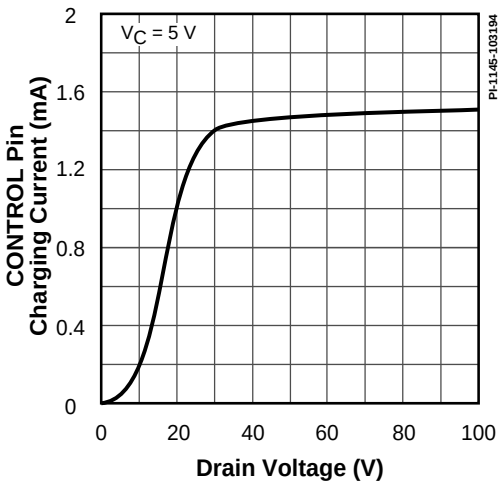

**FREQUENCY vs. TEMPERATURE**




**CURRENT LIMIT vs. TEMPERATURE**

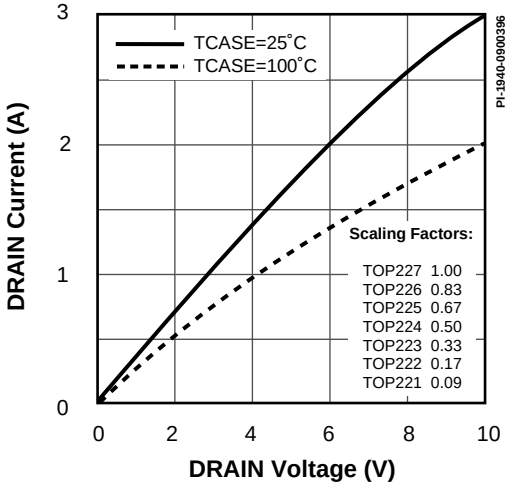



**$I_C$ vs. DRAIN VOLTAGE**

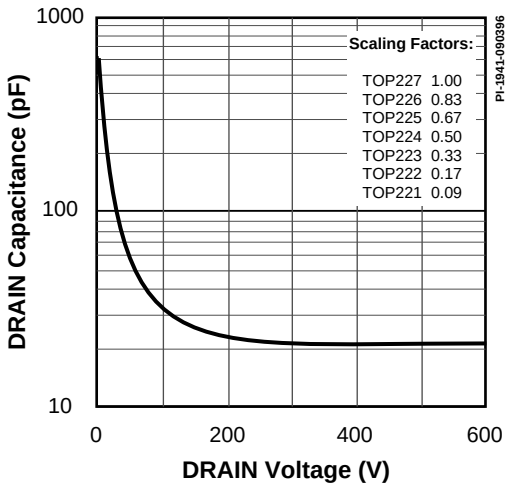


## Typical Performance Characteristics (cont.)

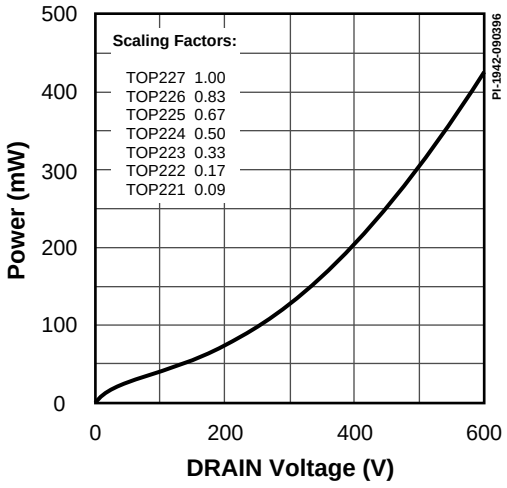
**OUTPUT CHARACTERISTICS**




**$C_{OSS}$ vs. DRAIN VOLTAGE**

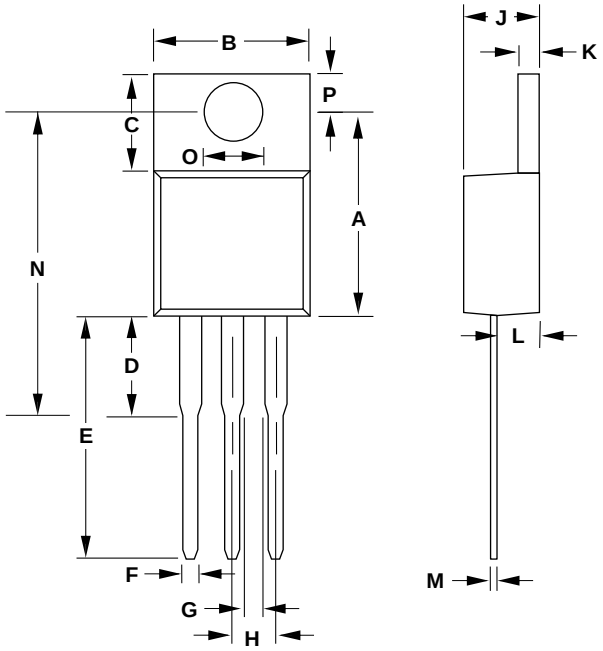



**DRAIN CAPACITANCE POWER**



## Y03A — Plastic TO-220/3

| DIM | inches | mm |
|---|---|---|
| A | .460-.480 | 11.68-12.19 |
| B | .400-.415 | 10.16-10.54 |
| C | .236-.260 | 5.99-6.60 |
| D | .240 - REF. | 6.10 - REF. |
| E | .520-.560 | 13.21-14.22 |
| F | .028-.038 | .71-.97 |
| G | .045-.055 | 1.14-1.40 |
| H | .090-.110 | 2.29-2.79 |
| J | .165-.185 | 4.19-4.70 |
| K | .045-.055 | 1.14-1.40 |
| L | .095-.115 | 2.41-2.92 |
| M | .015-.020 | .38-.51 |
| N | .705-.715 | 17.91-18.16 |
| O | .146-.156 | 3.71-3.96 |
| P | .103-.113 | 2.62-2.87 |




Notes:
1. Package dimensions conform to JEDEC specification TO-220 AB for standard flange mounted, peripheral lead package; .100 inch lead spacing (Plastic) 3 leads (issue J, March 1987)
2. Controlling dimensions are inches.
3. Pin numbers start with Pin 1, and continue from left to right when viewed from the top.
4. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15 mm) on any side.
5. Position of terminals to be measured at a position .25 (6.35 mm) from the body.
6. All terminals are solder plated.

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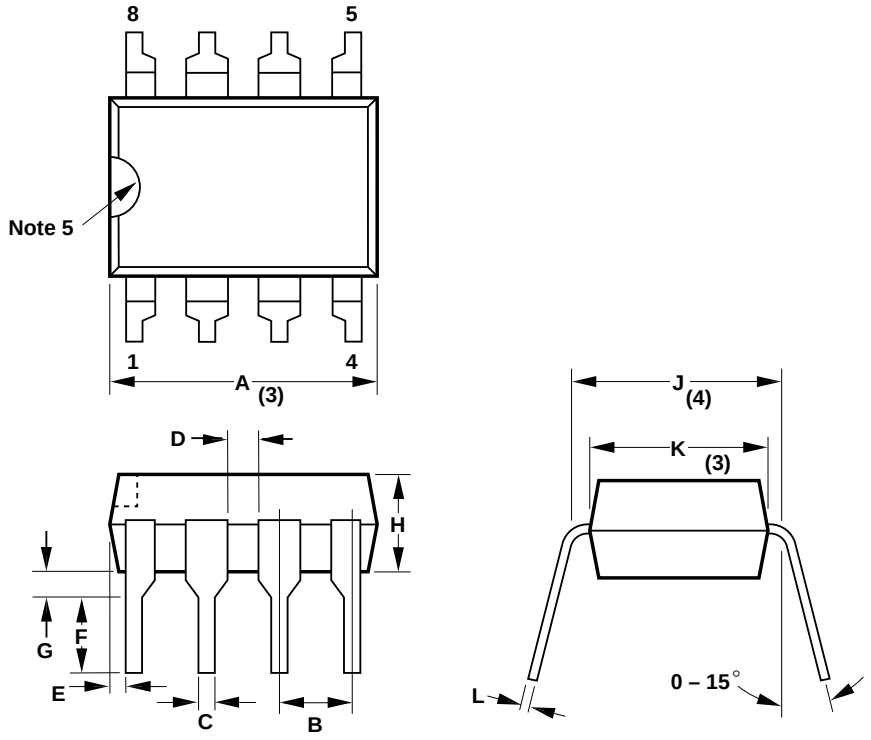
## P08A — Plastic DIP-8

| Dim. | inches | mm |
|---|---|---|
| A | .395 MAX | 10.03 MAX |
| B | .090-.110 | 2.29-2.79 |
| C | .015-.021 | 0.38-0.53 |
| D | .040 TYP | 1.02 TYP |
| E | .015-.030 | 0.38-0.76 |
| F | .125 MIN | 3.18 MIN |
| G | .015 MIN | 0.38 MIN |
| H | .125-.135 | 3.18-3.43 |
| J | .300-.320 | 7.62-8.13 |
| K | .245-.255 | 6.22-6.48 |
| L | .009-.015 | 0.23-0.38 |




Notes:
1. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 8 leads (issue B, 7/85).
2. Controlling dimensions: inches.
3. Dimensions are for the molded body and do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .010 inch (.25 mm) on any side.
4. These dimensions measured with the leads constrained to be perpendicular to package bottom.
5. Pin 1 orientation identified by end notch or dot adjacent to Pin 1.

PI-1842-050196

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