

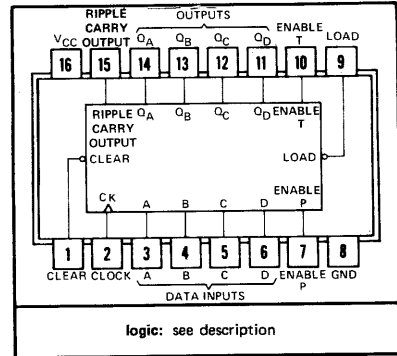
**TYPES SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A,
SN54S162, SN54S163, SN74160 THRU SN74163,
SN74LS160A THRU SN74LS163A, SN74S162, SN74S163
SYNCHRONOUS 4-BIT COUNTERS**

BULLETIN NO. DL-S 7611385, OCTOBER 1976

'160, '161, 'LS160A, 'LS161A . . . SYNCHRONOUS COUNTERS WITH DIRECT CLEAR
'162, '163, 'LS162A, 'LS163A, 'S162, 'S163 . . . FULLY SYNCHRONOUS COUNTERS

- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs

SERIES 54', 54LS', 54S' . . . J OR W PACKAGE
SERIES 74', 74LS', 74S' . . . J OR N PACKAGE
(TOP VIEW)



TYPE	TYPICAL PROPAGATION TIME, CLOCK TO Q OUTPUT	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'160 thru '163	14 ns	32 MHz	305 mW
'LS160A thru 'LS163A	14 ns	32 MHz	93 mW
'S162 and 'S163	9 ns	70 MHz	475 mW

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The '160, '162, 'LS160A, 'LS162A, and 'S162 are decade counters and the '161, '163, 'LS161A, 'LS163A, and 'S163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input of the '160 thru '163 or 'S163A or 'S162 should be avoided when the clock is low if the enable inputs are high at or before the transition. This restriction is not applicable to the 'LS160A thru 'LS163A. The clear function for the '160, '161, 'LS160A, and 'LS161A is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The clear function for the '162, '163, 'LS162A, 'LS163A, 'S162, and 'S163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL). Low-to-high transitions at the clear input of the '162 and '163 should be avoided when the clock is low if the enable and load inputs are high at or before the transition.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the QA output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the '160 thru '163 should occur only when the clock input is high. Transitions at the enable P or T inputs of the 'LS160A thru 'LS163A or 'S162 and 'S163 are allowed regardless of the level of the clock input.

'LS160A thru 'LS163A, 'S162 and 'S163 feature a fully independent clock circuit. Changes at control inputs (enable P or T, or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The 'LS160A thru 'LS163A are completely new designs. Compared to the original 'LS160 thru 'LS163, they feature 0-nanosecond minimum hold time and reduced input currents I_{IH} and I_{IL} .

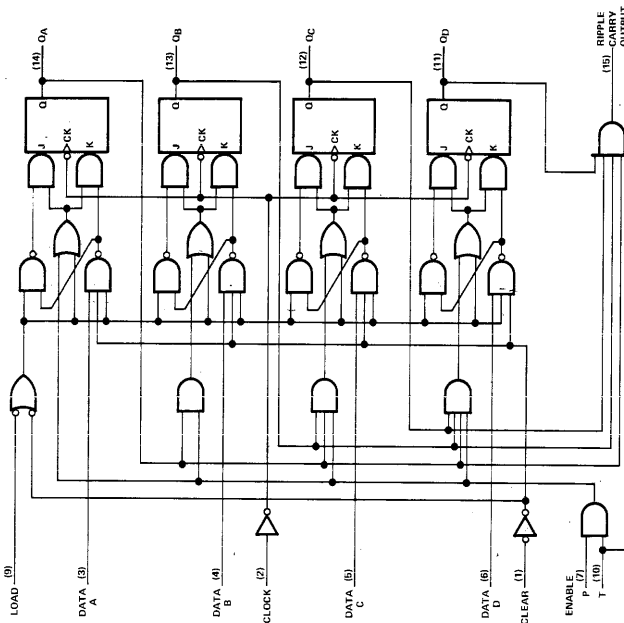
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TYPES SN54160 THRU SN54163, SN74160 THRU SN74163 SYNCHRONOUS 4-BIT COUNTERS

functional block diagrams

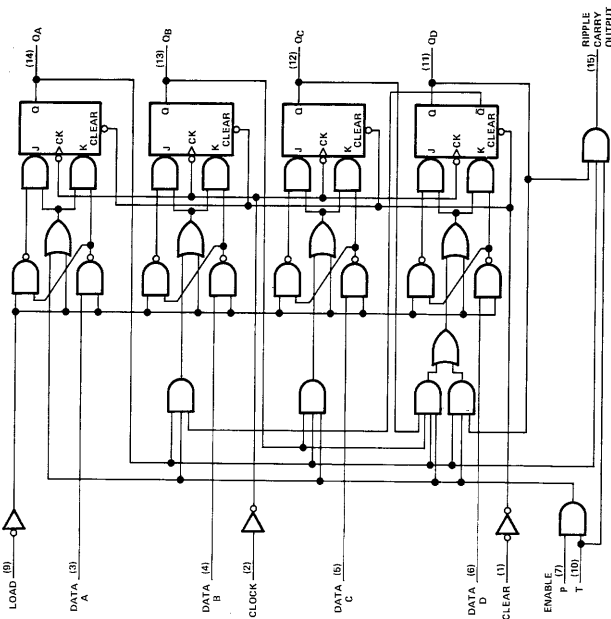
SN54163, SN74163 SYNCHRONOUS BINARY COUNTERS

SN54161, SN74161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54160, SN74160 decade counters at left.



SN54160, SN74160 SYNCHRONOUS DECADE COUNTERS

SN54162, SN74162 synchronous decade counters are similar; however, the clear is synchronous as shown for the SN54163, SN74163 binary counters at right.

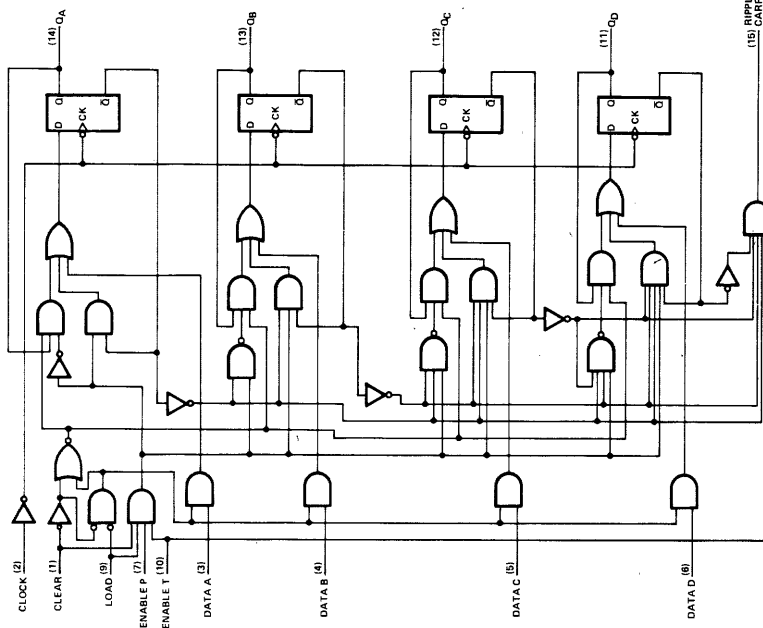


TYPES SN54LS160A THRU SN54LS163A, SN74LS160A THRU SN74LS163A SYNCHRONOUS 4-BIT COUNTERS

functional block diagram

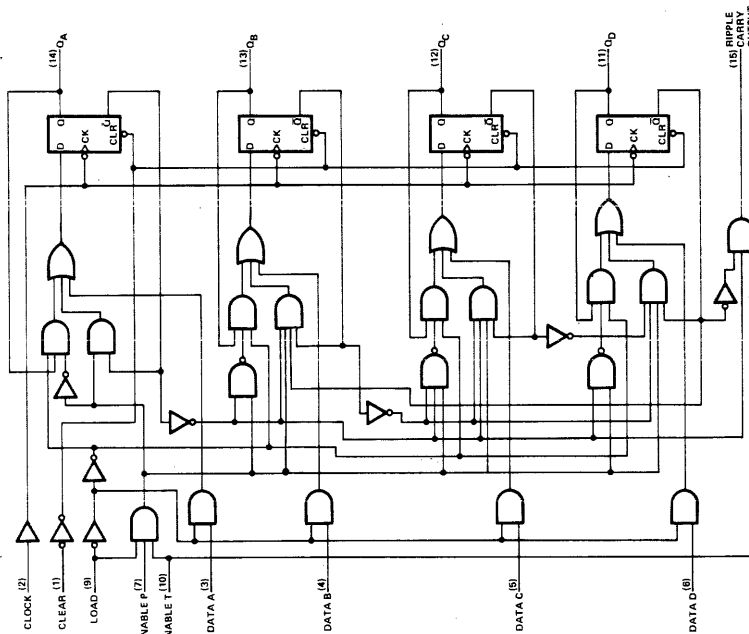
SN54LS163A, SN74LS163A SYNCHRONOUS BINARY COUNTERS

SN54LS161A, SN74LS161A synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54LS160A, SN74LS160A decade counters at left.



SN54LS160A, SN74LS160A SYNCHRONOUS DECADE COUNTERS

SN54LS162A, SN74LS162A synchronous decade counters are similar; however the clear is synchronous as shown for the SN54LS163A, SN74LS163A binary counters at right.



TENTATIVE DATA SHEET

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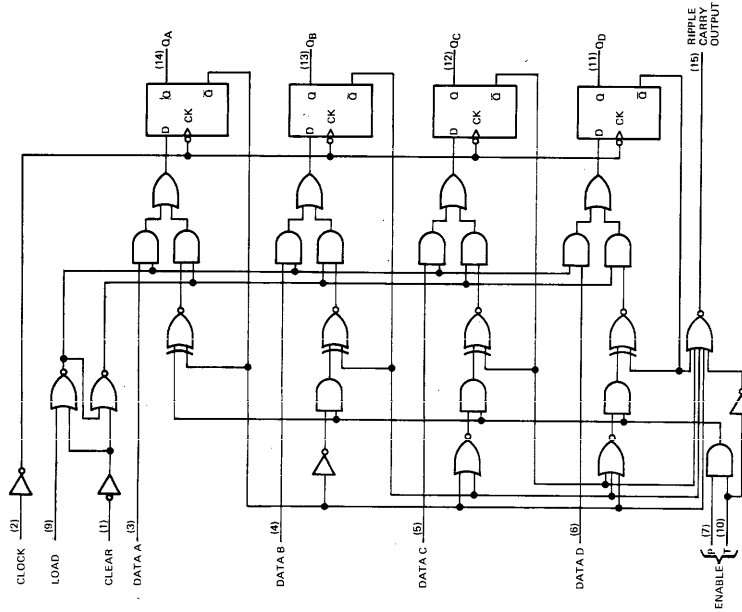
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TYPES SN54S162, SN54S163, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

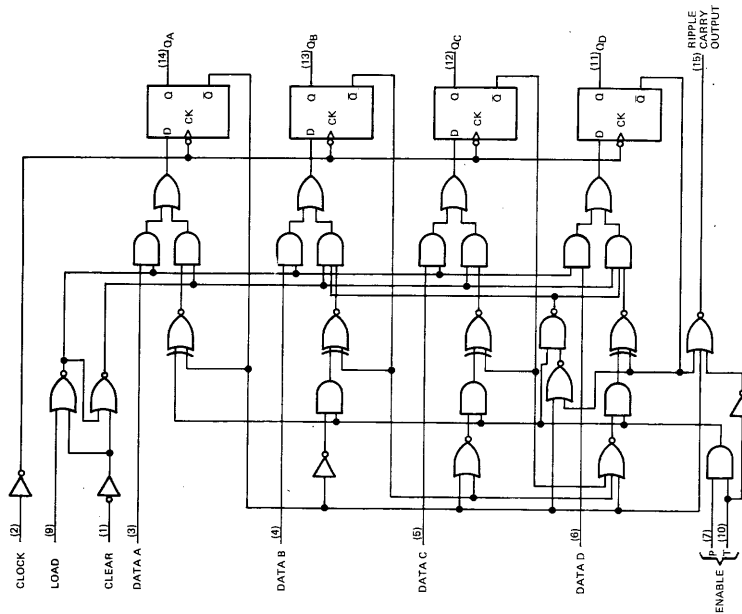
REVISED OCTOBER 1976

functional block diagrams

SN54S163, SN74S163 SYNCHRONOUS BINARY COUNTERS



SN54S162, SN74S162 SYNCHRONOUS DECADE COUNTERS



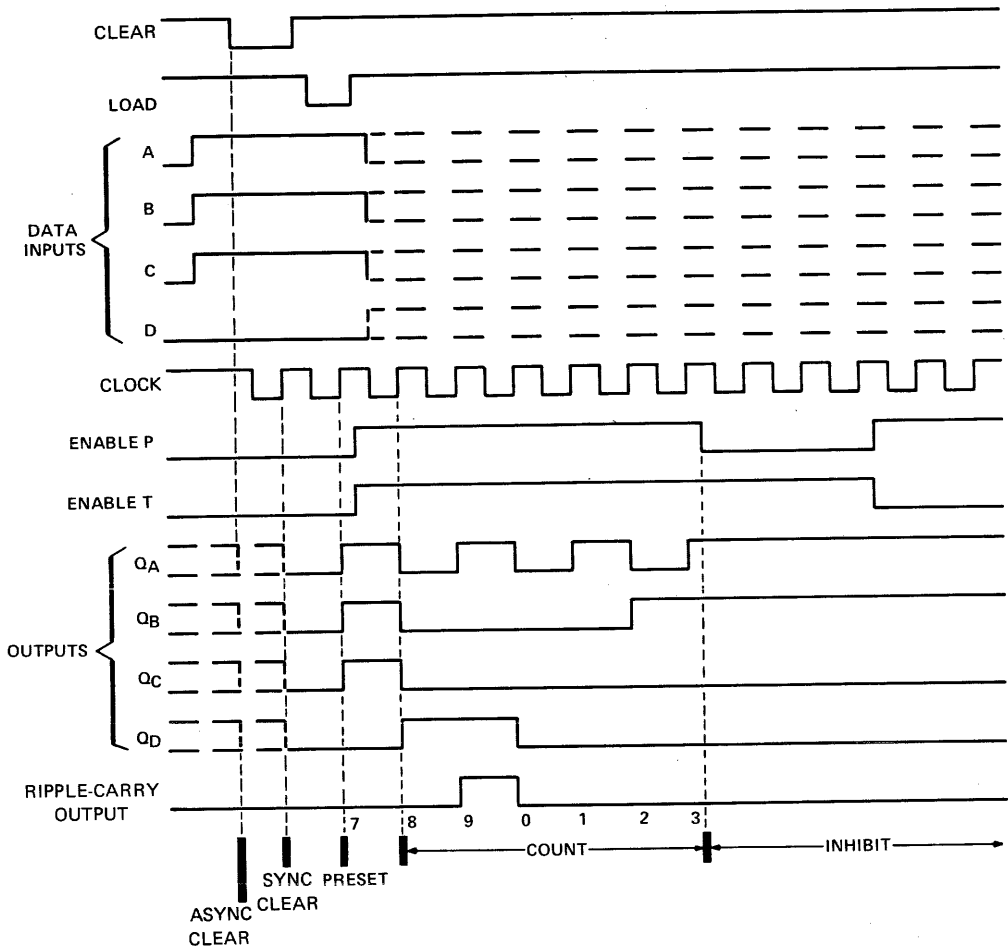
TYPES SN54160, SN54162, SN54LS160A, SN54LS162A, SN54S162, SN74160, SN74162, SN74LS160A, SN74LS162A, SN74S162 SYNCHRONOUS 4-BIT COUNTERS

'160, '162, 'LS160A, 'LS162A, 'S162 DECADE COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero ('160 and 'LS160A are asynchronous; '162, 'LS162A, and 'S162 are synchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit



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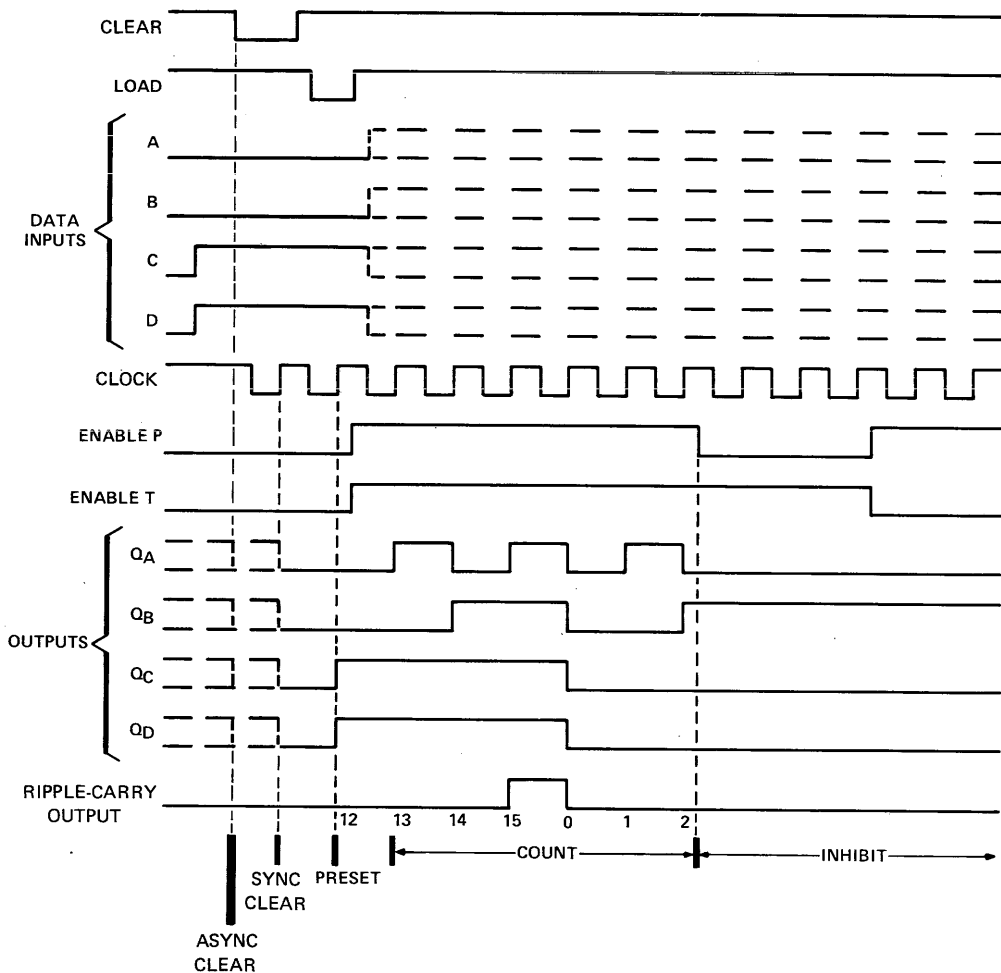
TYPES SN54161, SN54163, SN54LS161A, SN54LS163A, SN54S163, SN74161, SN74163, SN74LS161A, SN74LS163A, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

'161, 'LS161A, '163, 'LS163A, 'S163 BINARY COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero ('161 and 'LS161A are asynchronous; '163, 'LS163A, and 'S163 are synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen fifteen, zero, one, and two
4. Inhibit

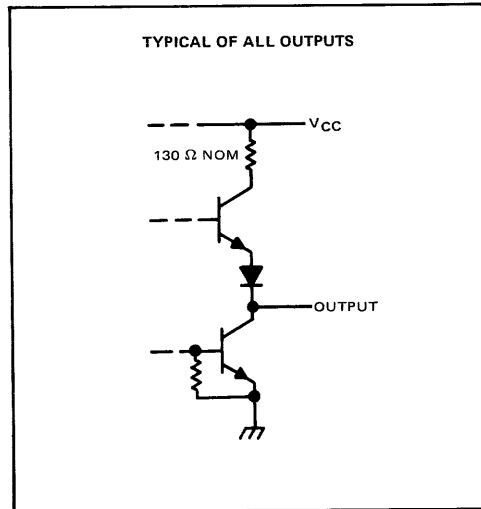
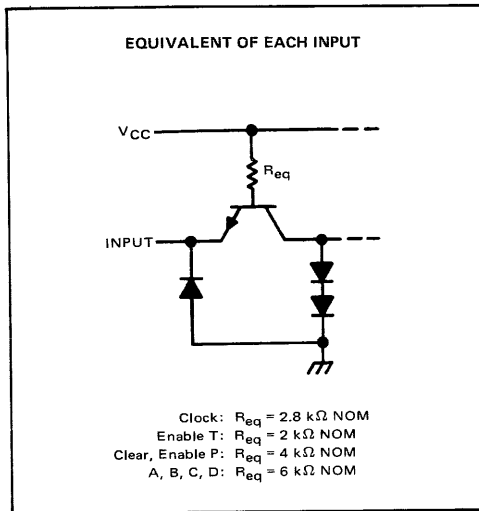


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TYPES SN54160 THRU SN54163, SN74160 THRU SN74163

SYNCHRONOUS 4-BIT COUNTERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54 ⁴ Circuits	-55°C to 125°C
SN74 ⁴ Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

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NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
 2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.

recommended operating conditions

	SN54160, SN54161 SN54162, SN54163			SN74160, SN74161 SN74162, SN74163			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0	25		0	25		MHz
Width of clock pulse, $t_{w(clock)}$	25			25			ns
Width of clear pulse, $t_{w(clear)}$	20			20			ns
Setup time, t_{su} (see Figures 1 and 2)	Data inputs A, B, C, D	20		20			ns
	Enable P	20		20			
	Load	25		25			
	Clear ^o	20		20			
Hold time at any input, t_h	0			0			ns
Operating free-air temperature, T_A	-55	125		0	70		°C

^oThis applies only for '162 and '163, which have synchronous clear inputs.

TYPES SN54160 THRU SN54163, SN74160 THRU SN74163 SYNCHRONOUS 4-BIT COUNTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54160, SN54161 SN54162, SN54163			SN74160, SN74161 SN74162, SN74163			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage		0.8			0.8			V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -12 mA	-1.5			-1.5			V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -800 μA	2.4	3.4		2.4	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA	0.2	0.4		0.2	0.4		V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V	1			1			mA
I _{IH}	High-level input current	Clock or enable T	80			80			μA
		Other inputs	40			40			
I _{IL}	Low-level input current	Clock or enable T	-3.2			-3.2			mA
		Other inputs	-1.6			-1.6			
I _{OS}	Short-circuit output current‡	V _{CC} = MAX	-20	-57		-18	-57		mA
I _{CCH}	Supply current, all outputs high	V _{CC} = MAX, See Note 3	59	85		59	94		mA
I _{CCL}	Supply current, all outputs low	V _{CC} = MAX, See Note 4	63	91		63	101		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTES: 3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER †	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
f _{max}			C _L = 15 pF, R _L = 400 Ω, See Figures 1 and 2 and Notes 5 and 6	25	32		ns	
‡ t _{PLH}	Clock	Ripple carry			23	35		ns
‡ t _{PHL}		Q			23	35		
‡ t _{PLH}	Clock (load input high)	Any			13	20		ns
‡ t _{PHL}		Q			15	23		
‡ t _{PLH}	Clock (load input low)	Any			17	25		ns
‡ t _{PHL}		Q			19	29		
‡ t _{PLH}	Enable T	Ripple carry			11	16		ns
‡ t _{PHL}		Any Q			11	16		
‡ t _{PHL}	Clear	Any Q			26	38		ns

† f_{max} = Maximum clock frequency

‡ t_{PLH} = propagation delay time, low-to-high-level output

‡ t_{PHL} = propagation delay time, high-to-low-level output

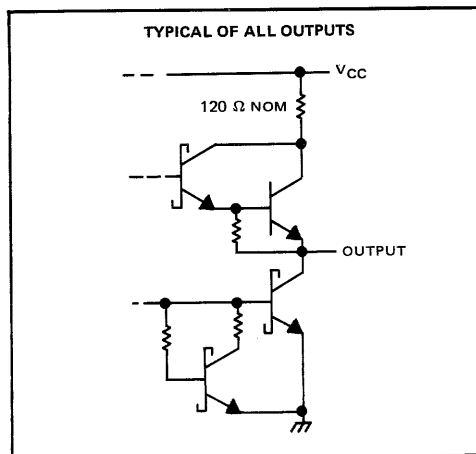
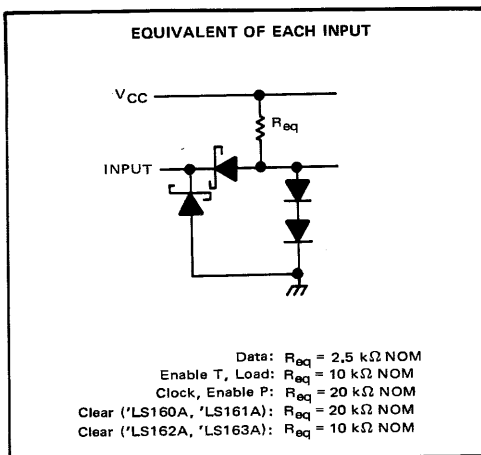
NOTES: 5. Load circuit is shown on page 3-10.

6. Propagation delay for clearing is measured from the clear input for the '160 and '161 or from the clock input transition for the '162 and '163.

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TYPES SN54LS160A, THRU SN54LS163A, SN74LS160A, THRU SN74LS163A, SYNCHRONOUS 4-BIT COUNTERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 7)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS' Circuits	-55°C to 125°C
SN74LS' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 7: Voltage values are with respect to network ground terminal.

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recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$	25		25				ns
Width of clear pulse, $t_{w(clear)}$	20		20				ns
Setup time, t_{SU} (see Figures 1 and 2)	Data inputs A, B, C, D	20		20			ns
	Enable P or T	20		20			
	Load	20		20			
	Clear [◇]	20		20			
Hold time at any input, t_H	0		0				ns
Operating free-air temperature, T_A	-55		125	0		70	°C

[◇] This applies only for 'LS162 and 'LS163, which have synchronous clear inputs.

TENTATIVE DATA

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TYPES SN54LS160A THRU SN54LS163A, SN74LS160A THRU SN74LS163A SYNCHRONOUS 4-BIT COUNTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage					0.7			V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA				-1.5			V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -400 µA	2.5	3.4		2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 4 mA		0.25	0.4	0.25 0.4		V
			I _{OL} = 8 mA				0.35 0.5		
I _I	Input current at maximum input voltage	Data or enable P	V _{CC} = MAX, V _I = 7 V				0.1		mA
		Load, clock, or enable T					0.2		
		Clear ('LS160A, 'LS161A)					0.1		
		Clear ('LS162A, 'LS163A)					0.2		
I _{IH}	High-level input current	Data or enable P	V _{CC} = MAX, V _I = 2.7 V				20		µA
		Load, clock, or enable T					40		
		Clear ('LS160A, 'LS161A)					20		
		Clear ('LS162A, 'LS163A)					40		
I _{IL}	Low-level input current	Data or enable P	V _{CC} = MAX, V _I = 0.4 V				-0.4		mA
		Load, clock, or enable T					-0.8		
		Clear ('LS160A, 'LS161A)					-0.4		
		Clear ('LS162A, 'LS163A)					-0.8		
I _{OS}	Short-circuit output current‡	V _{CC} = MAX	-20		-100	-20	-100	mA	
I _{CC}	Supply current, all outputs high	V _{CC} = MAX, See Note 3	18		31	18 31		mA	
I _{CCL}	Supply current, all outputs low	V _{CC} = MAX, See Note 4	19		32	19 32		mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES: 3. I_{CC}H is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			C _L = 15 pF, R _L = 2 kΩ, See Figures 1 and 2 and Notes 8 and 9	25	32		MHz
‡PLH	Clock	Ripple			20	35	ns
‡PHL		carry			18	35	
‡PLH	Clock (load input high)	Any			13	24	ns
‡PHL		Q			18	27	
‡PLH	Clock (load input low)	Any			13	24	ns
‡PHL		Q			18	27	
‡PLH	Enable T	Ripple			9	14	ns
‡PHL		carry			9	14	
‡PHL	Clear	Any Q			20	28	ns

¶ f_{max} = Maximum clock frequency

‡PLH = propagation delay time, low-to-high-level output.

‡PHL = propagation delay time, high-to-low-level output.

NOTES: 8. Load circuit is shown on page 3-11.

9. Propagation delay for clearing is measured from the clear input for the 'LS160A and 'LS161A or from the clock transition for the 'LS162A and 'LS163A.

TYPES SN54S162, SN54S163, SN74S162, SN74S163

SYNCHRONOUS 4-BIT COUNTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S162 SN54S163		SN74S162 SN74S163		UNIT
		MIN	TYP‡	MAX	MIN	
V _{IH} High-level input voltage		2			2	V
V _{IL} Low-level input voltage				0.8		0.8
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.2		-1.2
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA			0.5		0.5
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1		1
I _{IH} High-level input current	Enable T			100		100
	Other inputs			50		50
I _{IL} Low-level input current	Enable T			-4		-4
	Other inputs			-2		-2
I _{OS} Short-circuit output current §	V _{CC} = MAX	-40	-100	-40	-100	mA
I _{CC} Supply current	V _{CC} = MAX		95	160	95	160

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			C _L = 15 pF, R _L = 280 Ω, See Figures 1, 3, and 4 and Note 5	40	70		MHz
t _{PLH}	Clock	Ripple carry			14	25	ns
t _{PHL}					17	25	ns
t _{PLH}	Clock	Any Q			8	15	ns
t _{PHL}					10	15	ns
t _{PLH}	Enable T	Ripple carry			10	15	ns
t _{PHL}					10	15	ns

¶ f_{max} ≡ maximum clock frequency

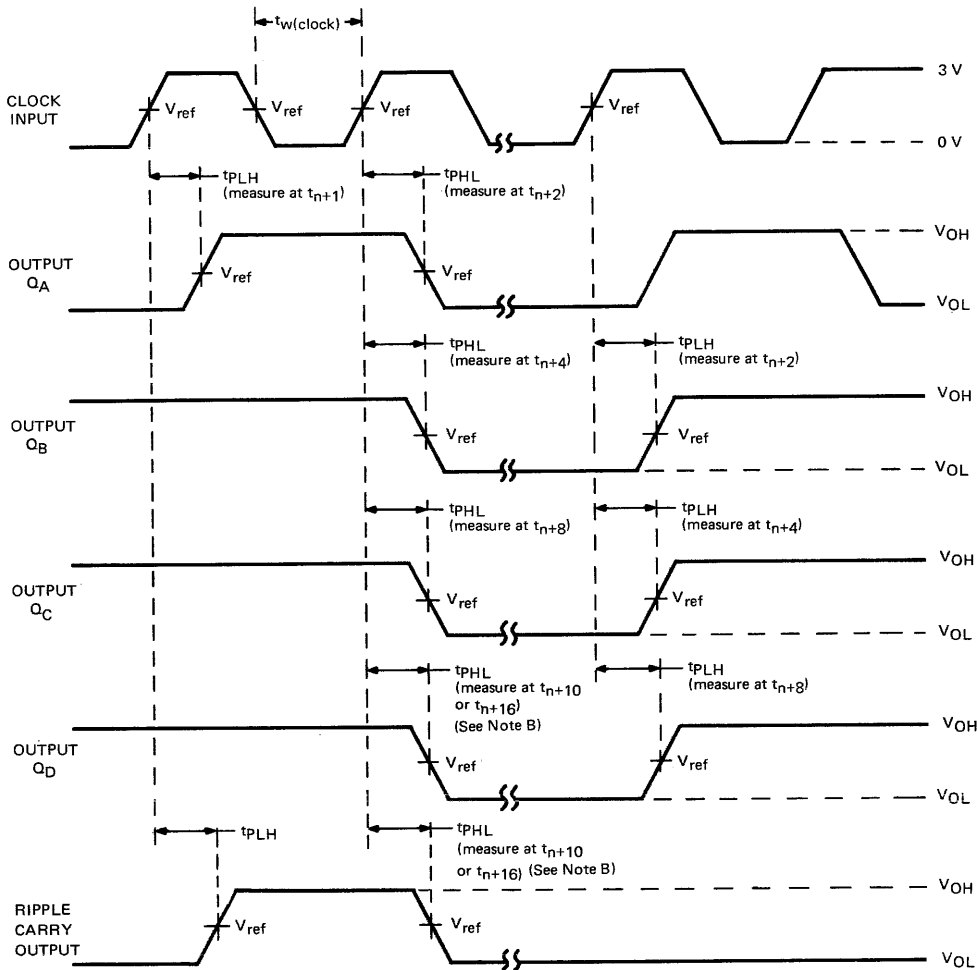
t_{PLH} ≡ propagation delay time, low-to-high-level output

t_{PHL} ≡ propagation delay time, high-to-low-level output

NOTE 5: Load circuit is shown on page 3-10.

**TYPES SN54160 THRU SN54163, SN54LS160A, THRU SN54LS163A,
SN54S162, SN54S163, SN74160 THRU SN74163,
SN74LS160A THRU SN74LS163A, SN74S162, SN74S163
SYNCHRONOUS 4-BIT COUNTERS**

PARAMETER MEASUREMENT INFORMATION



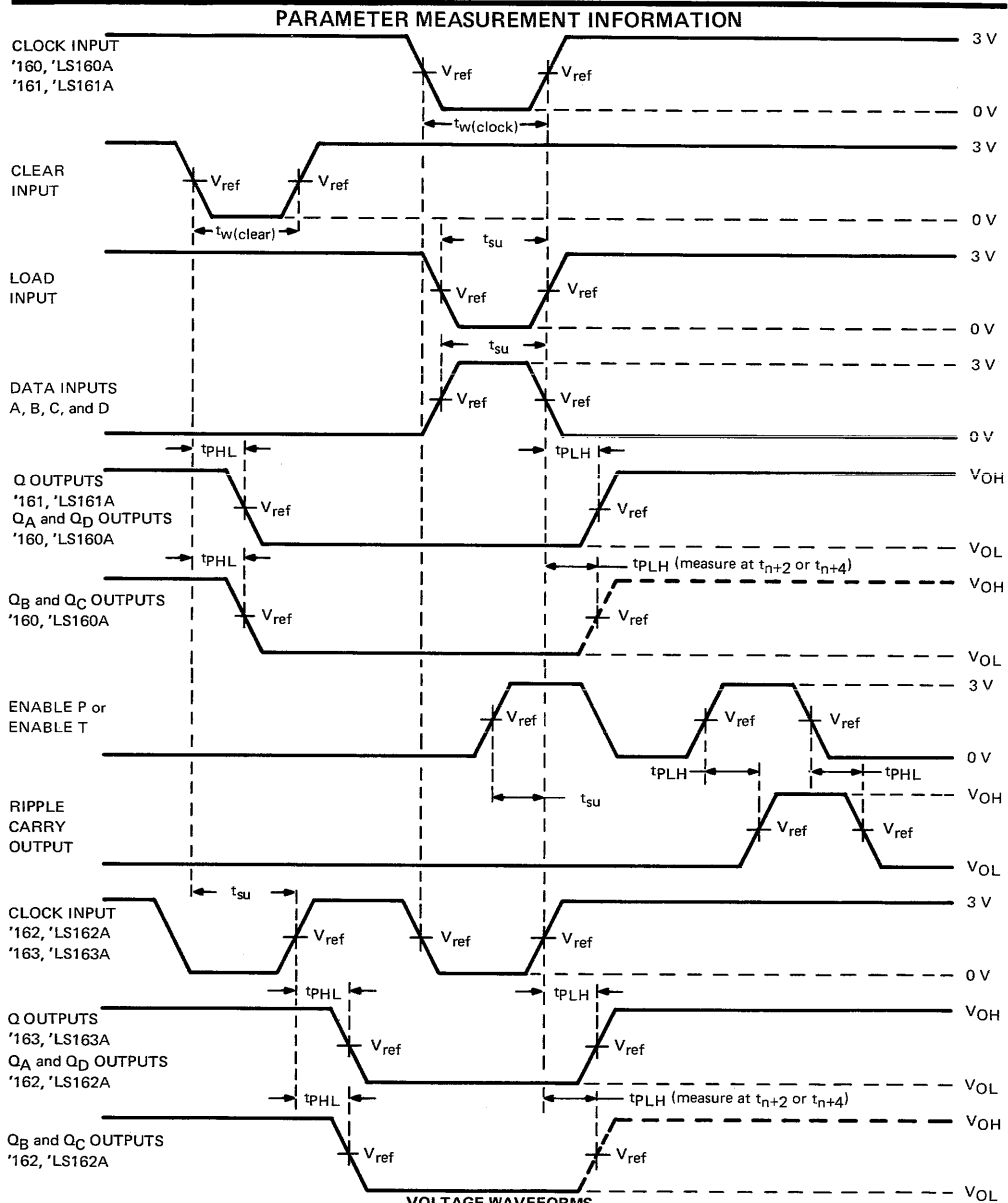
VOLTAGE WAVEFORMS

- NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $Z_{out} \approx 50 \Omega$; for '160 thru '163, $t_r \leq 10$ ns, $t_f \leq 10$ ns; for 'LS160A thru 'LS163A, $t_r \leq 15$ ns, $t_f \leq 6$ ns; and for 'S162, 'S163, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure f_{max} .
- B. Outputs Q_D and carry are tested at t_{n+10} for '160, '162, 'LS160A, 'LS162A, and 'S162, and at t_{n+16} for '161, '163, 'LS161A, 'LS163A, and 'S163, where t_n is the bit time when all outputs are low.
- C. For '160 thru '163, 'S162, and 'S163, $V_{ref} = 1.5$ V; for 'LS160A thru 'LS163A, $V_{ref} = 1.3$ V.

FIGURE 1—SWITCHING TIMES

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TYPES SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A SYNCHRONOUS 4-BIT COUNTERS



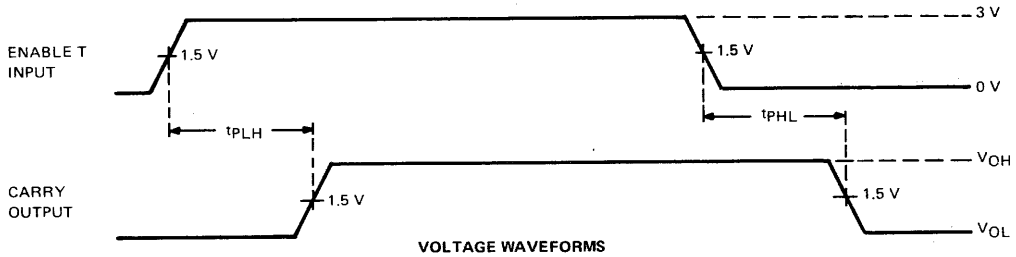
NOTES: A. The input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $Z_{out} \approx 50 \Omega$; for '160 thru '163, $t_r \leq 10$ ns, $t_f \leq 10$ ns; and for 'LS160A thru 'LS163A, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
 B. Enable P and enable T setup times are measured at t_{n+0} .
 C. For '160 thru '163, $V_{ref} = 1.5$ V; for 'LS160A thru 'LS163A, $V_{ref} = 1.3$ V.

FIGURE 2—SWITCHING TIMES

TYPES SN54S162, SN54S163, SN74S162, SN74S163

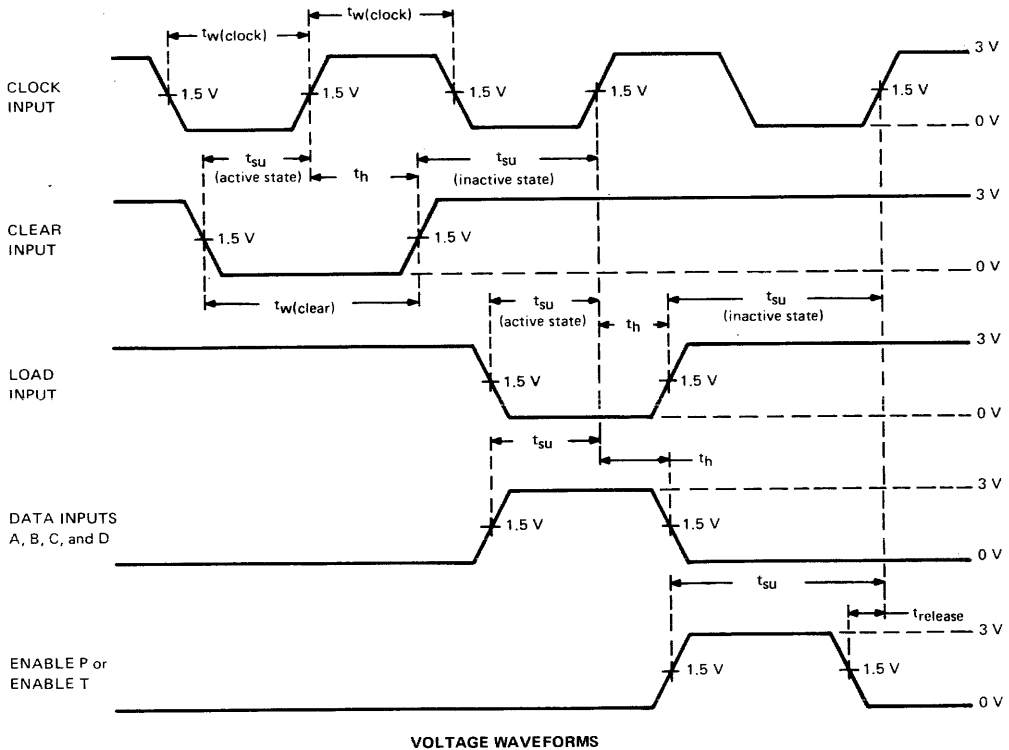
SYNCHRONOUS 4-BIT COUNTERS

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50 \Omega$.
 B. t_{PLH} and t_{PHL} from enable T input to carry output assume that the counter is at the maximum count (Q_A and Q_D high for 'S162, all Q outputs high for 'S163).

FIGURE 3—PROPAGATION DELAY TIMES FROM ENABLE T INPUT TO CARRY OUTPUT



- NOTE A: The input pulses are supplied by generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50 \Omega$.

FIGURE 4—PULSE WIDTHS, SETUP TIMES, HOLD TIMES, AND RELEASE TIME

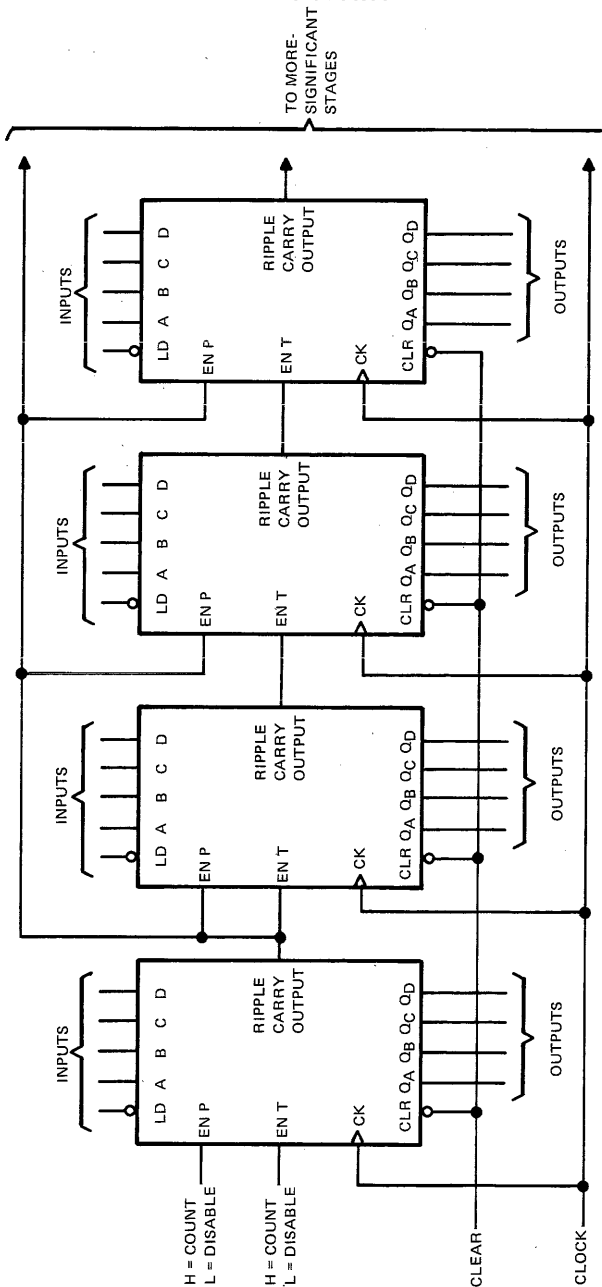
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**TYPES SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A,
SN54S162, SN54S163, SN74160 THRU SN74163,
SN74LS160A THRU SN74LS163A, N74S162, SN74S163
SYNCHRONOUS 4-BIT COUNTERS**

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The '160, '162, 'LS160A, 'LS162A, or 'S162 will count in BCD and the '161, '163, 'LS161A, 'LS163A or 'S163 will count in binary. Virtually any count mode (modulo-N, N₁-to-N₂, N₁-to-maximum) can be used with this fast look-ahead circuit.



H = COUNT
L = DISABLE

H = COUNT
L = DISABLE

CLEAR

CLOCK