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Introduction

Analog Applications Journal is a collection of analog application notes designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following product categories:

- Data Acquisition
- Power Management
- Data Transmission
- Amplifiers

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Because this book is limited in size, readers should refer to more detailed technical information, which can be found on TI's product-specific websites listed at the bottom of each application note.

Precision voltage references

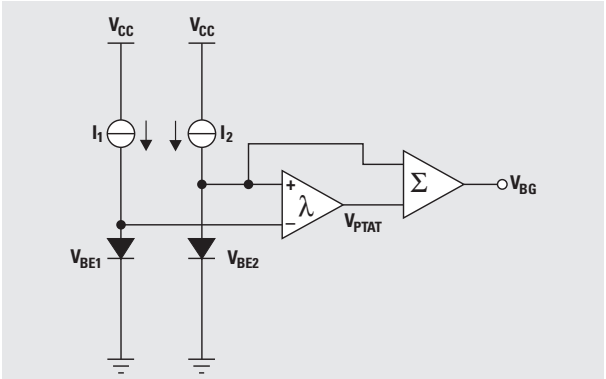
By Perry Miller, *Application Specialist—Data Converters, Texas Instruments, Dallas,*
and Doug Moore, *Managing Director, Thaler Corp., Tucson, Arizona*

Introduction

One reason why designing a data conversion system is such a challenge is the fact that the system accuracy very much depends on the accuracy of the voltage established by the internal or external DC voltage reference. The voltage reference is used to produce a precise value of output voltage for setting the full-scale input of the data conversion system. In an analog-to-digital converter (ADC), the DC voltage reference together with the analog input signal is used to generate the digitized output signal. And in a digital-to-analog converter (DAC), the DAC selects and produces an analog output from the DC reference voltage according to the digital input signal presented at the input of the DAC. Any errors in the reference voltage over the operating temperature range will adversely affect the linearity and spurious free dynamic range (SFDR) of the ADC/DAC. Practically all voltage references vary with time or environmental factors such as humidity, pressure, and temperature. As a result most CMOS ADCs/DACs have internal references suitable only for applications demanding ≤12-bit resolution even though the converter may be capable of higher resolution. Modern CMOS converters operate from 3.3-V or 5-V supplies, which limits the on-chip voltage reference to a band-gap reference. By way of the external reference pins provided on the chip, an external precision reference can also be connected to a CMOS ADC or DAC. A precision external voltage reference has a much lower temperature coefficient, thermal hysteresis, and long-term drift than an on-chip band-gap voltage reference; therefore, in applications demanding high accuracy (14-bit or 16-bit ADCs/DACs), an external precision voltage reference is often required.

Precision voltage references are available with varying degrees of precision and initial accuracy over some operating temperature range. But often what is not obvious when reading a manufacturer's data sheet is how the initial accuracy of the device is affected by other key device parameters such as line regulation, load regulation, initial voltage error, output voltage temperature coefficient (TC), output voltage noise, turn-on settling time, thermal hysteresis, quiescent supply current, and long-term stability.

Figure 1. Band-gap reference circuit



The design origins

Modern voltage references are constructed using the energy-band-gap voltage of integrated transistors, buried zener diodes, and junction field-effect transistors. Each technology offers inherent performance characteristics that can be enhanced with compensation networks or additional active circuitry. The basis topologies for the band-gap, buried zener, and XFET references are shown in Figures 1, 2, and 3, respectively.

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Figure 2. Buried zener reference circuit

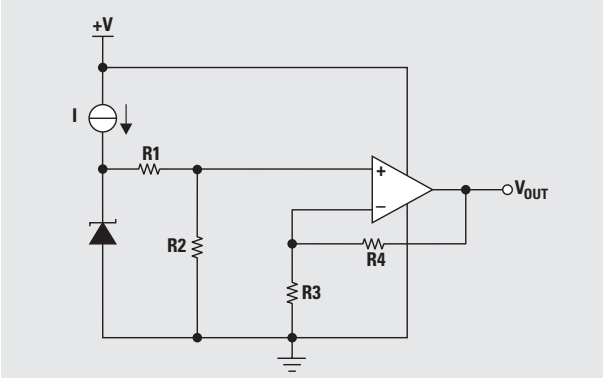
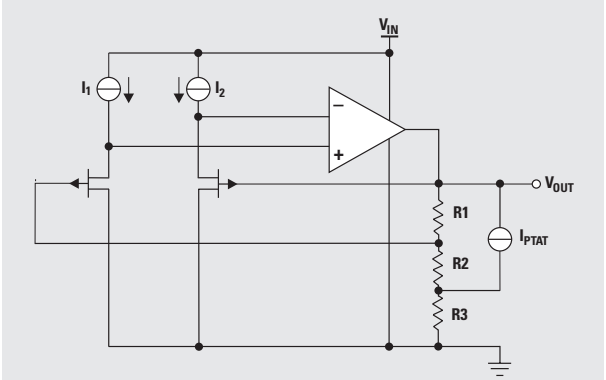


Figure 3. XFET reference circuit



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Band-gap reference

At its simplest, a band-gap reference is simply two transistors with different emitter areas used for generating a voltage proportional to absolute temperature. V_{BE1} and V_{BE2} have opposite temperature coefficients. The voltage V_{CC} is converted to a current I_1 and I_2 that are mirrored to the output branch. The output equation is

$$V_O = V_{BE1} + \lambda(V_{BE1} - V_{BE2}), \quad (1)$$

where λ is the scale factor, V_{BE1} is the base-emitter voltage of the larger of the two transistors, and V_{BE2} is the base-emitter voltage of the second transistor.

The band-gap references are widely used in ADC/DAC converters as well as for external reference source because they are fairly inexpensive. Generally, they are used in system designs where a maximum accuracy of 10 bits is required. Band-gap references typically have an initial error of 0.5–1.0% and a TC of 25–50 ppm/°C. The output voltage noise is typically 15–30 μV_{p-p} (0.1–10 Hz) with a long-term stability of 20–30 ppm/1000 hrs.

Zener reference

The zener voltage reference and feedback amplifier shown in Figure 2 are used to provide a very stable output. A current source is used to bias a 6.3-V zener diode. The zener voltage is divided by the resistor network R1 and R2. This voltage is applied to the non-inverting input of the operational amplifier, which amplifies the voltage to the required output voltage. The amplifier gain is determined by the resistor networks R3 and R4, where G = 1 + R4/R3. A 6.3-V zener diode is used because it is the most stable zener diode over time and temperature.

The output equation is

$$V_O = \frac{R2}{R1+R2}\left(1+\frac{R4}{R3}\right). \quad (2)$$

Buried zener diode references are more expensive than band-gap references but provide a higher performance level. They typically have an initial error of 0.01–0.04%, a TC of 1–10 ppm/°C, and less than 10-μV_{p-p} (0.1- to 10-Hz) noise. The long-term stability is typically 6–15 ppm/1000 hrs. Buried zener-based references are frequently used for 12-bit, 14-bit, and higher resolution systems because the performance of the buried zener-based references can be extended by incorporating nonlinear temperature compensation networks into the design. The compensation network is trimmed at several temperatures to optimize the electrical performance over the operating temperature range.

XFET reference

The XFET reference is a new reference technique that consists of two junction field-effect transistors, one of which has an extra channel implant to raise the pinch-off voltage. The two JFETs are run at the same drain current. The difference in pinch-off voltage is amplified and used to form a voltage reference. The general equation is

$$V_O = \Delta V_P\left(\frac{R1+R2+R3}{R1}\right) + (I_{PTAT})(R3), \quad (3)$$

where ΔV_P is the difference in pinch-off voltage between the two FETs and I_{PTAT} is the positive temperature coefficient correction current.

The simplified schematic for the XFET reference is shown in Figure 3.

The XFET references are relatively new and provide a performance level between band-gap and zener references. The initial error is typically 0.06%, a TC of 10 ppm/°C, and 15-μV_{p-p} (0.1- to 10-Hz) noise. The long-term stability is 0.2 ppm/1000 hrs.

Reference selection for a 14-bit converter

Specified parameters for voltage references include line regulation, load regulation, initial voltage error, output voltage temperature coefficient (TC), output voltage noise, turn-on settling time, thermal hysterisis, quiescent supply current, and long term stability.

The most important parameters for data acquisition systems design are initial error, output voltage temperature coefficient (TC), thermal hysteresis, noise, and long-term stability of the voltage reference device.

Table 1 summarizes the major error sources for the three references that are compared in this application note. The data represents the highest grade for each

Table 1. Voltage reference major error sources (all information is based on published data sheets)

PARAMETER	THALER CORP. VRE3050 TEMPERATURE RANGE –40°C to +85°C	MAXIM MAX6250 TEMPERATURE RANGE –40°C to +85°C	ANALOG DEVICES ADR293 TEMPERATURE RANGE –40°C to +85°C
Output voltage	5.000 V	5.000 V	5.000 V
Initial error	0.01%	0.04%	0.06%
Temperature coefficient	0.6 ppm/°C	3.0 ppm/°C	8.00 ppm/°C
Noise (0.1–10 Hz)	3.0 μV_{p-p}	3.0 μV_{p-p}	15.0 μV_{p-p}
Thermal hysteresis 25°C→50°C→25°C	2 ppm	20 ppm	15 ppm
Long-term stability	6.0 ppm/1000 hrs.	20.0 ppm/1000 hrs.	0.2 ppm/1000 hrs.
Power supply	8.0 V–36 V	8.0 V–36 V	6.0 V–15 V
Turn-on settling time	10 µs	10 µs	<10 µs
Line regulation (8 V ≤ V_{IN} ≤ 10 V)	25 ppm/V	35.00 ppm/V	100.00 ppm/V
Load regulation (source 0 mA ≤ I_O ≤ 15 mA)	5 ppm/mA	7 ppm/mA	100 ppm/mA
PSRR (10 Hz–900 Hz)	95 dB	90 dB	40 dB

respective model in the 8-pin plastic DIP package over the industrial temperature range (–40°C to +85°C). The poorest-performing references are band-gap type and are not included in this summary. Buried zener diodes have better overall performance than band-gap devices and the XFET references. The buried zener reference with a third-order temperature compensation network (VRE3050) is the best performer with respect to initial error, TC, and thermal hysteresis.

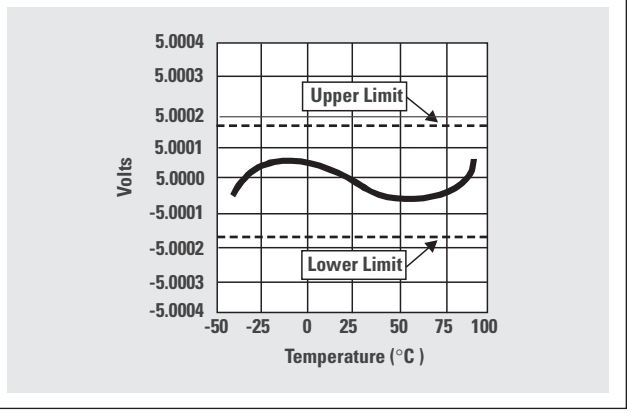
Explanation of parameters

***Initial error*—**The output voltage tolerance of a reference after the device is turned on and warmed up. It is usually measured without a load applied. In many applications, initial error is the most important specification. Often instrument manufacturers will specify a reference with a tight initial error so they do not have to perform room-temperature systems calibration after assembly.

***Temperature coefficient (TC)*—**A change in output voltage due to change in temperature usually expressed in ppm/°C. It is the second most important specification after initial accuracy. For many instrument manufacturers, a voltage reference with a temperature coefficient less than 1 ppm/°C makes it possible not to have to perform a system temperature calibration, a slow and costly process. Of the three TC specification methods (slope, butterfly, and box), the box method is most commonly used. A box is formed by the min/max limits for the nominal output voltage over the operating temperature range. The equation follows.

$$TC = \left[\frac{V_{MAX} - V_{MIN}}{V_{nominal} \times (T_{MAX} - T_{MIN})} \right] \times 10^6 \qquad (4)$$

Figure 4. V_{OUT} vs. temperature



This method corresponds more accurately to the method of test and provides a closer estimate of actual error than the other methods. The box method guarantees limits for the temperature error but does not specify the exact shape and slope of the device under test. Assuming a 5-V reference with a 0.6-ppm/°C TC over the industrial temperature range, a plot of the box calculation method would appear as in Figure 4.

A designer who needs a 14-bit accurate data acquisition system over the industrial temperature range (–40°C to +85°C) will need a voltage reference with a TC of 1.0 ppm/°C if the reference is allowed to contribute an error equivalent to 1 LSB. For 1/2 LSB equivalent error from the reference, a voltage reference with a temperature coefficient of 0.5 ppm/°C would be needed. Figure 5 shows the required reference TC vs. ΔT change from 25°C for resolution ranging from 8 bits to 20 bits.

***Thermal hysteresis*—**A change in output voltage as a result of a temperature change. When references experience a temperature change and return to the initial temperature, they do not always have the same initial output voltage. Thermal hysteresis is difficult to correct and is a major error source in systems that experience temperature changes of 25°C or more. Voltage reference manufacturers are starting to include this important specification in their datasheets.

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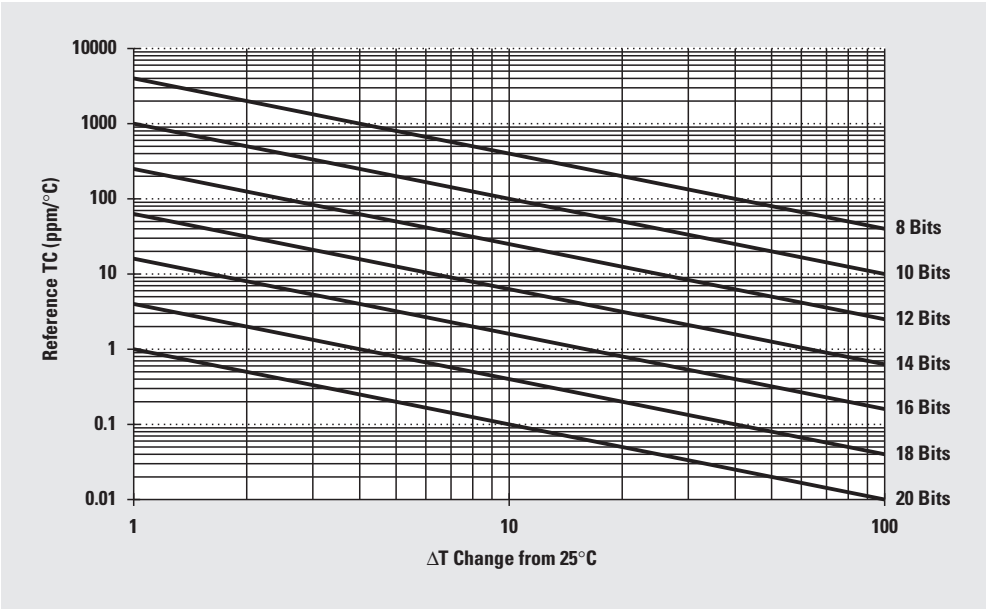
Figure 5. System performance vs. reference TC



Reference TC vs. ΔT change from 25°C for 1 LSB change

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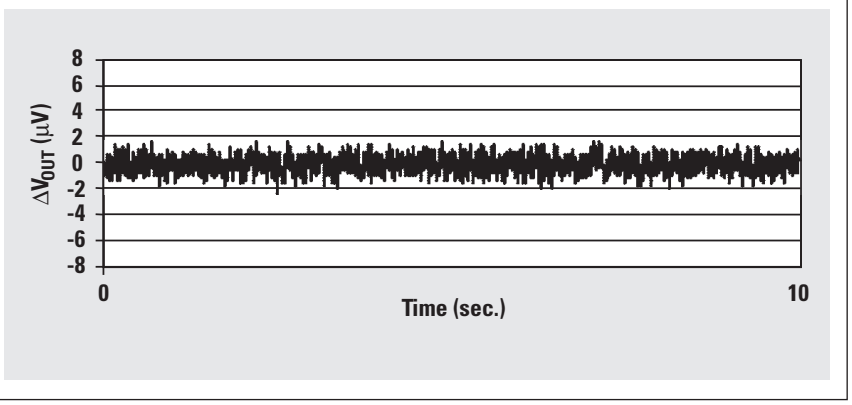
Noise (1/f and broadband)— Electrical noise on the output of a voltage reference. It can include wideband thermal noise and narrowband 1/*f* noise. Wideband noise can be effectively filtered with a simple RC network. 1/*f* noise is inherent in the reference and cannot be filtered. It is specified in the 0.1- to 10-Hz range. Low 1/*f* noise references are important in precision designs.

Figure 6. 0.1-Hz to 10-Hz noise



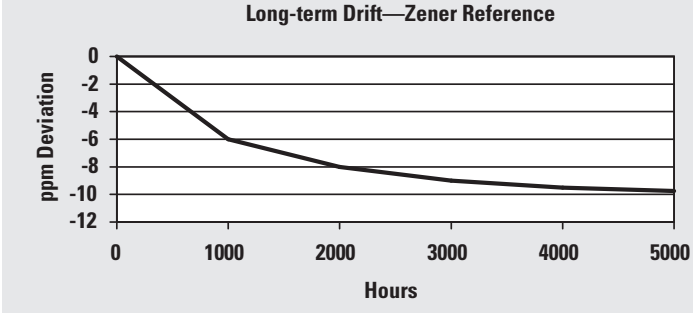
Long-term drift—A slow change in output voltage that occurs over months of operation. Long-term drift is usually expressed in ppm/1000 hrs. In zener references, the long-term drift is typically 6 ppm/1000 hrs. and decreases at an exponential rate over time. Additional temperature burn-in of the reference can accelerate the stability of a zener reference. The XFET reference has excellent long-term stability—0.2 ppm/1000 hrs.

Turn-on settling time—A change in voltage over a specified time interval after the power is applied. Most references settle to 0.1% in less than 10 µs. Turn-on settling time is important for portable battery systems that conserve energy by powering the circuitry only for short periods of time.

Line regulation—An error produced by a change in the input voltage. This dc specification does not include the effects of ripple voltage or line transients.

Load regulation—An error produced by a change in load current. Like line regulation, this dc specification does not include the effects of load transients.

Figure 7. VRE3050 long-term drift vs. hours



PCB layout—Poor printed circuit board layout can adversely affect the performance of the reference. Poor layout can affect the output voltage, noise, and thermal performance of the device. Inherent stress in the PCB can also be transferred to the reference and can shift the output voltage.

Conclusion

It has been shown that a number of key parameters must be evaluated before selecting an external reference for a high-resolution data acquisition system. The XFET reference is suitable for systems that will be held at a constant temperature and where good long-term stability of the reference is important. In 14-bit conversion systems that are designed for the industrial operating temperature range, the VRE3050 is the preferred device because of its better initial error, TC, and thermal hysteresis performance.

References

1. Analog Devices Inc., Low Noise, Micropower, Precision Reference ADR293 Datasheet.
2. Paul R. Gray and Robert G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 3rd ed. (John Wiley & Sons, Inc., 1992).
3. Maxim Corp., MAX6250, Low Noise Precision, +2.5 V +4.096 V +5 V Voltage Reference Datasheet.
4. Texas Instruments, THS1265, 12-bit, 65 MSPS, IF Sampling Communications A/D converter.
5. Texas Instruments, THS1470, 14-bit, 70 MSPS, IF Sampling Communications A/D converter.
6. Thaler Corp., Precision Reference VRE3050 Datasheet.

Techniques for sampling high-speed graphics with lower-speed A/D converters

By Bart De Canne

System Specialist, High-Speed Data Converters

One area where the need for high-speed A/D converters becomes apparent is in PC graphics digitizing. While conventional TV images have relatively low bandwidth and can be sampled at 13.5 MHz for component YUV signals or at a multiple (4×) of the subcarrier frequency for PAL or NTSC composite video, PC graphics digitizing requires much higher rates. Traditional CRT monitors accept an analog signal, but LCD monitors provide a pixellated display and need to be driven by a digital signal of the same resolution as the flat panel display in order to generate a full-size screen image. While the straightforward solution is to use an A/D converter specified at the same or a higher clock rate than the maximum pixel rate, two approaches using lower-speed converters are presented in this application note.

Table 1. Popular PC graphics formats

	REFRESH RATE (Hz)	PIXEL RATE (MHz)
SVGA (800 x 600)	72	50.000
	75	49.500
	85	56.250
XGA (1024 x 768)	70	75.000
	75	78.750
	85	94.500
SXGA (1280 x 1024)	60	108.000
	75	135.000
	85	157.500

Sample rates

Table 1 lists some display formats and rates as specified by VESA. For example, while the XGA standard goes up to 94.5 MHz, most of the panels can handle a screen refresh rate of up to only 75 Hz and are therefore limited to a 78.5-MHz pixel rate at XGA resolution. In this case there is little sense in configuring the PC graphics adaptor to produce 85-Hz output, as the rate will have to be brought down by frame-rate conversion circuitry on the LCD monitor's analog input interface. The system designer shouldn't spend extra money on the analog front end to enable 85-Hz input, as it will not be a recommended operating mode.

Suppose an 80-MHz converter is to be used to process a 95-MHz input signal. The cost/performance tradeoff might actually be better than if a more expensive 95-MHz ADC is used. To help understand how a system can be designed to accept such a high-speed input, the architecture of a typical LCD monitor's analog front end should be examined.

Analog front-end architecture

In concept, the analog front end includes a PGA (programmable gain amplifier), an A/D converter for each of the three color components (R,G, and B), a PLL to derive the pixel clock from the line rate, and a functional unit called a "display timing generator" to generate the LCD panel's timing control signals, as shown in Figure 1. This would be all that's required if there weren't a need for image

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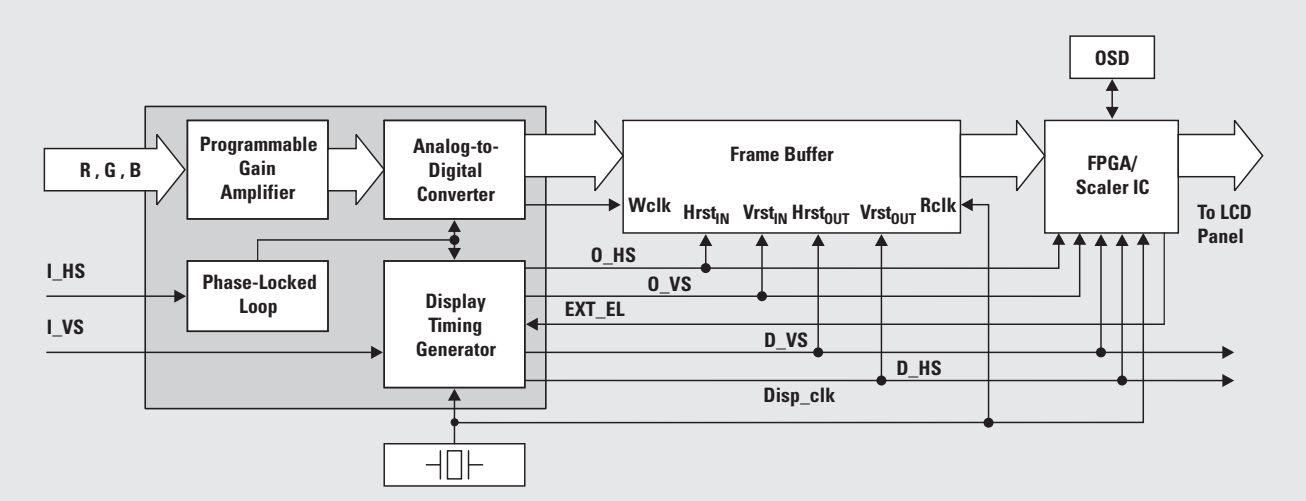
Figure 1. A typical LCD monitor's front end



A typical LCD monitor's front end includes PGA, ADC, PLL, and DTG. If ADCs with lower sampling rates can be used, the system cost is lower.

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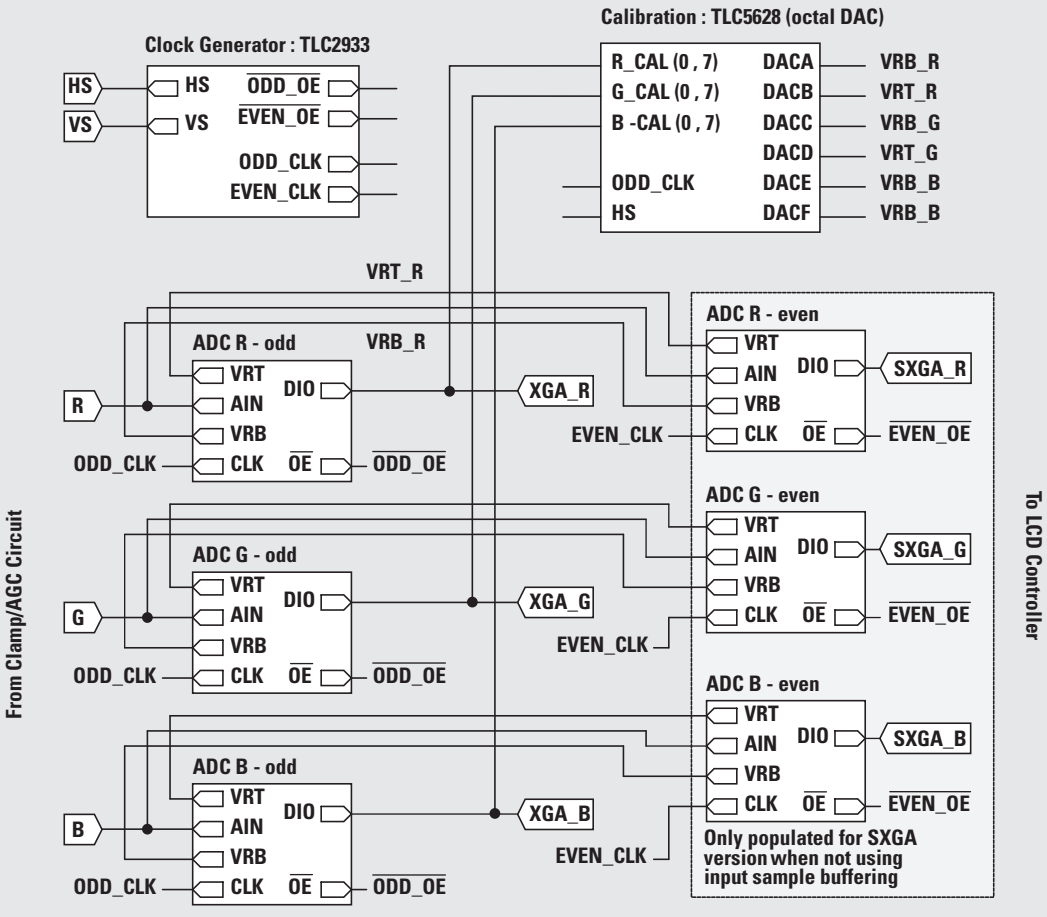
scaling. To ensure full-screen display of lower-resolution images (e.g., VGA on an XGA panel), the image needs to be enlarged (zoomed). An image processor ASIC is normally used to perform the required real-time image scaling. The two-dimensional scaling needs at least a line memory and complete external frame buffer for storing its data. A complete frame buffer is also needed if there is frame-rate-conversion in the system (from an 85-Hz to a 75-Hz refresh rate, for example). It is this frame buffer that gives considerable flexibility for the data acquisition function. The memory decouples the pixel frequency of the analog front end (the data converter) from the display pixel frequency.

The system could be designed to capture data at a lower speed than the pixel frequency by digitizing selective pixels when the pixel frequency is higher than the maximum speed of the A/D converter. A simple algorithm for this would be the digitization (at half the input pixel rate) of only the odd pixels on every line in odd frames and even pixels in even frames. In the example of a 94.5-MHz XGA, the converter need only operate at 48 MHz—in this case. A complete frame is captured for every two input frames. The frame buffer will hold the previous frame for further processing until the next one is completely acquired. Because of the lower sampling clock that needs to be generated in the system, there is an advantage on other functional blocks; e.g., the PLL's VCO operating range can be decreased since it needs to operate at up to only 80 MHz, not the original 94.5 MHz.

Advantages and disadvantages

Does all this come without disadvantages? Unfortunately not. Acquiring a full-screen image for only every two input frames essentially halves the horizontal frequency resolution over time. This will result in artifacts in objects that move horizontally in the image; however, given the fact that most LCD monitors will replace traditional analog PC monitors for the display of mostly static images, this performance penalty might be overcome by the price advantage. In the previous example, the 80-MHz converter

Figure 2. LCD monitor front end using reduced sample rates



This LCD monitor front end employs techniques to reduce the sampling rate for XGA performance at a 75-Hz refresh rate. The additional ADCs are needed only if full-speed SXGA performance is desired.

could be used to digitize input images at up to SXGA resolution at an 85-Hz (157.5-MHz) refresh rate, which makes sense only when the LCD panel can handle this resolution or when the resolution is reduced in some other way. This principle holds true only when a frame buffer is available for this function. Depending on the operation mode, a single memory could function for the storage of temporary results from the image scaler (at pixel rates lower or equal to the A/D converter's maximum speed) or act as an input buffer to extend the pixel input range of the LCD monitor, giving up its use of the scaling engine (which remains unused in this case). Higher pixel rates will normally occur for the panel's maximum resolution, so no zooming is needed anyway. If there is no frame memory present, it still might make sense to use lower-speed A/Ds.

Parallel ADCs

Two converters can be used in parallel to acquire the input image at full speed, with each converter operating at only half the input pixel rate. If the converter has an output enable function, like TI's TLV5580 8-bit 80-Msps ADC, the output bus could be used even for combining the A/D outputs, ruling out the need for an external multiplexer. Part and PCB uniformity across multiple LCD product lines might prove this concept to be commercially viable. For instance, a single LCD monitor interface board could handle both a version at up to XGA@75 Hz and a high-end version at higher refresh rates and/or resolutions. In both cases the same lower-priced ADC part can be used. Even using two in parallel for the high-end version might prove more cost-effective than using an expensive high-speed ADC.

To enable a correct matching of ADCs operated in parallel, their digitizing ranges (as set by their bottom/top reference voltages) should be identical. To ensure this, corresponding external reference pins on both parts can be tied together. Converters that provide the flexibility to enter both top and bottom reference voltages independently, like TLV5580, are preferred over parts that accept only a single (mid-range) level and derive both references internally. Small tolerance offsets between parts could (in the latter case) hamper their uniform operation, and the same analog input level could be digitized to different output codes in both converters. Note that for a 1-V_{pp} signal, 1 LSB on an 8-bit ADC corresponds to only 4 mV, so board noise in general is an issue. Careful PCB layout using separate analog and digital ground planes connected at a single point (underneath the A/D) is recommended. Converters that clearly separate analog and digital pins on their footprint simplify layout of the ground planes.

Autocalibration

To take accuracy even further, high-end monitors could include an autocalibration feature much like in high-end CRT monitors today where a calibration for color-temperature is provided. In the case of an LCD, a known stable input level is switched into the ADC during the non-active video portion of the image (the horizontal and/or vertical blanking interval). During that time the ADC output codes are monitored by the microcontroller and compared to their expected values. A control loop can adjust the analog input level or the ADC reference levels that may be generated from external DACs. Note that there is already control function on gain and offset of the analog input level for contrast and brightness level control of the display. Both are user controls accessible from the LCD monitor's front side.

Design example

The design example in Figure 2 shows some of the concepts described in this application. Three TLV5580s are used for the XGA@75-Hz board version, and three extra parts are included for the high-end SXGA that samples at full speed. Corresponding references of both odd/even sampling A/Ds are tied together to avoid in-channel offset. The autocalibration feature is implemented using an octal DAC with microprocessor interface. During horizontal sync (HS) the A/D values are read and compared to the expected blanking codes. These differences will adjust the DAC top/bottom DAC outputs. No use is made of the internal bandgap-derived references on the A/D, so they are powered down via their separate power-down pin (PWDN_REF high). Note also that in this design the maximum clock speed on the board is limited to half of the pixel clock. Even the panel interface is of "double pixel width," consisting of two buses for each color component. This reduces EMI considerably and eases PLL design. The same PLL circuit can be used both for XGA and SXGA versions. In the latter case the divider in the PLL feedback loop is programmed to half the number of pixels/line to produce half the pixel clock frequency. Even and odd clock signals run at the same frequency but in opposite phase.

Summary

Although analog LCD interface module design issues have been touched on only briefly, it is clear that there are considerable design trade-offs to be made and much room is left for product differentiation. It is the intent of this application note to present some options focusing on the data converter part and its impact on the complete system design.

TI TPS5602 for powering TI's DSP

By Bang S. Lee
Application Specialist, Power Management

The TI TPS5602 (a dual-channel synchronous buck switch-mode power-supply controller) features very fast feedback control and dual channels, and is designed specifically for DSP applications that require fast transient response and high efficiency. By using the hysteretic control method, it is ideal for high-transient current applications such as the 'C6000 and multiple 'C54x DSPs. The up and down power sequencing can be achieved by setting the standby pins, since both channels are independent. The wide input voltage and adjustable output voltage make the TPS5602 suitable for many applications.

TPS5602 operating conditions

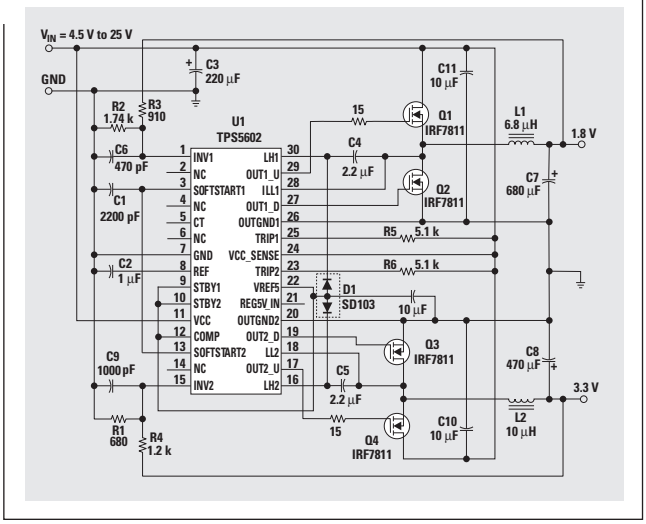
- V_{IN} range — 4.5 V to 25 V
- V_{OUT} range — 1.2 V to given input voltage
- I_{OUT} range — 14 A per output (the current capability can be extended in multi-phase configuration or if the switching devices are added in parallel)

Key features

- Independent dual channels
- Hysteretic control for fast transient response
- Adjustable output voltage down to 1.2 V
- Minimized external component count
- Synchronous rectifier enables efficiencies of >95%
- Separate standby control and over-current protection
- Low supply current (0.8 mA typ)
- 30-pin TSSOP
- Low standby current (1 µA maximum)
- EVM available (TPS5602EVM-121)
- Driver current 1.2 A at V_o = 3 V

Figure 1 shows a typical circuit design using the TPS5602 which features a dual-channel synchronous buck converter (1.8-V and 3.3-V outputs). The two output voltages are independent and can be adjustable (1.2 V to approximately input voltage) by using the sampling resistors R1, R2, R3, and R4. The output voltages, V_{OUT1} and V_{OUT2}, are set with the following equations, where the reference voltage is 1.185 volts.

Figure 1. Typical circuit design using the TPS5602



$$V_{OUT1} = \left(1 + \frac{R3}{R2}\right) V_{REF} \quad (1)$$

$$V_{OUT2} = \left(1 + \frac{R4}{R1}\right) V_{REF} \quad (2)$$

Figure 2 shows the TPS5602's transient response. The response is less than 2 microseconds after a load is applied. Conventional PWM buck converters exhibit approximately 100 microseconds of response.

Figures 3 and 4 show the efficiency of the two controllers over load up to 5 A. Efficiency can be improved by choosing lower on-resistance MOSFET.

Table 1 shows the setting values of TPS5602 to generate the output voltages 1.8 V, 2.5 V, or 3.3 V.

Figure 2. Fast load transient response

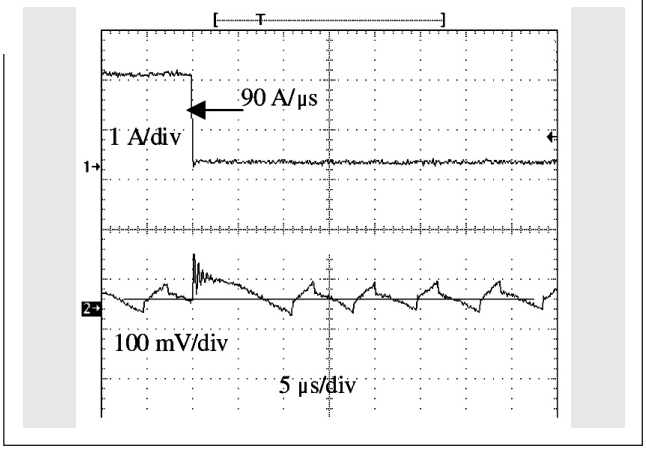


Table 1. Summary of setting values for TPS5602 1.8/2.5/3.3-V outputs

OUTPUT VOLTAGE (V)	R2 (or R1) (Ω)	R3 (or R4) (Ω)
3.3	680	1.2K
2.5	1K	1.1K
1.8	1.74K	910

The power solutions for TMS320C6xxx and TMS320VC54xx using TPS5602 are shown in Figures 5 and 6.

To avoid bus contention issues within a DSP system, start-up sequencing is recommended. The TMS320C6xxx specifications state that the core and I/O supplies should come up simultaneously, or the core first, followed by the I/O supply. The TMS320VC54xx specifications recommend that the I/O voltage should come up first, or simultaneously. There is a simple solution to meet the power sequencing recommendation. By using the SOFTSTART1 and SOFTSTART2 pins in Figure 1, the start-up sequencing (core voltage first, then peripheral voltage or vice versa) can be easily achieved. The softstart timing can be adjusted by selecting the softstart capacitor value, such as C1 and C12 shown in Figure 1. The equation is

$$C_{soft}(\mu F) = 2 \times T_{soft}(ms), \quad \textbf{(3)}$$

where C_{soft} is the softstart capacitance and T_{soft} is the start-up time. For example, to set the start-up time T_{soft} = 5 ms, the capacitance value of C_{soft} = 0.01 µF is needed.

In addition, The TPS5602 has two external pins (STBY1, STBY2) that can be alternatively used for power-up sequencing.

Figure 4. Efficiency of 1.8-V output

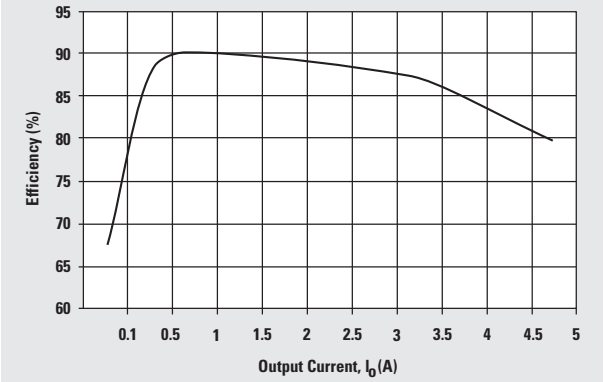


Figure 5. TMS320C6201B/'C6202/'C6211/'C6701/ 'C6711 power-supply solution using TPS5602

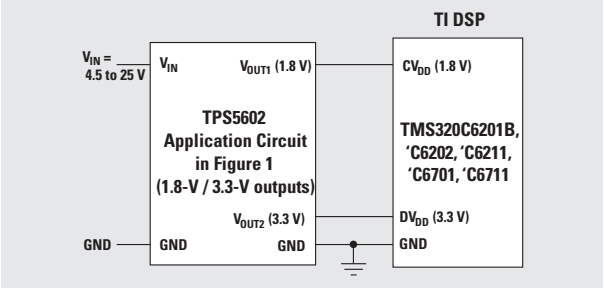
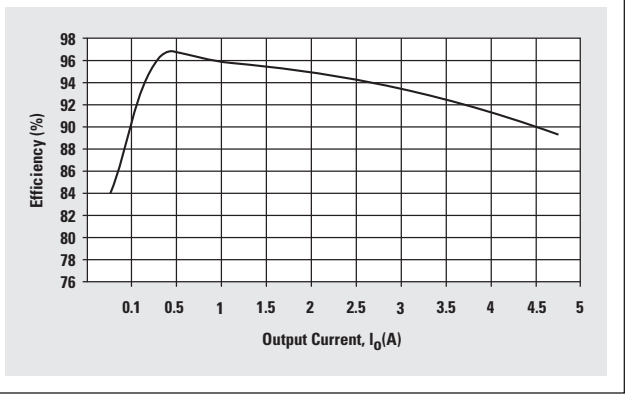


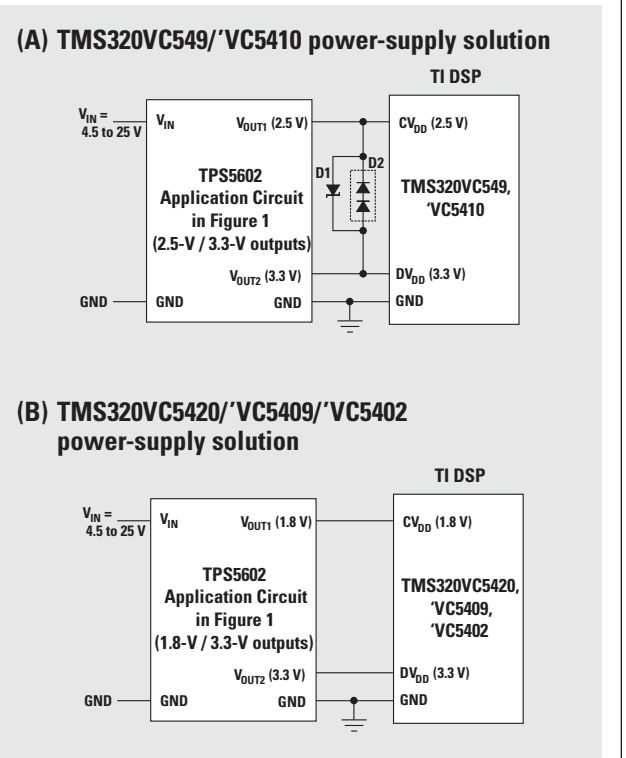
Figure 3. Efficiency of 3.3-V output



Protection diodes D1 and D2 shown in Figure 6 prevent excessive voltage differences (>2 V) between two outputs under any conditions, which is recommended by TMS320VC549/'VC5410.

The two power supplies should be placed close to the DSP to minimize the trace resistance and inductance, and to minimize the ground loop current between the two output grounds. This ground loop current can generate radiated EMI noise that can adversely affect any circuitry within the loop. The ground connection must be made directly on the DSP to help minimize the problem.

Figure 6. TMS320VC54xx power-supply solutions using TPS5602



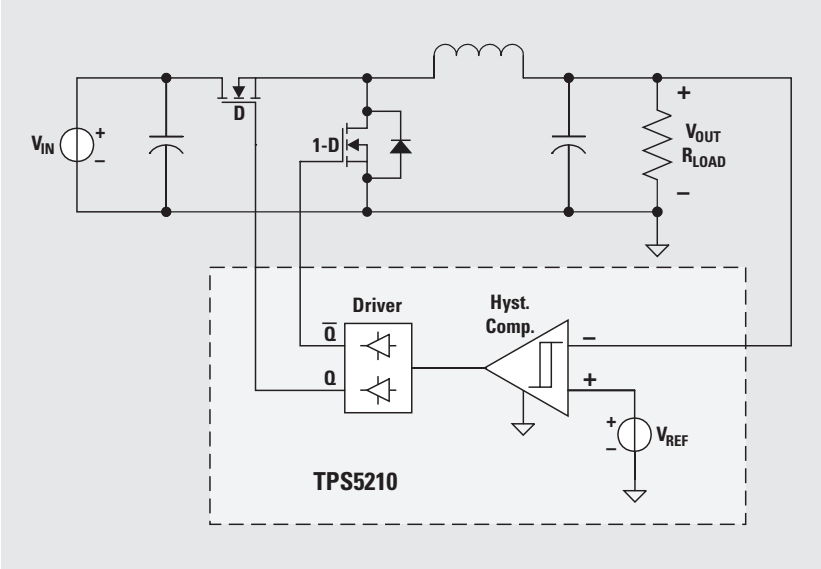
Data sheet and EVM board: **www-s.ti.com/sc/psheets/slvs217/slvs217.pdf**
Application note: **www.ti.com/sc/docs/apps/analog/power_management.html**

Synchronous buck regulator design using the TI TPS5211 high-frequency hysteretic controller

By Rais Miftakhutdinov
System Specialist, Power Management

Hysteretic mode control, which is implemented in TI's TPS5210 family of controllers, has become very popular for use in fast-transient-response power supplies for microprocessors and DSPs or other high-slew-rate transition loads, because it is a very simple solution with excellent dynamic characteristics. An example of a synchronous buck converter using a hysteretic controller is shown in Figure 1.

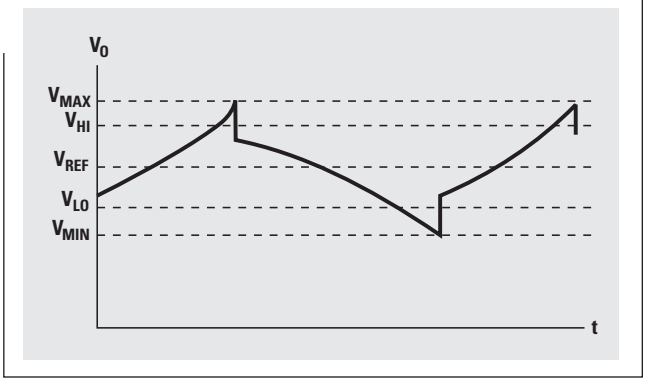
Figure 1. Hysteretic control approach with a fast feedback loop



A hysteretic controller is a self-oscillation circuit that regulates output voltage by keeping it within a hysteresis window set by a reference voltage regulator and comparator. The actual output ripple voltage is the combination of the hysteresis voltage, overshoot caused by internal delays, and the output capacitor characteristics. Figure 2 shows a hysteresis window voltage (V_{HI} to V_{LO}) and the output voltage ripple (V_{MAX} to V_{MIN}).

Unlike other control approaches, this device does not have a slow feedback loop and reacts on the load current transient in the same switching cycle that the transient occurs. The transient response time depends only on delays in the hysteretic comparator and drive circuitry. The high-frequency noise filter in the input of the comparator also adds some delay. These delays depend on the level of selected technology and therefore, the hysteretic control has the fastest transient response compared to other control approaches. The other advantage of the hysteretic controller is that its duty cycle covers the entire range from zero to one. It does not have any restrictions on the power switch conduction interval that most of the other control approaches have. Because of that, the recovery time of the output voltage after the load current transient is shortest. Excellent dynamic characteristics of hysteretic control result in smaller size and lower cost of output filtering.

Figure 2. Output ripple of hysteretic regulator



The switching frequency for this control approach depends on the output filter characteristics, input and output voltage, hysteresis window, and internal delays. The simplified equation for the switching frequency is

$$f_S \cong \frac{[V_{OUT} \times (V_{IN} - V_{OUT}) \times ESR]}{(V_{IN} \times L \times \text{Hysteresis window})},$$

where ESR is equivalent series resistance of the output capacitor and L is the output inductor value.

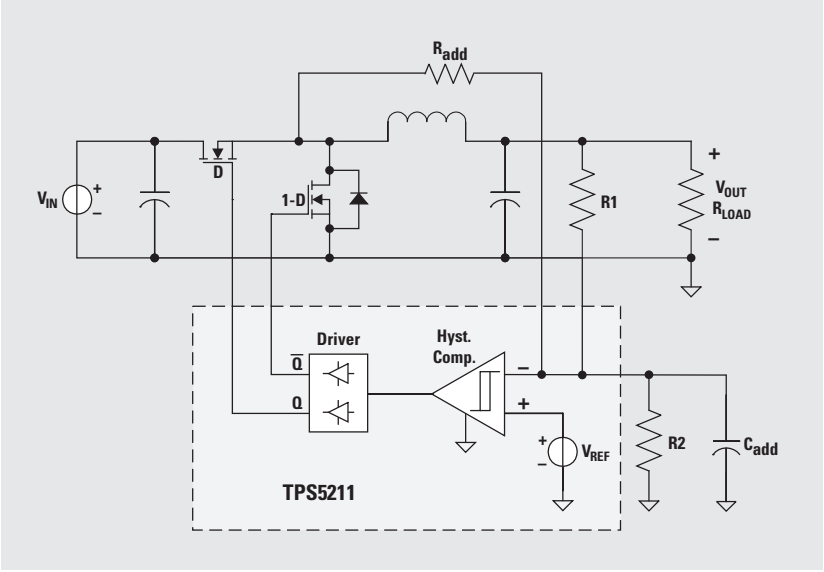
For high-frequency operation (>400 kHz) the hysteresis window might be decreased, but frequency variation becomes significant because of output capacitor parasitics, delays, and noise influence. The other problem relates to the type of output capacitor. One can see from the switching frequency equation that it is proportional to ESR. This means that using an "ideal" capacitor with very low ESR (like connecting many ceramic capacitors in parallel) is a

problem because the operating frequency becomes relatively low. The TI TPS5211 hysteretic controller overcomes these problems.

TPS5211 description

A functional block diagram of the TPS5211 controller is the same as for the TPS5210. The differences relate to parameters and characteristics specified for higher-frequency operation (up to 700 kHz). Also, there are a few external components that have to be added to a dc-to-dc converter. A simplified diagram of an asynchronous buck converter using the TPS5211 hysteretic controller is shown in Figure 3.

Figure 3. Synchronous buck converter with TPS5211 hysteretic controller



The additional R_{add} - C_{add} circuitry is added to the dc-to-dc regulator. R_{add} is connected between the input of the hysteresis comparator and the midpoint of the power switches. C_{add} is connected between the input of the comparator and the ground. This R_{add} - C_{add} circuitry forms an additional ramp signal through the input of the hysteretic comparator. The two signals are summed through the inputs of the comparator—the ramp signal from R_{add} - C_{add} circuitry and the signal from the output of converter. By proper selection of R_{add} and C_{add} one can get the amplitude of the additional ramp signal which is greater than the output ripple of the converter. As the result, the switching frequency is higher while the output ripple becomes lower. The switching frequency depends on R_{add} - C_{add} values and does not depend on the output filter characteristics including the ESR, ESL, and C of the output capacitor. The simplified equation for the switching frequency of the TPS5211 controller is

$$f_S = 1/T_S,$$

$$T_S \cong \frac{V_{IN} \times R_{add} \times C_{add} \times \text{Hysteresis window}}{V_{REF} \times (V_{IN} - V_{REF})} + T_{DELAY} \times \left(2 + \frac{V_{REF}}{V_{IN} - V_{REF}} + \frac{V_{IN} - V_{REF}}{V_{REF}}\right),$$

where T_{DELAY} characterizes comparator and drive circuitry delays.

At the same time, the dc feedback signal from the output of the converter controls the dc level of the output voltage, which is defined by

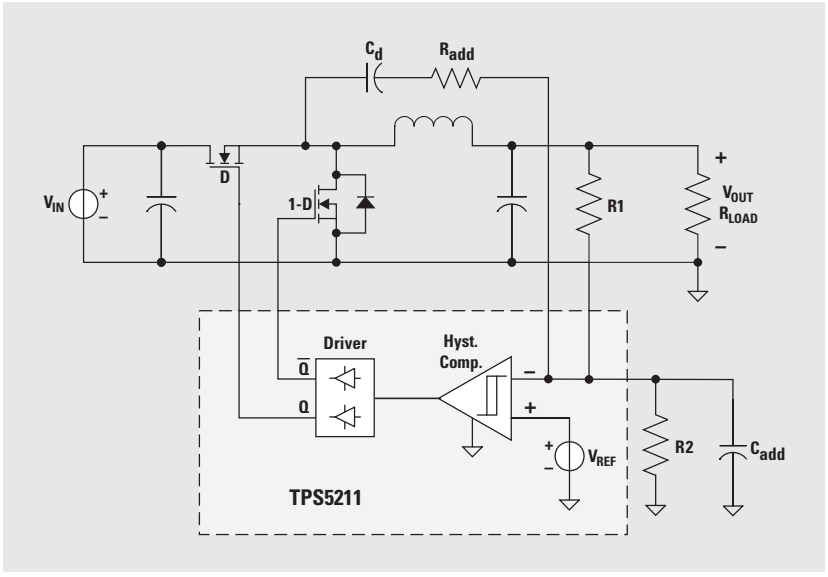
$$V_{OUT} = V_{REF} \times \left[1 + \frac{R1 \times R_{add}}{R2 \times (R1 + R_{add})}\right].$$

One can see that the output voltage V_{OUT} depends on the additional resistor R_{add}. To avoid this dependence, the dc decoupling capacitor C_d can be added in series with R_{add} as shown in Figure 4. The value of this capacitor has to be much higher than C_{add}.

With the decoupling capacitior C_d, the output voltage is defined by

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right).$$

Figure 4. Synchronous buck converter with dc decoupling capacitor C_d



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The switching frequency does not depend on output capacitor characteristics, so high-frequency, low-cost ceramic or film capacitors can be used in this dc-to-dc converter, maintaining the same excellent load current transient response characteristics.

The R_{add} - C_{add} circuitry adds feed-forward properties to the controller, which also improves the input voltage transient response characteristics. The design aspects, which are specific for the TPS5211 controller (compared to the TPS5210), are described in this application note. The remaining design topics, including the power-train components selection, setting of the hysteresis window, active voltage droop positioning, and overcurrent protection limit are described in the application information section of the product datasheet.[1]

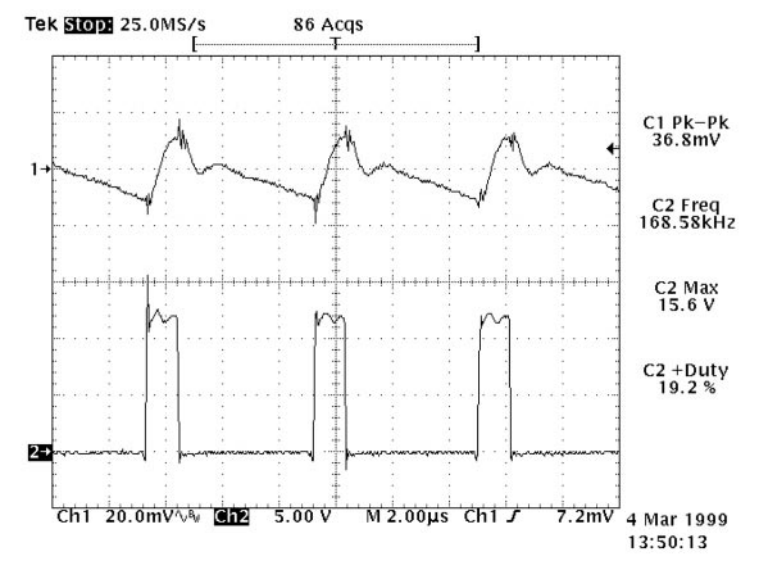
Comparison of TPS5210 and TPS5211 controllers and their application areas

The output voltage ripple and power-switches midpoint waveforms of the same dc-to-dc converter using the TPS5210 or TPS5211 controllers are shown in Figure 5. The converter using the TPS5210 is optimized for low power losses and high efficiency and operates at 168 kHz, while the same converter using the TPS5211 operates at 450 kHz. In spite of that, the hysteresis window has been set at the same level (20 mV for both controllers) and the peak-to-peak output ripple is 36.8 mV for the TPS5210 and 9.6 mV for the TPS5211. The much lower output ripple for a converter using the TPS5211 does not depend on a hysteresis window.

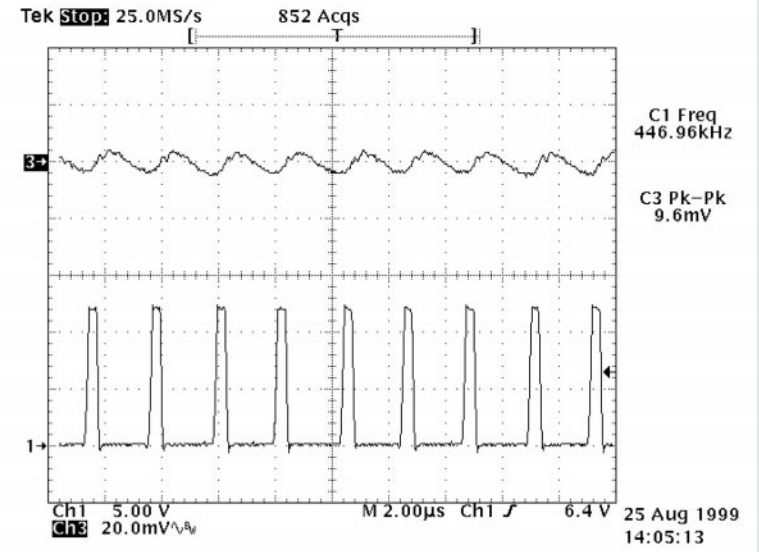
The load current transient response waveforms shown in Figure 6 illustrate that the TPS5211 has the same excellent load current transient response characteristics as the TPS5210.

Both hysteretic controllers have excellent load current transient response characteristics compared with other types of controllers having slow feedback loops like the PWM voltage and current modes. There are application areas where each hysteretic controller has advantages over the other. There are trade- offs relative to which controller is preferable for a specific application and customer requirements. Table 1 compares application areas for TPS5210 and TPS5211 controllers.

Figure 5. TPS5210 and TPS5211 switching waveforms



(A)



(B)

Output voltage ripple and power-switches midpoint waveforms of the same converter using (A) the TPS5210 controller and (B) the TPS5211 with external R_{add} - C_{add} circuitry

Conclusion

The modified hysteretic control approach using TI's TPS5211 controller is described. It is shown that adding simple external circuitry that applies an additional ramp signal to the hysteresis comparator input significantly changes the properties of the dc-to-dc regulator. Its switching frequency becomes independent of output filter characteristics and parasitics, while the output ripple is lower than the hysteresis window. A high switching frequency along with fast transient response enables tight supply voltage tolerance requirements for the next-generation microprocessors and DSPs with a 50–60% lower cost for output filtering.

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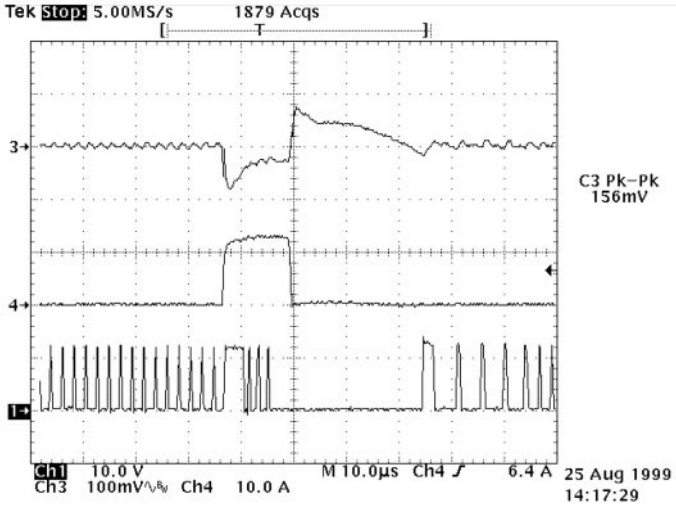
3. "Designing Fast Response Synchronous Buck Regulator Using the TPS5210," Application Report, Texas Instruments Inc., March 1999, literature number SLVA044.
4. "TPS5211 High Frequency Programmable Synchronous-Buck Regulator Controller," Texas Instruments Inc., September 1999, literature number SLVS243.

Figure 6. Output voltage transient response



The output voltage transient response of a converter with the TPS5211 controller. The load current has a 14-A step with a slew rate of 30 A/µS.
Ch.1: Drain-source voltage (10 V/div.)
Ch.3: Output voltage (100 mV/div.)
Ch.4: Load current (10 A/div.)

Table 1. Comparison of the TPS5210 and TPS5211 and their applications

CONTROLLER	TPS5210	TPS5211
Switching frequency (kHz)	100–400	400–700
Frequency variation	Depends on output filter characteristics	Independent of output filter and easy to evaluate
Output current (A)	Up to 40	Up to 18–20 (can be increased in multiphase configuration)
Efficiency (%) (Depends on frequency, output current, V_{IN}, V_{OUT}, components, etc.)	85–95	75–85
Input and output filter	Requires bulk electrolytic capacitors, especially if I_{OUT} > 12 A, and large inductor	Surface-mount ceramic and POSCAP type capacitors and 40–65% smaller inductors
Components cost	20–40% lower for TPS5211	
System cost including reliability, power losses, cooling, etc.	Can be estimated only during design for a given specific application	
Layout and design	Special attention to the noise-sensitive places like hysteresis comparator and sample-hold circuitry	Special attention not to exceed frequency and I_{CC} limits. High-frequency dc-to-dc converter design rules.
Compatibility with the whole system	For high-current applications it is difficult to meet high-density, minimum-size requirements	A dc-to-dc converter can be placed close to microprocessor or DSP to decrease the number of decoupling capacitors

Understanding the stable range of equivalent series resistance of an LDO regulator

By Bang S. Lee
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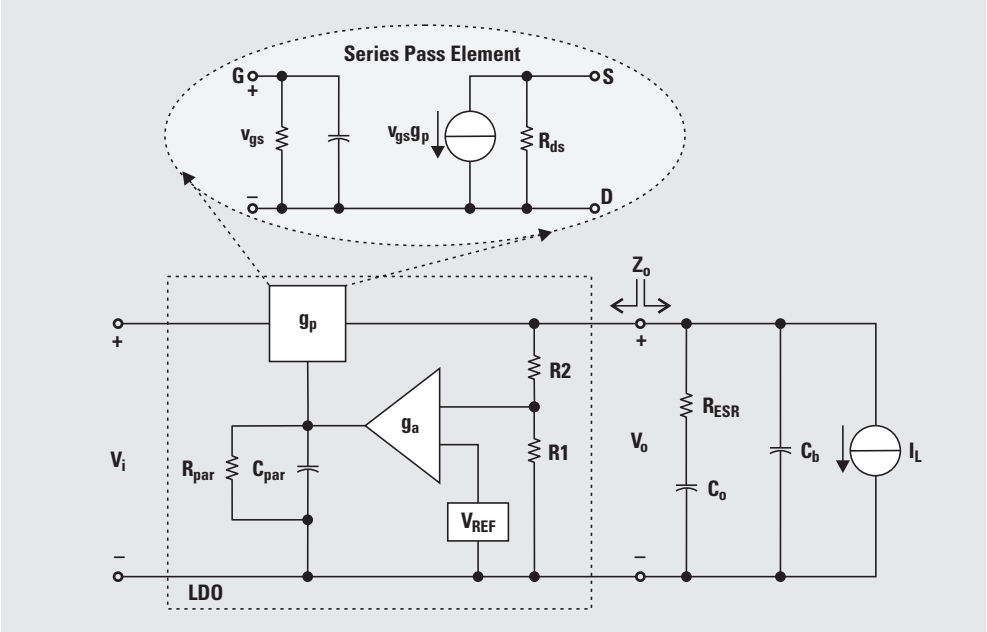
This application note explores the stable range of equivalent series resistance (ESR) values for LDO regulators. An ac model of an LDO regulator is presented to discuss the LDO frequency response. Both stable and unstable ESR ranges are examined.

Figure 1. An ac model of a linear regulator



An ac model of an LDO regulator

Figure 1 shows the essential elements of a PMOS LDO regulator. The LDO regulator can be partitioned into four separate and distinct functional blocks—the pass element, the reference, the sampling resistor, and the error amplifier. The error amplifier is modeled by a transconductor (g_a) with a load comprised of capacitor C_{par} and resistor R_{par}. The parasitic parameters (C_{par}, R_{par}) represent both the output impedance of the error amplifier and the input impedance of the series pass element. The series pass element (PMOS transistor) is modeled by a small signal model with transconductance g_p. An output capacitor C_o with an equivalent series resistor (R_{ESR}) and a bypass capacitor C_b are added.

From Figure 1, the output impedance is given by

$$Z_o = R_{12p} \left\| \left(R_{ESR} + \frac{1}{SC_o} \right) \right\| \frac{1}{SC_b} \qquad (1)$$

$$= \frac{R_{12p}(1 + SR_{ESR}C_o)}{S^2 R_{12p} R_{ESR} C_o C_b + S[(R_{12p} + R_{ESR})C_o + R_{12p}C_b] + 1},$$

where $R_{12p} = R_{ds} \| (R1 + R2) \approx R_{ds}$. (2)

Typically, the output capacitor value C_o is considerably larger than the bypass capacitor C_b. Thus, the output impedance Z_o approximates to

$$Z_o \approx \frac{R_{ds}(1 + SR_{ESR}C_o)}{[1 + S(R_{ds} + R_{ESR})C_o] \times [1 + S(R_{ds} \| R_{ESR})C_b]}. \qquad (3)$$

From Equation 3, a part of the overall open-loop transfer function for the regulator is obtained, and the zero and poles can be found. The first pole is

$$P_o; \quad S(R_{ds} + R_{ESR})C_o = -1 \qquad (4)$$

$$\therefore f_{po} = \frac{-1}{2\pi(R_{ds} + R_{ESR})C_o} \approx \frac{-1}{2\pi R_{ds} C_o} \ (\because R_{ds} >> R_{ESR}). \qquad (5)$$

The second pole is obtained from Equation 3 again:

$$P_b; \quad S(R_{ds} \| R_{ESR})C_b = -1 \qquad (6)$$

$$\therefore f_{pb} = \frac{-1}{2\pi(R_{ds} \| R_{ESR})C_b} \approx \frac{-1}{2\pi R_{ESR} C_b}. \qquad (7)$$

The zero is

$$Z_{ESR};\quad SR_{ESR}C_o = -1 \tag{8}$$

$$\therefore f_{Z(ESR)} = \frac{-1}{2\pi R_{ESR}C_o}. \tag{9}$$

In addition, another pole exists from the input impedance of the pass element (i.e., the output impedance of the amplifier, R_{par}, C_{par}). The approximated poles and the zero of the LDO regulator are then given by

$$P_o \approx \frac{1}{2\pi R_{ds}C_o} \approx \frac{I_L}{2\pi V_A C_o}, \tag{10}$$

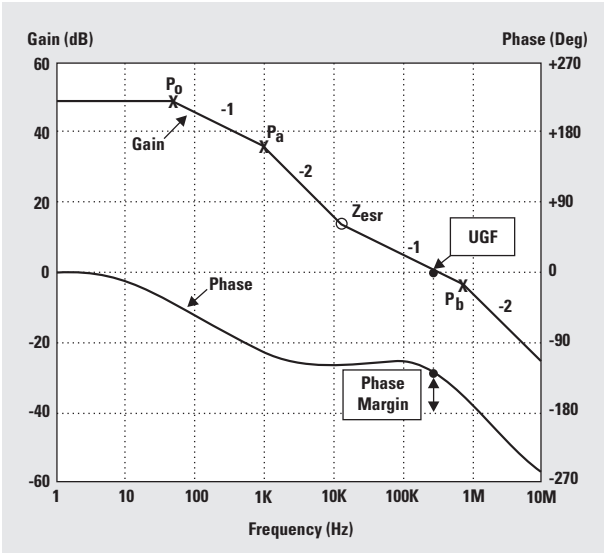
$$P_b \approx \frac{1}{2\pi R_{ESR}C_b}, \tag{11}$$

$$P_a \approx \frac{1}{2\pi R_{par}C_{par}}, \text{ and} \tag{12}$$

$$Z_{ESR} \approx \frac{1}{2\pi R_{ESR}C_o}, \tag{13}$$

where $R_{ds} \approx V_A/I_L$, $V_A = 1/\lambda$ for MOS device, and λ is the channel-length modulation parameter. Pole P_a is the only one introduced at the input of the pass device, not at the output of the device. Based upon the derived poles and zero, the typical frequency response of the LDO regulator is obtained and is shown in Figure 2. Pole P_o depends on the load current. When load current is low, a pole response occurs at relatively low frequencies, thereby degrading phase margin. Worst-case of stability arises at the extreme values of the ESR and at low load currents.

Figure 2. Typical frequency response of the LDO voltage regulator



Range of stable ESR

An LDO regulator would require an output capacitor with an output equivalent series resistor (ESR) to stabilize the control loop. As shown in Figure 3, an LDO has two poles that cause instability if it is not compensated. It is obvious that the linear regulator is unstable because the phase shift at unity gain frequency (UGF) is –180° (i.e., phase margin = 0°) due to the effects of two poles (P_o, P_a) at low

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Figure 3. LDO frequency response without compensation

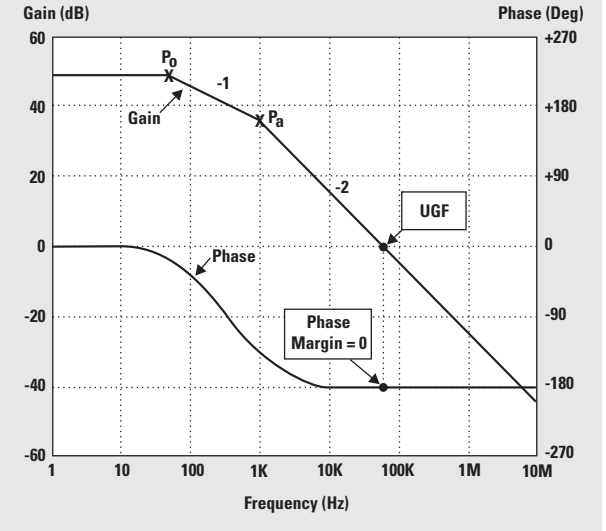
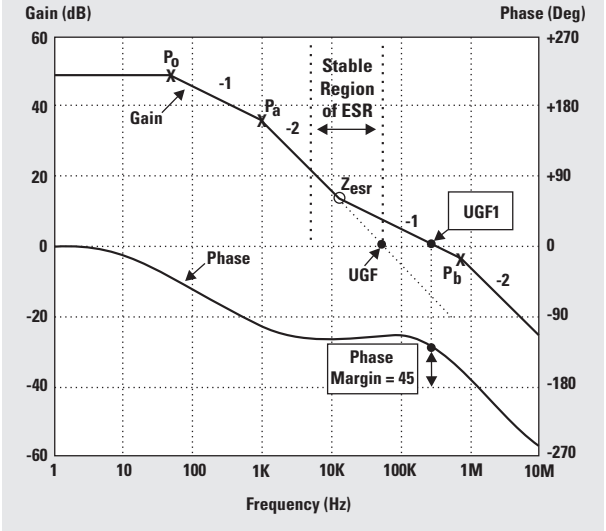


Figure 4. LDO frequency response with external compensation



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frequencies. To make the regulator stable, a zero must be added, which will cancel out the phase effect of one of two poles.

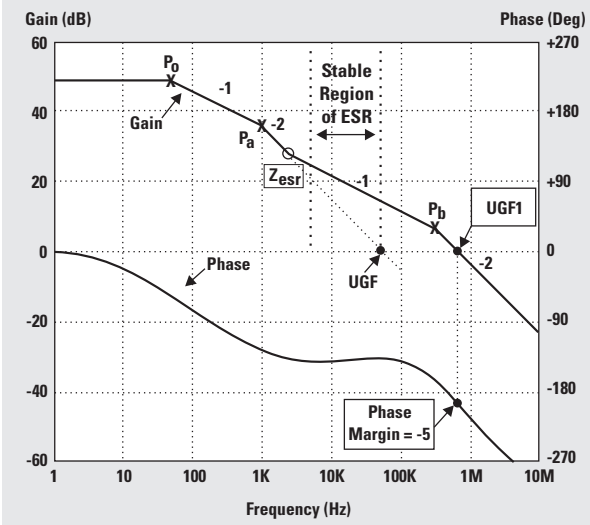
The ESR of an output capacitor or a compensated series resistor (CSR) is used for the zero. Figure 4 shows how the ESR (or CSR) zero stabilizes the control loop. The zero produced by the ESR locates before UGF so that the phase margin at UGF_1 will be higher than 0°. Thus, the linear regulator becomes stable. The phase margin of the control loop at UGF always should be more than 0° for the system stability.

The ESR value should be maintained in the range that determines the loop stability. In most cases, LDO regulators have the minimum/maximum ESR values. Figures 5 and 6 show that the loop responses are unstable even though a zero is added. From Equations 11 and 13, the zero Z_{esr} and the pole P_b are determined by the ESR. When the ESR changes, Z_{esr} and P_b are shifted upward/downward and the loop stability is affected.

Figure 5 illustrates the unstable frequency response of LDO when the ESR is too high, and Figure 6 illustrates the LDO frequency response when the ESR is too low. For both cases, the phase margin at UGF is less than or equal to 0°, resulting in system instability. Figures 5 and 6 show the stable range of Z_{esr}.

Since ESR can cause instability, LDO manufacturers typically provide a graph showing the stable range of ESR values. Figure 7 shows a typical range of ESR values with respect to the output currents (TI TPS76933, 3.3-V LDO regulator). This curve is called the "Tunnel of Death." The curve shows that ESR must be between 0.1 Ω and 8 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the ESR requirements.

Figure 5. Unstable frequency response of LDO with ESR too high



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4. Gabriel Alfonso Rincon-Mora, "Current Efficient, Low Voltage, Low Drop-Out Regulators," PhD Thesis, Georgia Institute of Technology, November 1996.

Figure 6. Unstable frequency response of LDO with ESR too low

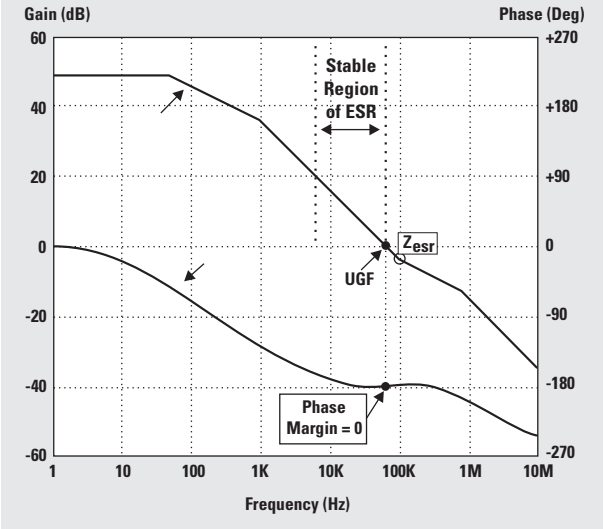
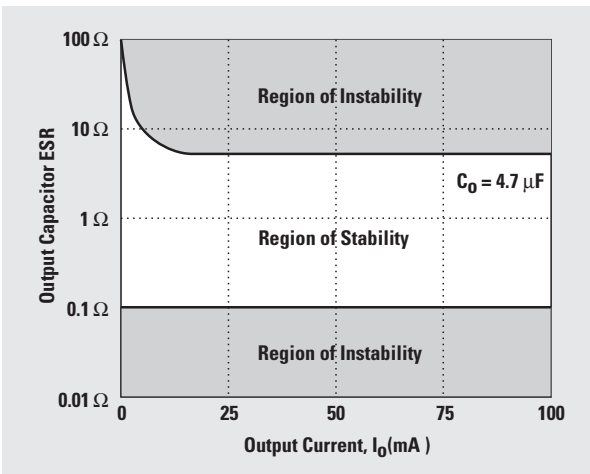


Figure 7. Range of stable ESR values



www.ti.com/sc/docs/products/msp/pwrmgmt/index.htm
www.ti.com/sc/docs/products/analog/tps76933.html

www.ti.com/sc/docs/apps/analog/power_management.html

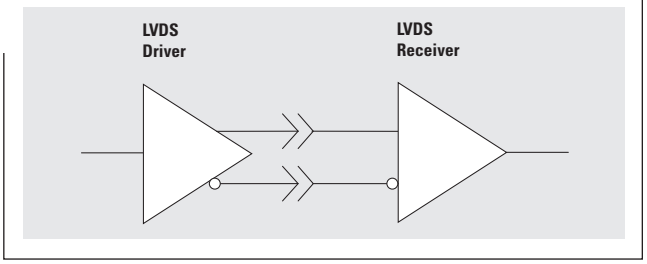
Keep an eye on the LVDS input levels

By E.D. Cole, P.E.
Application Engineer, Data Transmission

Introduction to LVDS input levels

Low-voltage differential signaling (LVDS) systems (see Figure 1) run at extremely high data rates. These systems are unusually robust in terms of noise immunity and V_{CC} stability, and provide an easy way to get data between two points very quickly. One of the design parameters for an LVDS system is the level of the signal provided to the input of the LVDS driver. It is important that the high-level and low-level inputs to the LVDS driver be kept balanced (symmetrical) about the threshold voltage where the driver switches the output between states.

Figure 1. An LVDS system



Impact of non-symmetrical inputs

It is easy to see the effects of a non-symmetrical input. As shown in Figure 2, the receiver output appears distorted when the inputs are not centered on the V_{THRES} switching level of the driver.

LVDS level specifications

The input levels to a 3.3-V LVDS line driver are specified as 0.0 V_{DC} to 0.8 V_{DC} for a logic-0 and 2.0 V_{DC} to 3.0 V_{DC} for a logic-1. Input levels between 0.8 V_{DC} and 2.0 V_{DC} are undefined, which means that a driver's switching threshold voltage is also undefined, but it is not hard to determine. By applying a clock signal into the system and adjusting the input levels V_{IH} and V_{IL} while monitoring the receiver output for a 50% duty cycle, the data in Figure 3 is obtained. The values of V_{THRES} shown in Figure 3 are calculated from the V_{IH} and V_{IL} input levels. Note that this can be interpreted as the input sensitivity, not just for the LVDS driver but for the entire LVDS system. The calculated results show a V_{THRES} of approximately 1.35 V_{DC} independent of the data (or clock) rate.

Amplitude and offset

Figure 4 shows the driver output when the input levels are not centered on the input threshold. The Channel 1 waveform (approximately 52% duty cycle) is the driver output when V_{IH} = 2.35 V_{DC} and V_{IL} = 0.35 V, which is closely centered about the 1.35-V threshold. But note the Channel 2 waveform in Figure 4 (approximately 60% duty cycle). This shows the driver output response to an input with V_{IH} = 2.5 V_{DC} and V_{IL} = 0.5 V_{DC}. This is still at a 2.0-V_{PP} amplitude but is centered at 1.5 V_{DC}. The result is a slight "skew" in the output. The duration of a logic-1 has increased by approximately 640 psec at the expense of the duration (or width) of the logic-0.

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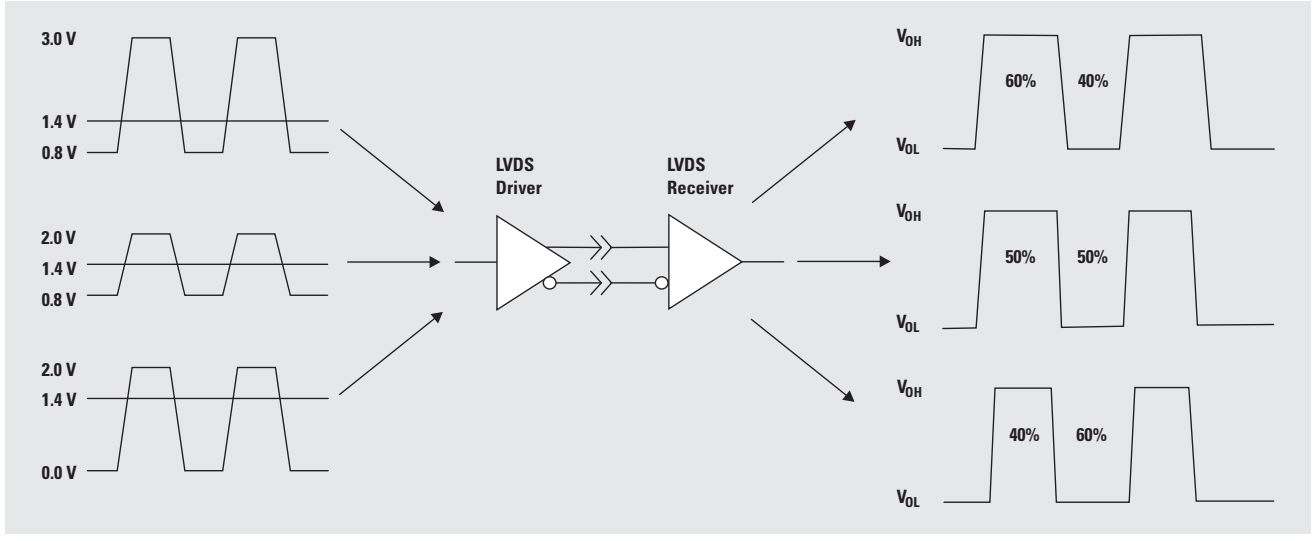
Figure 2. Outputs appear distorted when inputs are not symmetrical



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When used for clock distribution, this skew is not a problem because the rising and falling edges are clean and stable. High-speed clock signals are rarely perfect square waves with a 50% duty cycle, but when transmitting data (in this example it would become 200 Mbps) this skew could present a problem. At 200 Mbps, each data bit would be 5 nsec wide, but the results in Figure 4 show the Channel 2 waveform with a 0 bit that is 4.36 ns wide (5.0 ns – 0.64 ns) and a 1 that is 5.64 ns wide (5.0 ns + 0.64 ns). The difference between a 0 and 1 would be 1.28 ns, with V_{IH} = 2.5 V_{DC} and V_{IL} = 0.5 V_{DC}—well within the specification.

As long as the inputs are centered about the input threshold, the output will maintain the correct duty cycle and bit width. The reader should think of this as an input amplitude and offset. In Figure 5, Channel 1 is the driver output when the input amplitude is 1.5 V_{DC} with an offset of 1.35 V_{DC} (V_{IH} = 2.1 V_{DC} and V_{IL} = 0.6 V_{DC}). Channel 2 is the driver output after the input amplitude has been reduced to 0.5 V_{DC} with no change in the 1.35-V_{DC} offset (now V_{IH} = 1.85 V and V_{IL} = 0.85 V). There is no noticeable difference in propagation delay (through the driver) or shift in duty cycle out of the driver. These inputs levels do not meet the LVDS specification, but work well.

Figure 4. Effects of non-symmetrical inputs on the output waveform

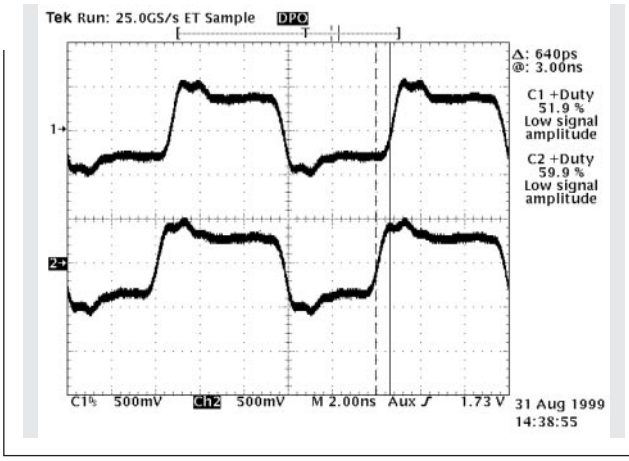


Figure 5. Output response to different amplitude levels but the same offset voltage

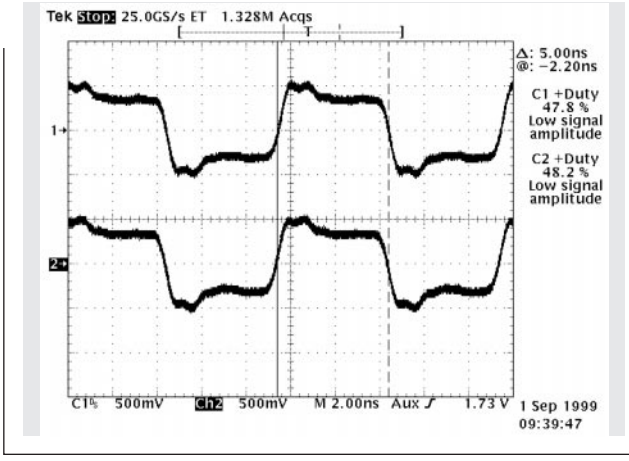
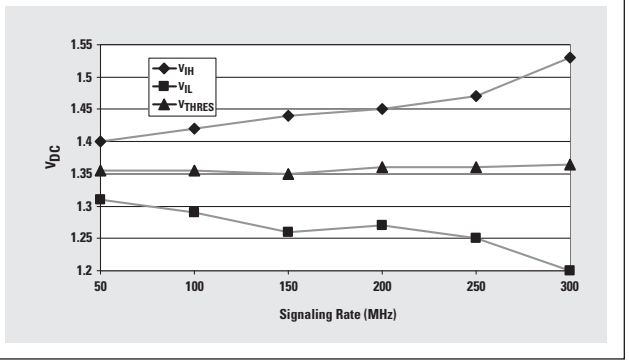


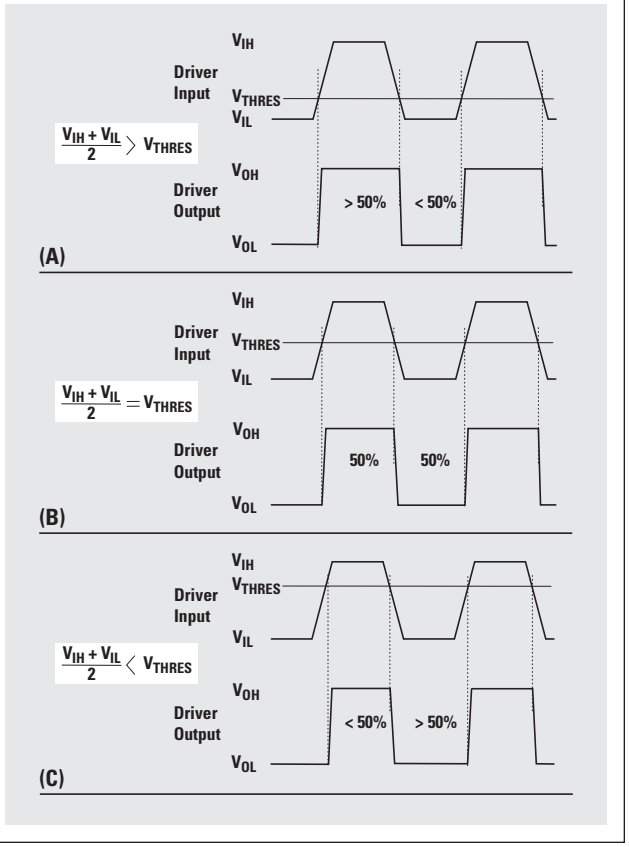
Figure 3. Minimum differential input levels to an LVDS system



Why does the duty cycle change?

The answer to this question is shown in Figure 6. In Figure 6(A), the input levels are centered above the threshold, which results in an increase in the positive

Figure 6. Driver output characteristics vs. input levels



duty cycle. In Figure 6(B), the inputs are centered, which results in a 50%/50% duty cycle. Figure 6(C) shows the input levels centered below the threshold, a condition resulting in a decrease in the positive duty cycle. Figure 6(C) also shows the driver's response to its input signal. This change in duty cycle for NRZ data streams translates into a difference between the width of 0's and 1's.

Threshold adjustment

The threshold cannot be adjusted, but the input levels might be adjustable. The data in Figure 3 shows that even at high signaling rates the input sensitivity to an LVDS driver is approximately 300 mV (and less at slower signaling rates). This means it may be possible to adjust the input signal by installing a resistor divider at the driver input.

The author simulated a 100-MHz clock distribution system with V_{IH} = 3.5 V and V_{IL} = 0.5 V_{DC} (amplitude = 3.0 V, offset = 2.0 V_{DC}) to the driver. To bring the offset voltage down near the driver's threshold voltage, the resistor divider network shown in Figure 7 was installed.

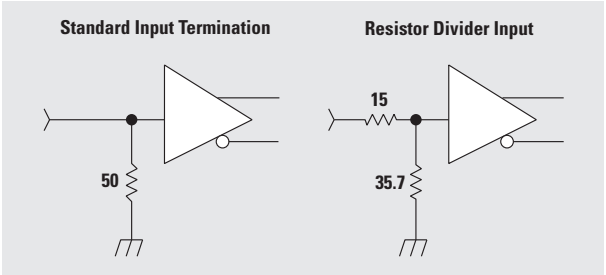
This divider reduces the offset from 2.0 V to 1.4 V, very near the threshold voltage of the driver. It also reduces the input amplitude by 30%, making V_{IH} = 2.46 V_{DC} and V_{IL} = 0.35 V_{DC}.

Performance of this modified input was compared to another driver having the standard 50-ohm input termination. The results are shown in Figure 8. Notice that the Channel 1 waveform is very symmetrical with a very good duty cycle. The Channel 2 waveform has an offset voltage of 2.0 V_{DC} and produces the increased (57%) positive duty cycle result expected.

Data transmission

What happens when the driver is sending data? A shift in duty cycle is the same as a "skew" in the width of data bits—1's and 0's will not be the same width. This can be seen using eye patterns to view the serial data stream. Figure 8 shows how, using two clock inputs, the resistor divider can be used to center the offset level. By changing these inputs from "clocks" to random data (NRZ formatted) the serial data stream using eye patterns can be viewed. The input levels have not been changed.

Figure 7. Using a resistor divider to "center" the input levels



The Channel 1 trace contains the eye pattern for the adjusted signal. The divider has aligned the input very near the switching threshold of the LVDS driver, and the output has the familiar "X" at the crossovers indicating the system is switching 1's to 0's and 0's to 1's at the same time. In other words, each bit is the same width.

The Channel 2 trace is the eye pattern for the unadjusted signal. These input levels resulted in the 57% duty cycle waveform shown in Figure 8, and after the format is changed to "data" the corresponding eye pattern shows that the data bits are not the same width. The falling edges are outside the rising edges, so the 1's are wider than the 0's.

Conclusion

In any transmission system, the input levels to the driver are one of many factors that will influence the quality of the signal out of the line receiver. This is true for any line driver, RS-422, LVDS, SCSI, etc. Keep in mind that the distortion evident in the Channel 2 waveform as shown in Figure 9 can be caused by several factors, and in some cases may not even be related to driver input levels. Also, remember that the Channel 2 waveform is the result of input levels (V_{IH} =3.5 V) that are not even within specified limits.

Figure 8. Resistor divider input vs. standard input to an input clock

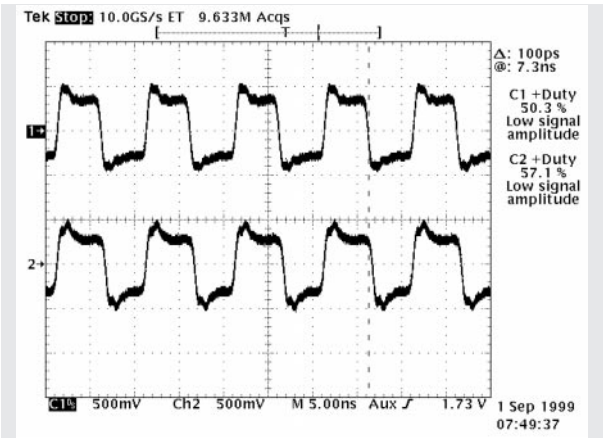
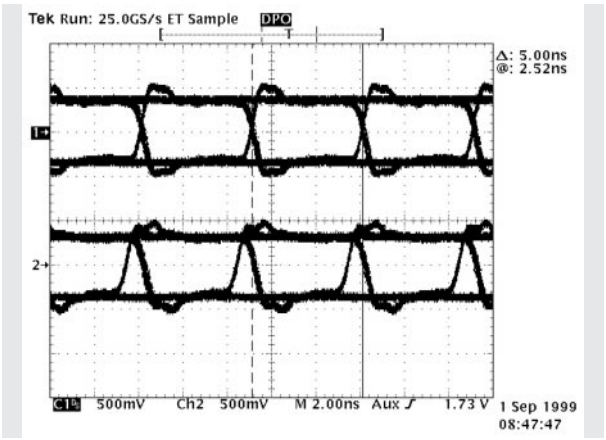


Figure 9. Resistor divider input vs. standard input using eye patterns on serial data



Single-supply op amp design

By Ron Mancini
Senior Application Specialist, Operational Amplifiers

Introduction

Most portable systems have one battery, thus the popularity of portable equipment results in increased single-supply applications. Split- or dual-supply op amp circuit design is straightforward because op amp inputs and outputs are referenced to the normally grounded center tap of the supplies. In the majority of split-supply applications, signal sources driving the op amp inputs are referenced to ground; thus with one input of the op amp referenced to ground, as shown in Figure 1, common-mode voltage and voltage bias problems are negligible.

When signal sources are referenced to ground, single-supply op amp circuits exhibit a large input common-mode voltage (Figure 2). The input voltage is not referenced to the midpoint of the supplies like it would be in a split-supply application; rather, it is referenced to the lower-power supply rail. This circuit malfunctions when the input voltage is positive because the output voltage should go negative; this is hard to do with a positive supply. It operates marginally with small negative input voltages because most op amps cannot function when the inputs are connected to the supply rails.

The constant requirement to account for input references makes it difficult to design single-supply op amp circuits. This application note develops an orderly procedure for designing single-supply op amp circuits that leads to a working design every time. Application Note SLAA068, entitled, "Understanding Basic Analog—Ideal Op Amps," develops the ideal op amp equations. The ideal op amp assumptions used to write ideal op amp equations are shown in Table 1 for your reference.

Figure 1. Split-supply op amp circuit

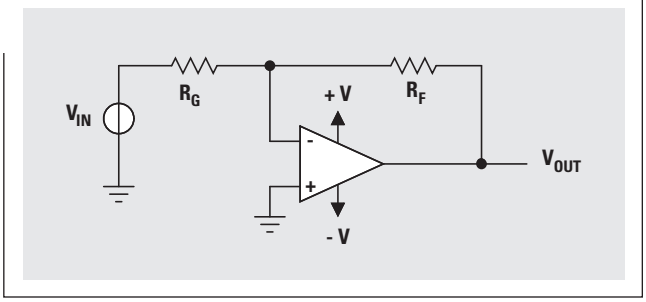


Figure 2. Single-supply op amp circuit

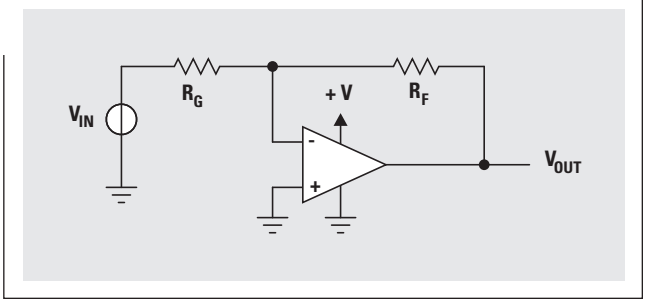


Table 1. Ideal op amp parameter values

PARAMETER NAME	PARAMETER SYMBOL	VALUE
Input current	I_{IN}	0
Input offset-voltage	V_{OS}	0
Input impedance	Z_{IN}	∞
Output impedance	Z_{OUT}	0
Gain	*a*	∞

Boundary conditions

Use of a single-supply limits the output voltage range to the positive supply voltage. This limitation precludes negative output voltages when the circuit has a positive supply voltage, but it does not preclude negative input voltages. As long as the voltage on the op amp input leads does not become negative, the circuit can handle negative input voltages.

Beware of working with negative input voltages when the op amp is powered from a positive supply because op amp inputs are highly susceptible to reverse voltage breakdown. Also, insure that all possible startup conditions do not reverse bias the op amp inputs when the input and supply voltage are of opposite polarity.

Simultaneous equations

Taking an orderly path to developing a circuit that works the first time means following these steps until the equation of the op amp is determined. Use specifications and simultaneous equations to determine what form the op amp equation must have. Go to the section that illustrates that equation form (called a case), solve the equations to determine the resistor values, and you have a working solution.

A linear op amp transfer function is limited to the equation of a straight line.

$$y = \pm mx \pm b \quad \textbf{(1)}$$

The equation of a straight line has four possible solutions depending upon the sign of m (the slope) and b (the intercept), thus simultaneous equations yield solutions in four forms. Four circuits are developed, one for each form of the equation of a straight line. The four equations, cases, or forms of a straight line are given in Equations 2 through 5 where electronic terminology has been substituted for math terminology.

$$V_{OUT} = mV_{IN} + b \quad (2)$$

$$V_{OUT} = mV_{IN} - b \quad (3)$$

$$V_{OUT} = -mV_{IN} + b \quad (4)$$

$$V_{OUT} = -mV_{IN} - b \quad (5)$$

Given a set of two data points for V_{OUT} and V_{IN}, simultaneous equations are solved to determine m and b for the equation that satisfies the given data. The sign of m and b determines the type of circuit required to implement the solution.

The given data is derived from the specifications; i.e., a sensor output signal ranging from 0.1 volts to 0.2 volts must be interfaced into an analog-to-digital converter that has an input voltage range of 1 volt to 4 volts. These data points (V_{OUT} = 1.0 V @ V_{IN} = 0.1 V, V_{OUT} = 4.0 V @ V_{IN} = 0.2 V) are inserted into Equation 2, as shown in Equations 6 and 7, to obtain m and b for the specifications.

$$1 = m(0.1) + b \quad (6)$$

$$4 = m(0.2) + b \quad (7)$$

Solving Equations 6 and 7 yields b = –2 and m = 30. Now m and b are substituted back into Equation 2, yielding Equation 8.

$$V_{OUT} = 30V_{IN} - 2 \quad (8)$$

Notice that, although Equation 2 was the starting point, the form of Equation 8 is identical to Equation 3. The specifications or given data determine the sign of m and b, and starting with Equation 2, the final equation form is discovered after m and b are calculated. The next step is to develop a circuit that has an m = 30 and b = –2 to complete the problem solution. Circuits were developed for Equations 2 through 5, and they are given under the headings Case 1 through Case 4, respectively.

Case 1 — $V_{OUT} = mV_{IN} + b$

The circuit configuration that yields a solution for Case 1 is shown in Figure 3.

Figure 3. Schematic for Case 1 — $V_{OUT} = mV_{IN} + b$

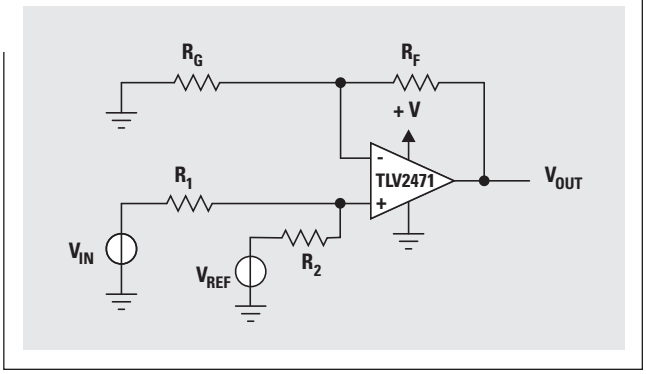
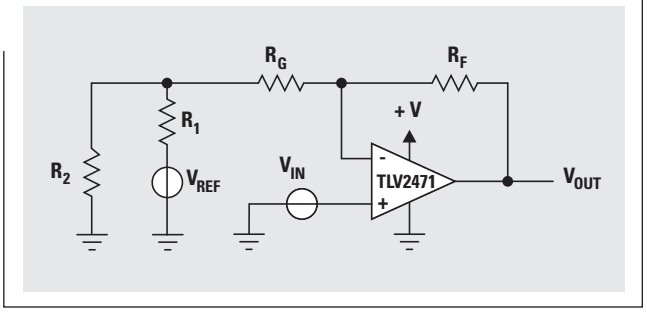


Figure 4. Schematic for Case 2 — $V_{OUT} = mV_{IN} - b$



The circuit equation is written using the voltage divider rule and superposition.

$$V_{OUT} = V_{IN}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) + V_{REF}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \quad (9)$$

$$m = \left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \quad (10)$$

$$b = V_{REF}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \quad (11)$$

Case 2 — $V_{OUT} = mV_{IN} - b$

The circuit shown in Figure 4 yields a solution for Case 2. The circuit equation is obtained by taking the Thevenin equivalent circuit looking into the junction of R_1 and R_2. After the R_1, R_2 circuit is replaced with the Thevenin equivalent circuit, the gain is calculated with the ideal gain equation.

$$V_{OUT} = V_{IN}\left(\frac{R_F + R_G + R_1 \| R_2}{R_G + R_1 \| R_2}\right) - V_{REF}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F}{R_G + R_1 \| R_2}\right) \quad (12)$$

$$m = \frac{R_F + R_G + R_1 \| R_2}{R_G + R_1 \| R_2} \quad (13)$$

$$|b| = V_{REF}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F}{R_G + R_1 + R_2}\right) \quad (14)$$

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Case 3 — $V_{OUT} = -mV_{IN} + b$

The circuit shown in Figure 5 yields the transfer function desired for Case 3.

The circuit equation is obtained with superposition.

$$V_{OUT} = -V_{IN}\left(\frac{R_F}{R_G}\right) + V_{REF}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \quad \textbf{(15)}$$

$$|m| = \frac{R_F}{R_G} \quad \textbf{(16)}$$

$$b = V_{REF}\left(\frac{R_1}{R_1 + R}\right)\left(\frac{R_F + R_G}{R_G}\right) \quad \textbf{(17)}$$

Case 4 — $V_{OUT} = -mV_{IN} - b$

The circuit shown in Figure 6 yields a solution for Case 4. The circuit equation is obtained by using superposition to calculate the response to each input. The individual responses to V_{IN} and V_{REF} are added to obtain Equation 18.

$$V_{OUT} = -V_{IN}\left(\frac{R_F}{R_{G1}}\right) - V_{REF}\left(\frac{R_F}{R_{G2}}\right) \quad \textbf{(18)}$$

$$|m| = \frac{R_F}{R_{G1}} \quad \textbf{(19)}$$

$$|b| = V_{REF}\left(\frac{R_F}{R_{G2}}\right) \quad \textbf{(20)}$$

Figure 5. Schematic for Case 3 — $V_{OUT} = -mV_{IN} + b$

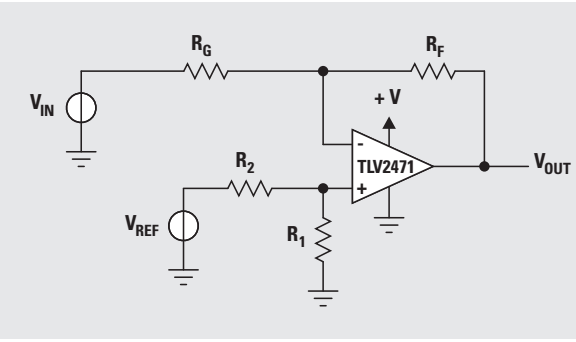
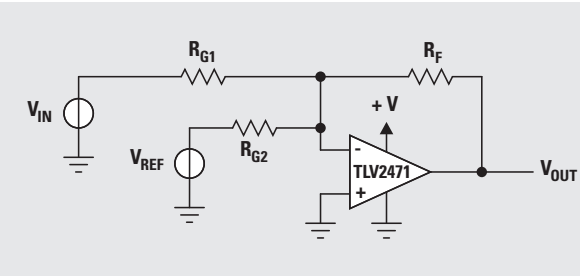


Figure 6. Schematic for Case 4 — $V_{OUT} = -mV_{IN} - b$



Conclusion

Single-supply op amp design is more complicated than split-supply op amp design, but with a logical design approach excellent results are achieved. Single-supply design was considered technically limiting because the older op amps had limited capability. Op amps such as the TI TLV247x, TLC07x, and TLC08x have excellent single-supply parameters; thus, when used in the correct applications, these op amps yield rail-to-rail performance far surpassing their split-supply counterparts. More in-depth information concerning single-supply op amp design can be found in Texas Instruments Application Note SLOA030, entitled, "Single-Supply Op Amp Design Techniques."

www.ti.com/sc/docs/products/msp/amp_comp/default.htm
www.ti.com/sc/docs/products/analog/tlc070.html
www.ti.com/sc/docs/products/analog/tlc080.html
www.ti.com/sc/docs/products/analog/tlv2470.html

Reducing crosstalk of an op amp on a PCB

By Randy Stephens
System Specialist, High-speed Amplifiers

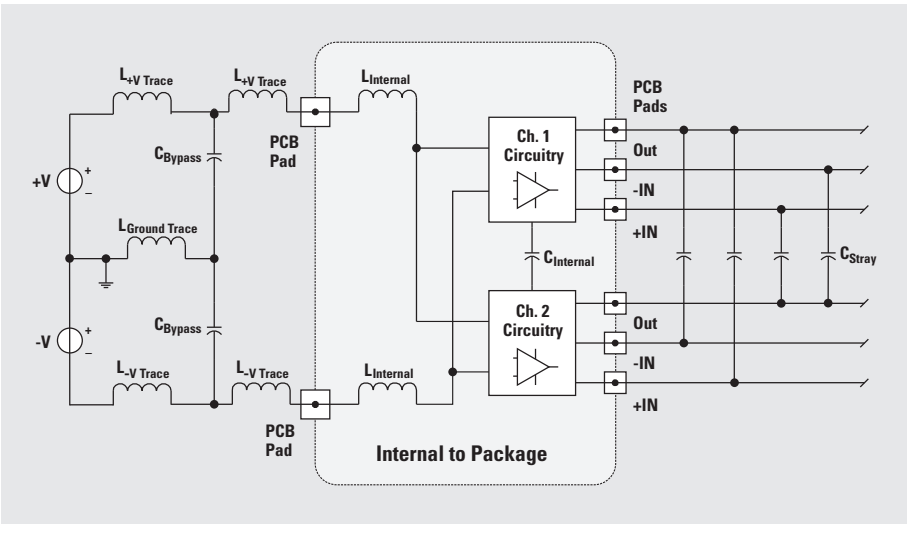
The use of operational amplifiers is common these days. In many instances, it can be advantageous to utilize a dual or quad op amp to save circuit board space and costs, but one of the drawbacks is that the signal from one amplifier may "talk" into the other amplifiers within the single package. This is commonly referred to as crosstalk. To measure crosstalk, a signal is applied to only one amplifier within the package while the outputs of all the remaining amplifiers are probed to determine how much of the source signal is feeding through (or crosstalking). There are several notes and papers on how to minimize crosstalk, but these typically deal only with the silicon and/or packaging. This is not much help to the user of a multi-channel op amp who has no control over what is going on inside the packaged part. The only thing the user can control is the external circuitry and the printed circuit board (PCB) layout. Numerous elements contribute to crosstalk, but the main contributors are shown in Figure 1. Design decisions are based on the measured results, and conclusions are drawn to provide real-world solutions to minimize crosstalk in the TI THS4052 dual-channel high-speed amplifier.

The internals of a dual-channel amplifier

It is helpful to understand what the user does and does not have control over with a dual-channel amplifier. When buying a packaged part, the user has no control over what is inside the package. This includes the lead frame, the silicon die, bond wires, etc. Figure 1 shows the important internal structures that lead to crosstalk within a dual-channel amplifier. Both internal inductors ($L_{Internal}$) on each power-supply line are comprised of the lead-frame pins on the package, the internal bond wires that interconnect the lead frame and the silicon die, and the metal traces within the silicon die itself. Inductors form a low pass filter element that has an impedance directly proportional to frequency ($Z_L = 2\pi fL$). Assume that Channel 1 of this amplifier is producing a signal with a current draw from the power supplies +V and –V. Because both internal inductors represent a high impedance at high frequencies (>1 MHz), the circuitry within Channel 2 most certainly will be affected by the demands of Channel 1. This includes fluctuations of the supply voltages and capacitive coupling into Channel 2's circuitry via the power-supply bus.

There are several ways to minimize these effects, including separate power supplies for each channel, minimizing the bond wire lengths, and using smaller lead frames and packages. Another thing that cannot be controlled by the user is the isolation between the two circuits. Whenever there are two electrical potentials separated by an insulator, a capacitor ($C_{Internal}$) is formed. This stray capacitance allows two signals to couple into each other. The impedance of a capacitor is indirectly proportional to the frequency of the signal ($Z_C = 1/2\pi fC$). Because this capacitance is typically in the low pF range, the coupling will typically start to appear at frequencies greater than 1 MHz. The silicon designer has numerous choices to help minimize this capacitive coupling, including trench isolation, silicon-on-insulator (SOI) topology, physical separation of the circuits, and circuitry geometry. The problem presented to the purchaser of this product is that he has no influence on what the silicon designer has done to minimize crosstalk. Now that we know what we cannot do to minimize crosstalk, let's look at what we can do.

Figure 1. Simplified crosstalk components of a dual op amp on a PCB



Power-supply rules

Figure 1 shows that the inductance of the power supplies could be a big factor associated with crosstalk. To make matters worse, in order to connect the op amp to a power source, traces must be used. These traces can run several inches. Since any piece of electrically conducting wire (like a PCB trace) has an inductance based on the length of the wire (around 15 nH per inch), the previous problem of

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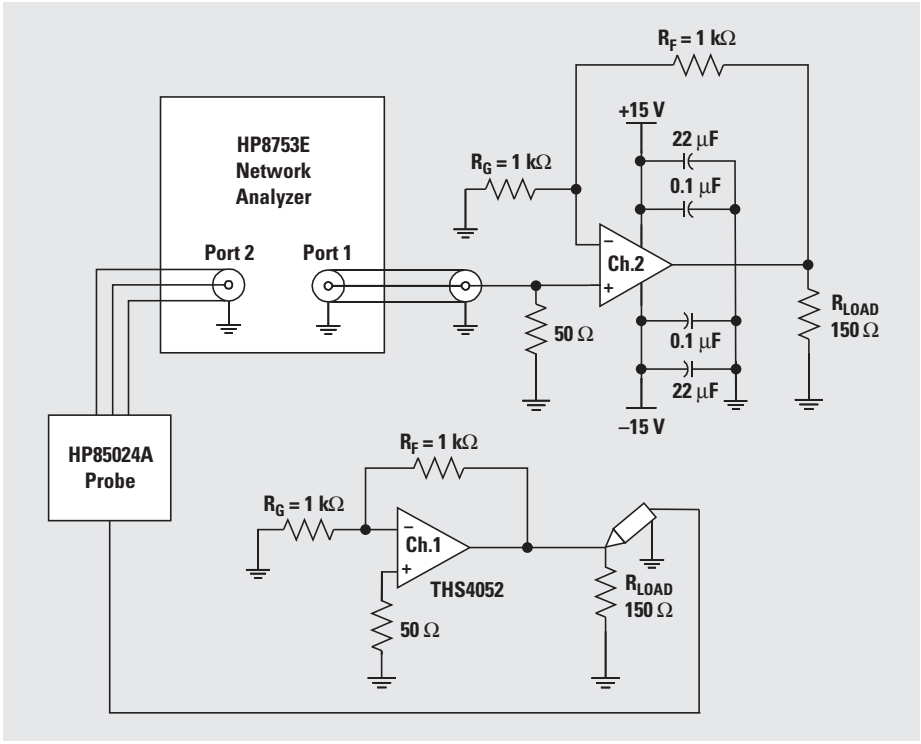
inductance on the power supply only gets worse. In fact, the PCB trace can easily have much more inductance than that of the packaged part itself.

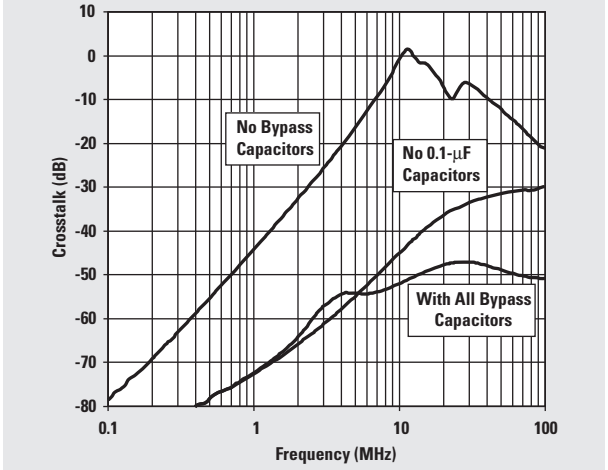
The cure for this inductance problem is easy to implement by using bypass capacitors. These capacitors should be located physically as close as possible to the op amp power-supply pins. When it comes to dealing with high-frequency amplifiers that have bandwidths exceeding 50 MHz, the distance between the pin and the bypass capacitor can be extremely critical. These bypass capacitors should have very good high-frequency characteristics, which usually precludes the use of large electrolytic or tantalum capacitors. Large "bulk" capacitors play an important role in supplying lower-frequency currents, but they do not perform very well with frequencies above 1 MHz.

Figure 2. Default test circuit set-up configuration



The most common type of capacitor used for high-frequency bypass is the ceramic capacitor. Using surface-mount technology (SMT) components over leaded parts is also recommended. This will virtually eliminate the lead inductance of the capacitor, making the capacitor behave more like the "ideal" capacitor. To see the benefits, the ground side of the bypass capacitors should always be connected to the ground plane with vias or as short a trace as possible. The trace is an inductor at high frequencies, counteracting the good bypassing effects of the capacitor. There are numerous other ideas to improve power-supply decoupling, but they tend to cost more and consume precious board space.[1] For most circuits, though, the use of a simple 0.1-µF or 0.01-µF ceramic capacitor in parallel with a large tantalum or electrolytic capacitor will provide sufficient power-supply decoupling.

Figure 3. Power-supply decoupling crosstalk results



A few tests will illustrate the effects of power-supply decoupling. These tests were done using a THS4052 high-speed amplifier packaged in an MSOP PowerPAD™ package. Because this amplifier has a bandwidth of 70 MHz, the crosstalk frequency range was limited to 100 MHz. Refer to Figure 2 for the test set-up and amplifier configurations and to Figure 3 for the results.

As Figure 3 shows, removing the 0.1-µF capacitors made the crosstalk worse by almost 10 dB at 10 MHz and by over 20 dB at 100 MHz. For experimentation purposes, the 22-µF tantalum bypass capacitors were also removed to see the effects on crosstalk. As expected, the crosstalk became much worse across the entire frequency range.

Looking at Figure 1, we see that the supply voltages (+V and –V) should not cause any changes in crosstalk performance. To verify if this was true, the results for all the tests conducted throughout this application note were taken with ±15-V and ±5-V supplies. As expected, the crosstalk performances with different supply voltages were practically indistinguishable from each other. The power supplies do not play any significant role with respect to crosstalk issues and will be ignored for the remainder of this discussion.

One question arises from this figure. Why does the crosstalk start dropping again at high frequencies when there are no bypass capacitors? There are two answers. The first is that since the amplifiers were connected with a gain of +2, the bandwidth of this voltage feedback amplifier will be around only 35 MHz (following the traditional gain-bandwidth product). Above this frequency, the amplitude of both amplifiers starts to drop off and the current demand on the power supply is also reduced, minimizing the effects of the trace inductances.

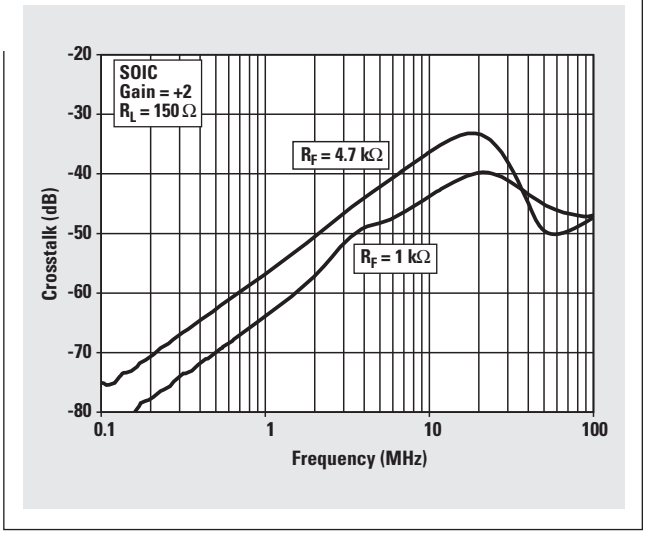
The second answer is that the utilization of a ground plane on the PCB helps minimize the lead inductance problem. As the power-supply trace runs on top of the ground plane, some distributed capacitance is formed. This capacitance performs exactly the same job as the small ceramic capacitors originally performed—not quite to the extent of the real 0.1-µF capacitor, because the equivalent capacitance value is much less.

Taking this idea the next step, a power plane for each supply voltage and at least one ground plane can significantly increase the high-frequency power-supply bypassing effects. The first thing this does is to minimize the trace inductance of the power supplies. The greater the surface area, the lower the inductance. The second benefit provided by power planes is a very large, uniformly distributed power-supply bypass capacitor. This capacitance can be extremely helpful when dealing with frequencies greater than 100 MHz. Not all PCB designs lend themselves to utilizing multi-layer PCBs, though. At the very least, a ground plane should be utilized on at least one side of a PCB to eliminate the $L_{Ground\ Trace}$ inductance. This can be easily accomplished by filling the unused portions of the PCB with a ground plane. Just make sure that there are no isolated "islands" on the board. They should be connected to the ground plane by PCB vias, or simply eliminated.

Amplifier resistor selection

No matter how an amplifier is used, resistors are used to give an amplifier a specific response. Sometimes designers have no choice in the resistances used to close the amplifier loop. But, if any resistor value can be chosen, there are some choices to make related to crosstalk performance.

Figure 4. Effects of feedback and gain resistors on crosstalk—SOIC



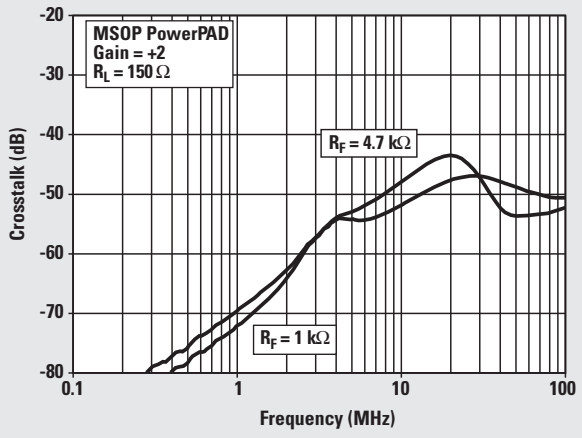
As shown in Figure 1, the output pins and input pins can couple into each other by stray capacitances. Notice that crosstalk directly into the output trace is usually not a problem. This is because the closed loop impedance of an amplifier is very small, allowing the amplifier to overcome just about any form of crosstalk coupling.

The same does not hold true when it comes to the inverting and non-inverting input pins of the amplifier. This is because the input impedance of these pins is generally very high. In the case of FET amplifiers, it can approach 10^{12} ohms. This is very important because the amount of stray capacitance required to inject a signal is tied indirectly to the impedance of a circuit node. When the impedance of a capacitor (Z_C) is equal to the nodal resistance, the amount of signal injection has reached the half-power point (–3 dB). If the frequency increases or if the capacitance is increased, it is obvious that the amount of signal injection will also increase. But if the nodal resistance can be lowered, the effects of the stray capacitance can be reduced.

This idea is the basis for the next design rule to help reduce crosstalk. Simply use smaller resistances for both the inverting and non-inverting nodes of an amplifier. For the inverting node, which must have a feedback resistor (R_F) and usually a gain resistor (R_G), the ac nodal resistance is equivalent to the parallel resistance of both of these resistors. Figures 4 and 5 illustrate this point for the THS4052 in both the standard SOIC package and the MSOP PowerPAD package. The test circuit shown in Figure 2 was also used for this test, with the resistor values as shown in the figures.

The amplifiers were placed into a gain of +2 by making the feedback (R_F) and gain (R_G) resistor values equal to each other. It can be seen that as the ac resistance value

Figure 5. Effects of feedback and gain resistors on crosstalk—MSOP



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at the inverting node decreased, the crosstalk also decreased, especially for the SOIC package. However, there may be some drawbacks to reducing the resistor values. In the case of high-speed amplifiers, the feedback resistor can play a very important role in determining the frequency response of the amplifier. Another thing that is typically overlooked is that the feedback resistor is also part of the load to the amplifier. What happens as the load is increased on the amplifier?

Amplifier loading effects

Recall from the first section that trace inductances, both internal and external, may play a key role in crosstalk. This happens when the current flowing through these inductances starts increasing. The main reason for an increase in current being drawn from the power supplies is that the amplifier is driving a low-impedance load. This load may be reactive and/or resistive, but only resistive loading is considered for comparison. Figures 6 and 7 show the effects of loading on the amplifiers. As the load resistance increases, the crosstalk decreases. At some point, increasing the load resistance may not decrease the crosstalk very much. This is due to the feedback resistor (R_F) becoming the dominant load to the amplifier. In general, the higher the load resistance on the amplifier, the lower the crosstalk will become.

Amplifier configuration considerations

Up to this point all of the results have been shown with the amplifiers in a non-inverting configuration with a gain of +2. This is done to maintain a constant point of reference while changing specific circuit parameters. The next step in the process is trying different amplifier configurations.

The first thing to try is changing the non-inverting gain from +2 to different values. This usually brings up some good questions about what will happen. Lower gains mean that the ac resistance at the inverting node will tend to be higher than with higher gains. But the amplifier will be amplifying the crosstalk signal by only a small gain instead of a larger gain. The next configuration is an inverting configuration. This places the inverting node at a virtual ground, but to the amplifier, a gain of –1 is equivalent to a noise gain of +2. So the only thing that really changes is the source amplifier's input. The measured amplifier is held in the exact same configuration as a gain of +2.

Figures 8 and 9 show the results of different gains and configurations. For all gains shown, the feedback resistance (R_F) was held at 1 kΩ, and the gain resistor (R_G) was adjusted accordingly. Both amplifiers were also configured the same way such that if Channel 2 was set in a gain of +5, Channel 1 was also set in a gain of +5.

The results speak for themselves. It appears that as the gain increases, the crosstalk becomes much worse. It also appears that the inverting gain configuration is the best of

Figure 6. Effects of load resistance on crosstalk—SOIC

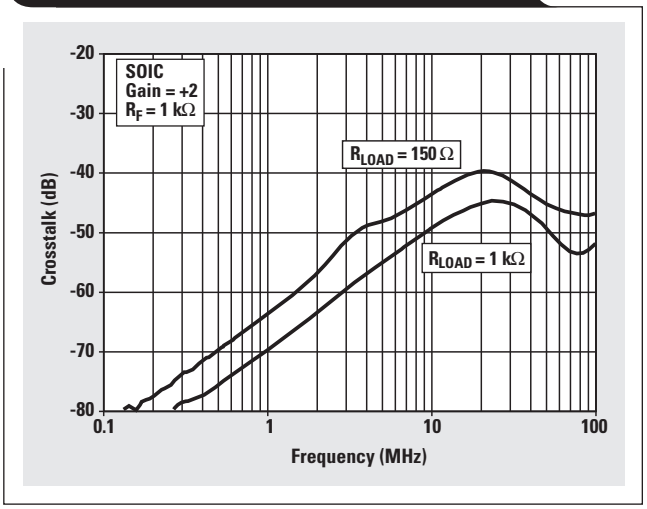


Figure 7. Effects of load resistance on crosstalk—MSOP

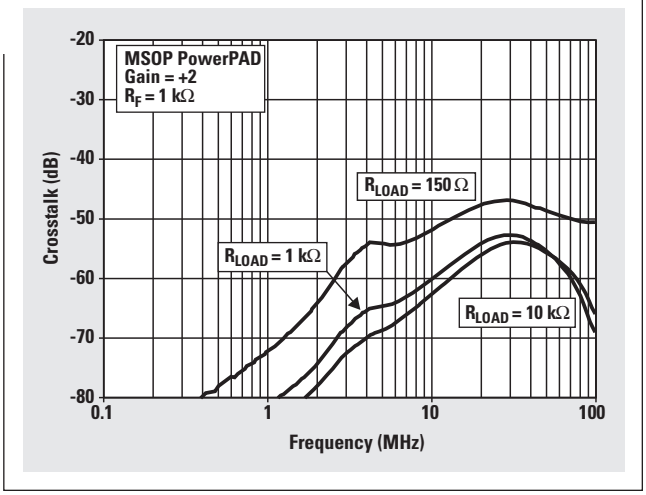
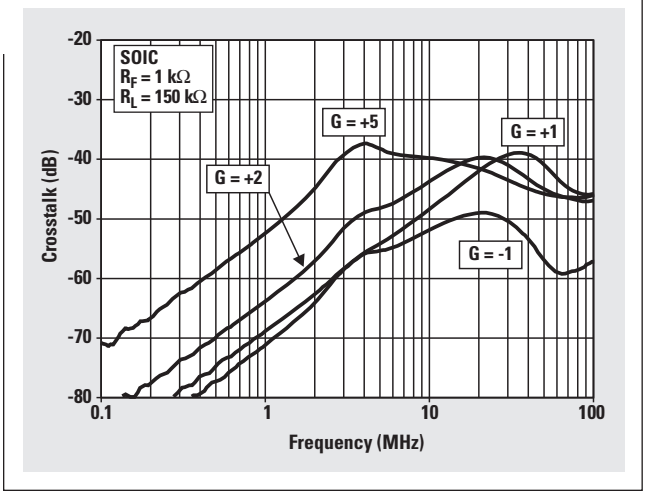


Figure 8. Effects of gain and configuration on crosstalk—SOIC



the test set, surpassing the gain of +2 by a fairly respectable margin. By the non-inverting node being held at ground and the inverting node being held at a virtual ground, the low input impedance appears to have an edge over the non-inverting gain set-up. This configuration also keeps the common-mode input of the amplifier at a fixed reference. Traditionally, this usually keeps the common-mode rejection ratio (CMRR) of the amplifier at its best performance. As long as the stray capacitances and noise levels are held fairly close to each other at both of the input nodes, the CMRR will help keep crosstalk out of the amplifier.

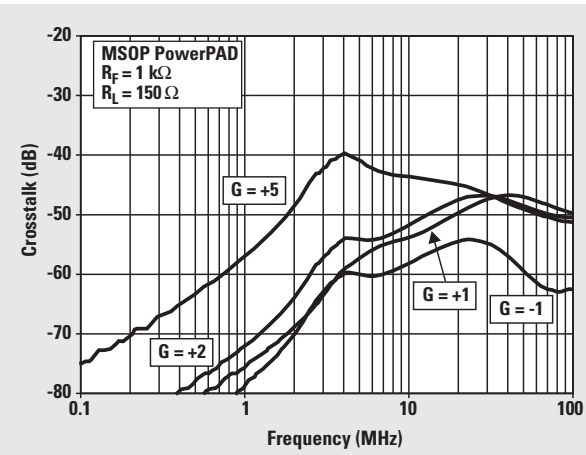
One last configuration to try was the non-inverting buffer configuration with no feedback resistance ($R_F = 0\ \Omega$). This will keep the inverting node impedance very small due to the direct connection to the output of the amplifier. Figures 10 and 11 show that this configuration is the absolute best when it comes to dealing with crosstalk issues. The problem with this configuration is that typically the frequency response of a high-speed amplifier will suffer with a 0-Ω feedback resistance. This is especially true for current feedback amplifiers that must have a feedback resistance for stability purposes. The intent of this application note is to show real-world situations, and this unity gain buffer configuration normally will not be used for high-frequency applications. Instead, there typically will be a feedback resistance that may significantly affect crosstalk performance.

Packaging and layout considerations

The next thing that plays a role in crosstalk is packaging. The choices may include PDIP, SOIC, MSOP, or TSSOP. The packages may give a clue as to which might perform better. Remember that the circuit designer has no control over the internals of the package, so selecting the smallest package possible will probably keep the inductances down to a minimum. In the case of the THS4052, there are two choices—the SOIC and the MSOP PowerPAD package, where the MSOP is substantially the smaller of the two.

In order to see the results of these packages, they must be placed on a circuit board. The PCBs used for all these

Figure 9. Effects of gain and configuration on crosstalk—MSOP



tests were practically identical. Only the landing area for the chips was changed accordingly. The MSOP package has a PowerPAD on the bottom of the chip to improve heat dissipation of the small package. The advantage of this is that the pad is soldered onto the ground plane between all of the pins. This means that there is a low-impedance area to absorb the signals coming from the source amplifier via the ground plane, before the signal couples into the measured amplifier.

The SOIC-packaged amplifier, on the other hand, does not require a ground plane between the pins. The test PCB has a cutout only to minimize leakages between the pins of the amplifier. This does not represent a low-impedance sink to the crosstalk signals. To see if adding a ground area actually does anything, a piece of copper tape was soldered under the SOIC package and connected

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Figure 10. Crosstalk with unity gain buffer configuration—SOIC

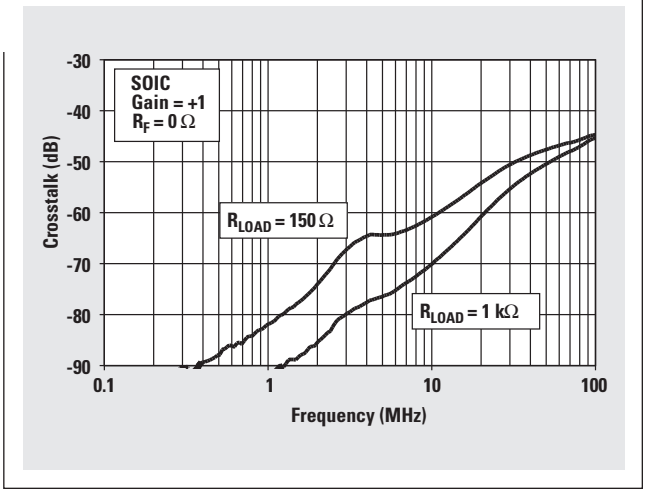
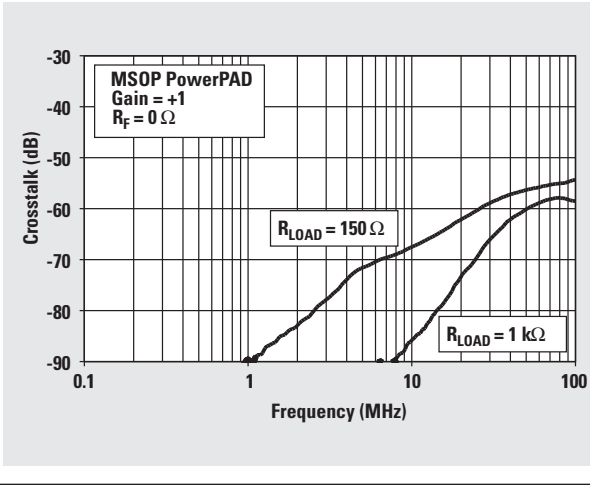


Figure 11. Crosstalk with unity gain buffer configuration—MSOP



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to the ground plane to simulate the MSOP PowerPAD configuration.

Figures 12 and 13 show the results of the different packages. Again, the gain of –1 configuration shows the best real-situation results. The addition of the ground plane under the SOIC package did help with crosstalk by about 5 dB across the entire test frequency range, but it is still not quite as good as the MSOP PowerPAD package.

There are two reasons for this. The first is the physical size of the MSOP PowerPAD package. It is smaller than the SOIC package, reducing inductances. Second, the PowerPAD keeps the substrate of the silicon at a ground reference. Thus the two channels inside the package have a low-impedance noise "sink" and do not allow the substrate to act as a noise-coupling device into the adjacent channel. The SOIC package, on the other hand, does not have this extremely low-impedance system. To keep the substrate at a fixed level, it is fairly common to connect one of the power-supply pins to the substrate. The drawback is that the pin itself has the same lead inductance as shown in Figure 1, reducing the effectiveness of this noise "sink."

It cannot be denied that a ground plane does improve the SOIC crosstalk response. Instead of placing a ground between the pins, it makes sense that power-supply traces between the leads would also serve the same purpose as the ground plane. Just keep in mind that usually the power-supply traces will not have as low an inductance, and hence impedance, as a true ground plane. Another concern is that power-supply noise also may be capacitively coupled into the chip by the traces being directly under the silicon die. A good power-supply plane should remedy all of these possible problems.

General design guidelines and conclusions

The results of this testing have shown several things to look for when crosstalk is an issue. Some things were not tested in detail but generally can be accepted as true based on experience and extrapolation of this data. The keys to attaining a high crosstalk rejection include:

1. Use 0.1-µF or 0.01-µF SMT ceramic bypass capacitors as close as possible to the power-supply pins on each and every amplifier.
2. Use a very large ground plane on the PCB.
3. Use a power-supply plane for each supply voltage if possible.
4. The best crosstalk performance is achieved with a gain of +1 configured with a 0-Ω feedback resistance. But, for most applications, use a gain of –1 if possible.
5. Keep the amplifier gain to a minimum.
6. Keep the feedback (R_F) and gain (R_G) resistances down to a minimum.
7. Use as high a load resistance as your design allows.
8. Pick a small surface-mount (SMT) package.
9. Consider the PowerPAD package with the pad soldered directly to the ground plane.
10. If using a non-PowerPAD package, place a ground pad or low-impedance traces between the pins.
11. Keep non-inverting and inverting pin traces to a minimum. The longer the trace, the more stray capacitance it will have.
12. If design allows, put guard traces around the input pins of the amplifier. This guard trace should be connected to the ground plane for high isolation.
13. Keep the ground return path of the load routed away from the amplifier's input traces.
14. Isolate the traces for each amplifier from the other amplifier(s) as much as possible.

Following these rules should minimize crosstalk issues in PCB design and allow the user of multi-amplifier packages to save PCB space and money.

Figure 12. Effects of packaging and PCB on crosstalk—Gain = +2

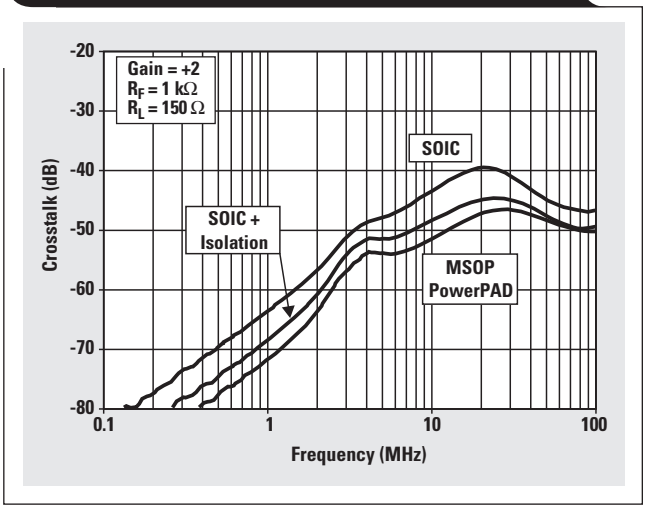
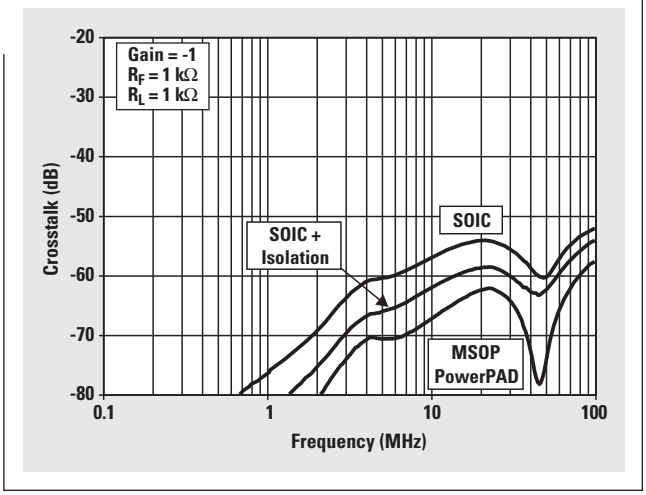


Figure 13. Effects of packaging and PCB on crosstalk—Gain = –1



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