Designing Switching Voltage Regulators with TL494

Application Report

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Abstract

In this application report, the TL494 switching power supply control is discussed in detail. A general overview of the device's architecture presents the primary functions contained in the 16-pin dual-in-line package and its features. An in-depth study of each of the device's primary building blocks highlights the versatility and limitations of the control circuit and gives a thorough understanding of their interrelationship. Applying the control circuit to several basic applications demonstrates the circuits' usefulness and outlines some still unresolved problems.

Introduction

Over the past few years, a series of monolithic integrated circuits for the control of switching power supplies have been introduced. One of these, the TL494, combines many of the features previously requiring several control circuits. The TL494 simplifies many design problems with its unique architecture. It is the purpose of this application report to give the reader a thorough understanding of the TL494, its features, its performance characteristics, and its limitations.

The Basic Device

The design of the TL494 not only incorporates the primary building blocks required for the control of a switching power supply but also addresses many basic problems and reduces the amount of additional circuitry required in a total design. Figure 1 shows a block diagram of the TL494.

Principle of Operation

The TL494 is a fixed-frequency pulse-width-modulation (PWM) control circuit. Modulation of output pulses is accomplished by comparison of the sawtooth waveform, created by the internal oscillator on the timing capacitor (C_T), to either of two control signals. The output stage is enabled during that portion of time when the sawtooth voltage is greater than the control signals. As the control signals increase, the period of time the sawtooth input is greater decreases; therefore, the output pulse duration decreases. A pulse-steering flip-flop alternately directs the modulated pulse to each of the two output transistors. Figure 2 illustrates the relationship between the pulses and signals.

The control signals are derived from two sources: the dead-time (off-time) control circuit and the error amplifier circuit. The dead-time-control input is compared directly by the dead-time-control comparator. This comparator has a fixed 100-mV offset. With the control input biased to ground, the output is inhibited during the portion of time the sawtooth waveform is below 110 mV. This provides a preset dead time of approximately 3%, which is the minimum dead time that can be programmed. The PWM comparator compares the control signal created by the error amplifiers. One function of the error

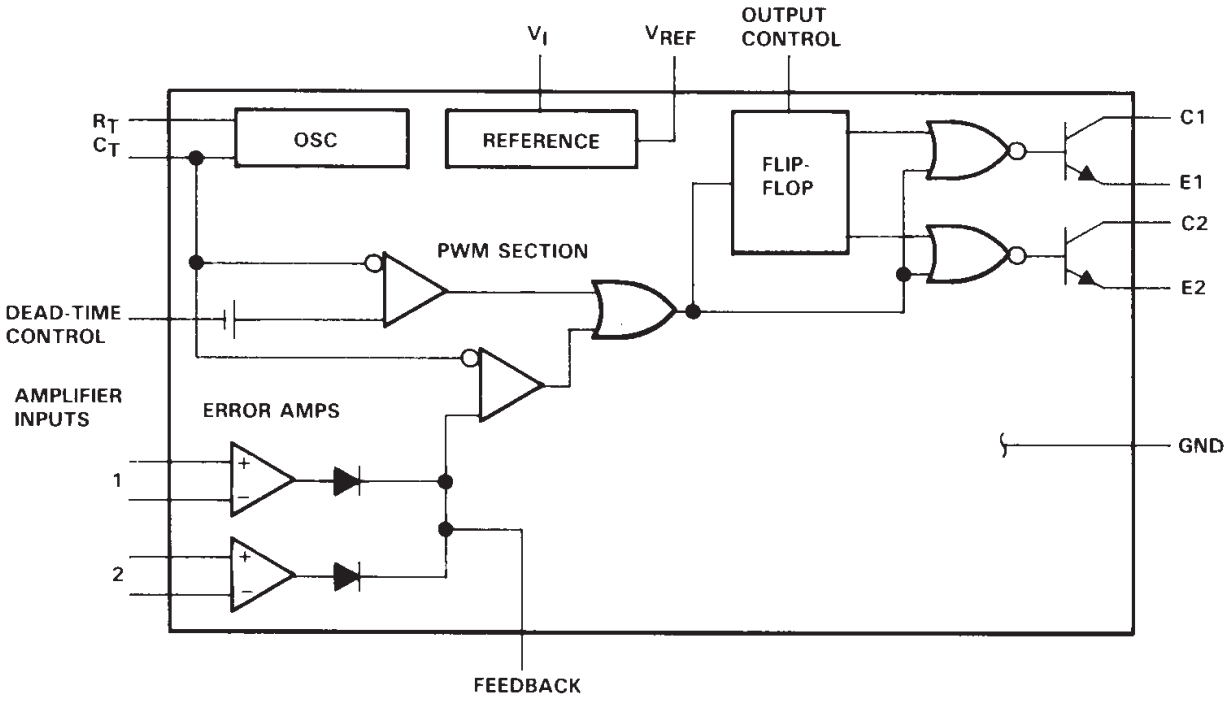


Figure 1. TL494 Block Diagram

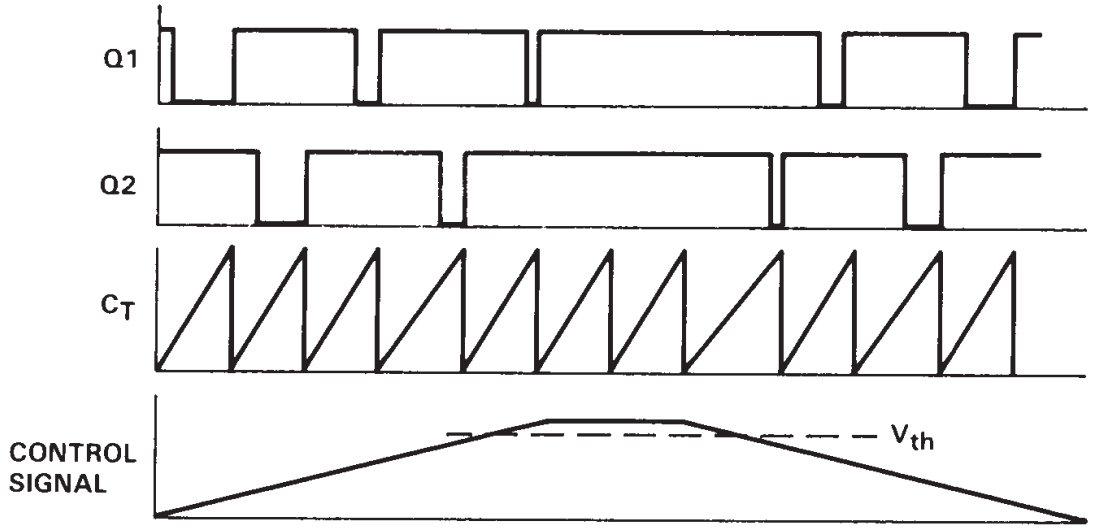


Figure 2. TL494 Modulation Technique

amplifier is to monitor the output voltage and provide sufficient gain so that millivolts of error at its input will result in a control signal of sufficient amplitude to provide 100% modulation control. The error amplifiers can also be used to monitor the output current and provide current limiting to the load.

5-V Reference Regulator

The TL494 internal 5-V reference regulator is shown in Figure 3. In addition to providing a stable reference, it acts as a preregulator and establishes a stable supply from which the output-control logic, pulse-steering flip-flop, oscillator, dead-time-control comparator, and PWM comparator are powered. The regulator employs a band-gap circuit as its primary reference to maintain a thermal stability of less than 100-mV variation over the operating free-air temperature range of 0 °C to 70 °C. Short-circuit protection is provided to protect the internal circuit from excessive load or short-circuit conditions. Designed primarily as an internal reference and preregulator, 10 mA of load current is available for additional bias circuits. The reference is internally programmed to an initial accuracy of ±5% and maintains a stability of less than 25-mV variation over an input voltage range of 7 V to 40 V. For input voltages less than 7 V, the regulator saturates within 1 V of the input voltage and tracks it, as shown in Figure 4.

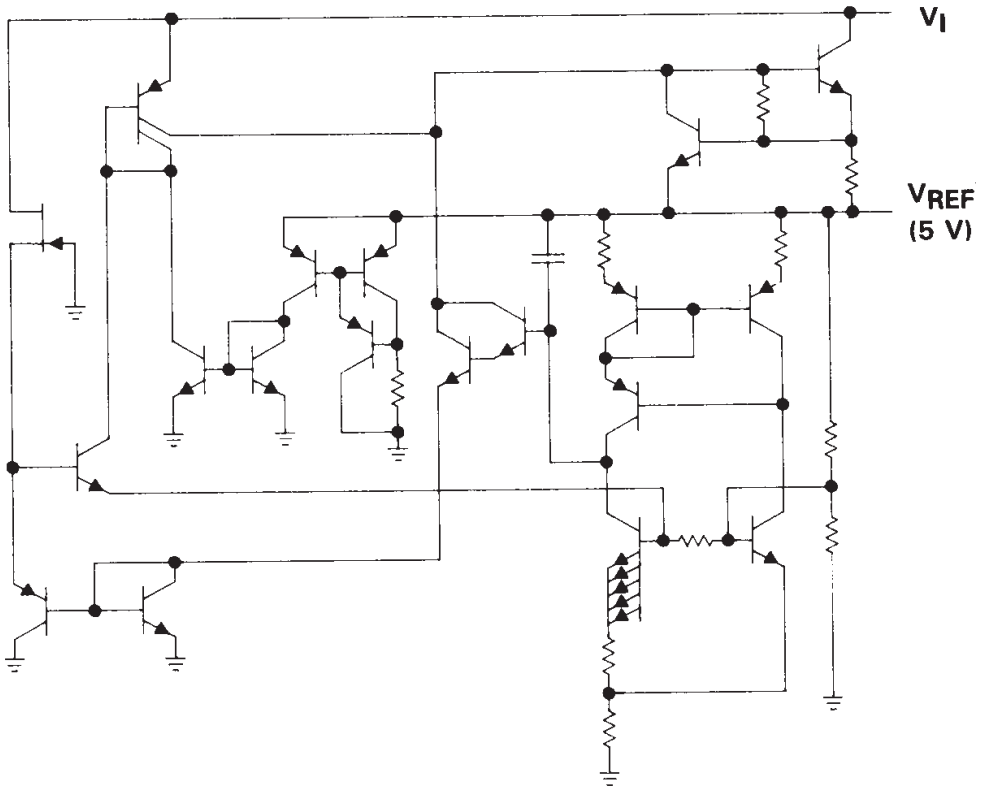


Figure 3. 5-V Reference Regulator

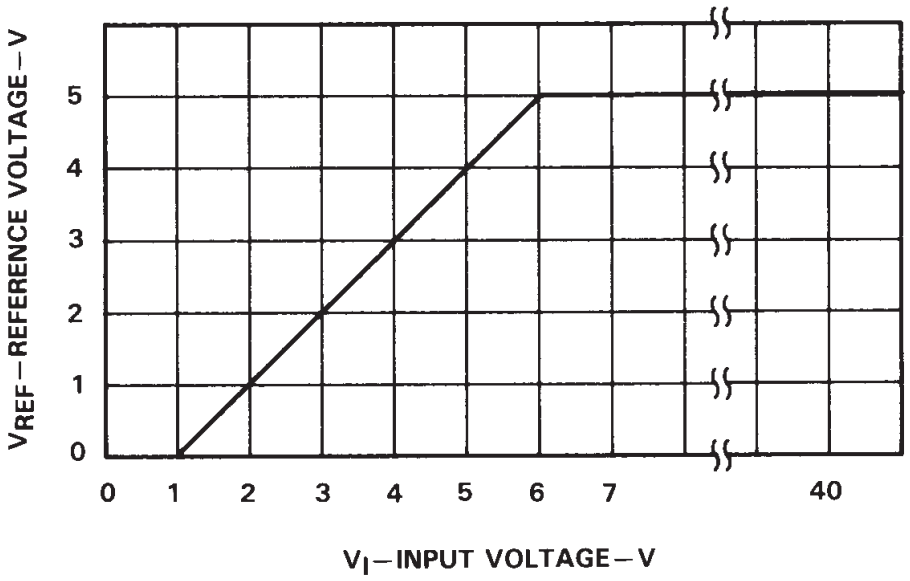


Figure 4. Reference Voltage vs Input Voltage

Oscillator

A schematic of the TL494 internal oscillator is presented in Figure 5. The oscillator provides a positive sawtooth waveform to the dead-time and PWM comparators for comparison to the various control signals.

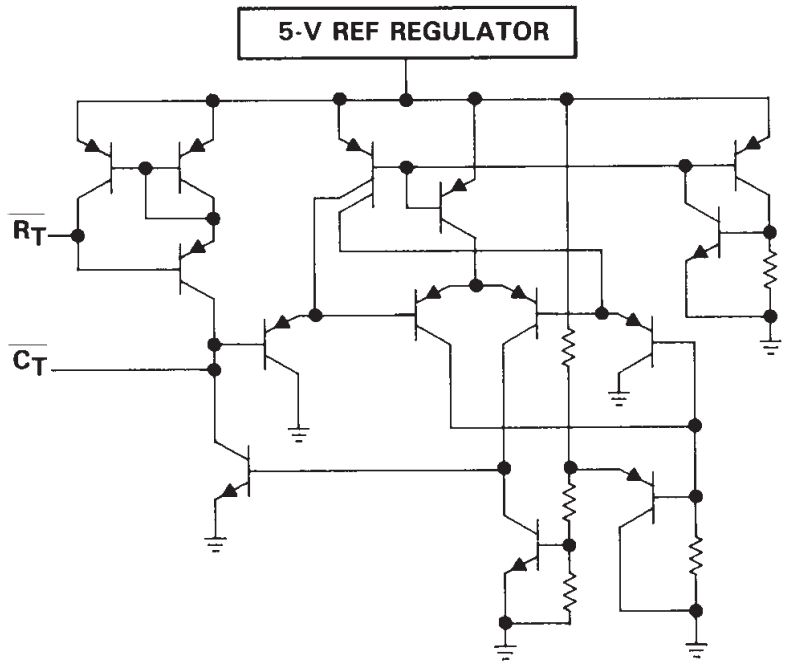


Figure 5. Internal Oscillator Schematic

Operation Frequency

The frequency of the oscillator is programmed by selection of the timing components R_T and C_T. The oscillator charges the external timing capacitor, C_T, with a constant current — the value of which is determined by the external timing resistor, R_T. This produces a linear-ramp voltage waveform. When the voltage across C_T reaches 3 V, it is discharged by the oscillator circuit and the charging cycle is reinitiated. The charging current is determined by the formula:

$$I_{CHARGE} = \frac{3\ V}{R_T}$$

The period of the sawtooth is:

$$t = \frac{3\ V \bullet C_T}{I_{CHARGE}} \qquad t = R_T \bullet C_T$$

The frequency of the oscillator then becomes:

$$f_{OSC} = \frac{1}{R_T \bullet C_T}$$

The oscillator frequency, however, is only equal to the output frequency for single-ended applications; for push-pull applications, the output frequency is one-half the oscillator frequency:

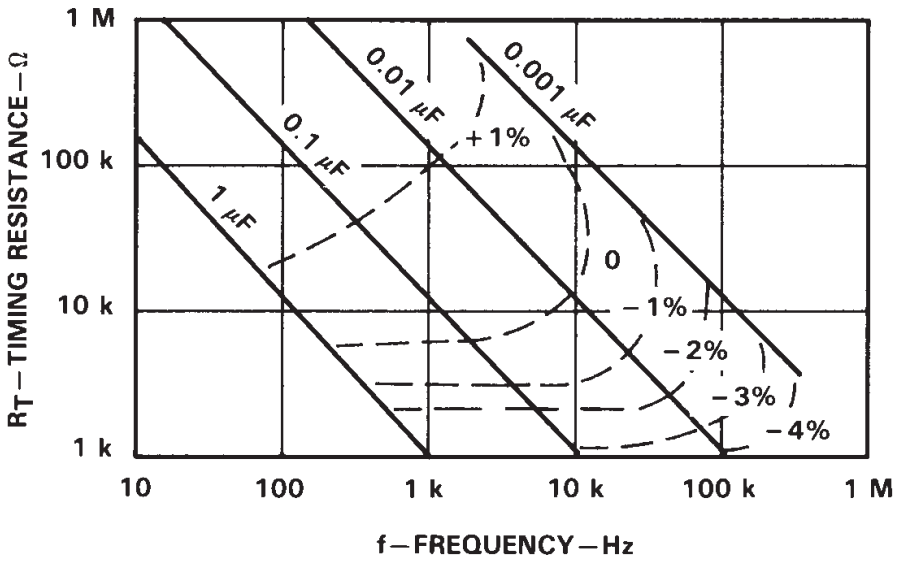
Single-ended applications: $f = \frac{1}{R_T \bullet C_T}$

Push-pull applications: $f = \frac{1}{2R_T \bullet C_T}$

The oscillator is programmable over a range from 1 kHz to 300 kHz. Practical values for R_T and C_T range from 1 kΩ to 500 kΩ and 470 pF to 10 μF, respectively. A plot of the oscillator frequency versus R_T and C_T is shown in Figure 6. The stability of the oscillator, for free-air temperature variations from 0 °C to 70 °C for various ranges of R_T and C_T, is also indicated in Figure 6.

Operation Above 150 kHz

At an operation frequency of 150 kHz, the period of the oscillator is 6.67 μs. The dead time established by the internal offset of the dead-time comparator (≈3% period) yields a blanking pulse of 200 ns. This is the minimum blanking pulse acceptable to assure proper toggling of the pulse-steering flip-flop. For frequencies above 150 kHz, additional



NOTE: The percent of oscillator frequency variation over the 0°C to 70°C free-air temperature range is represented by dashed lines.

Figure 6. Oscillator Frequency vs R_T/C_T

dead time (above 3%) is provided internally to assure proper triggering and blanking of the internal pulse-steering flip-flop. Figure 7 shows the relationship of internal dead time (expressed in percent) provided for various values of R_T and C_T.

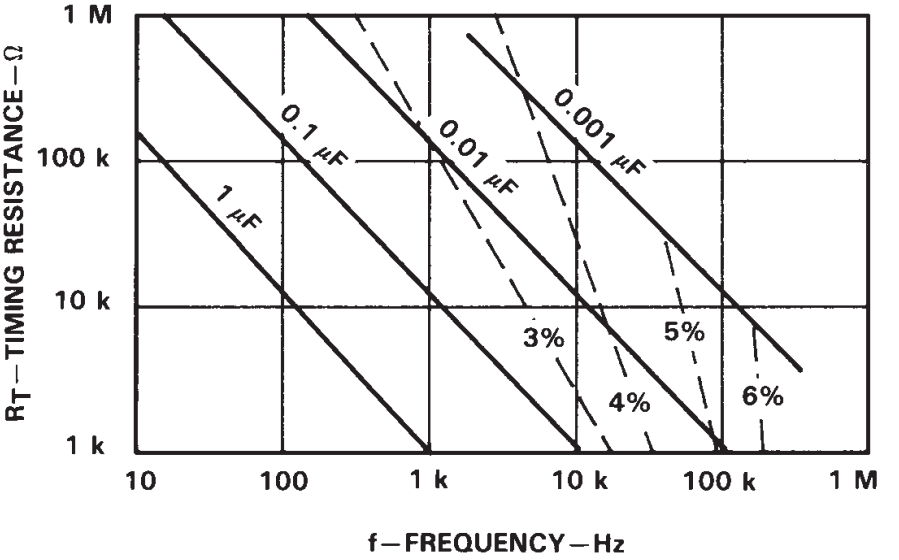


Figure 7. Variation of Dead Time vs R_T/C_T

Dead-Time-Control/PWM Comparator

The functions of the dead-time-control comparator and the PWM comparator are incorporated in a single comparator circuit, as shown in Figure 8. Since the two functions are totally independent, each function is discussed separately.

Comparator

The comparator is biased from the 5-V reference regulator. This provides isolation from the input supply for improved stability. The input of the comparator does not exhibit any hysteresis, so caution should be observed to protect against false triggering near the threshold. The comparator exhibits a response time of 400 ns from either of the control-signal inputs to the output transistors, with only 100-mV overdrive. This assures positive control of the output, within a half cycle, for operation within the recommended 300-kHz range.

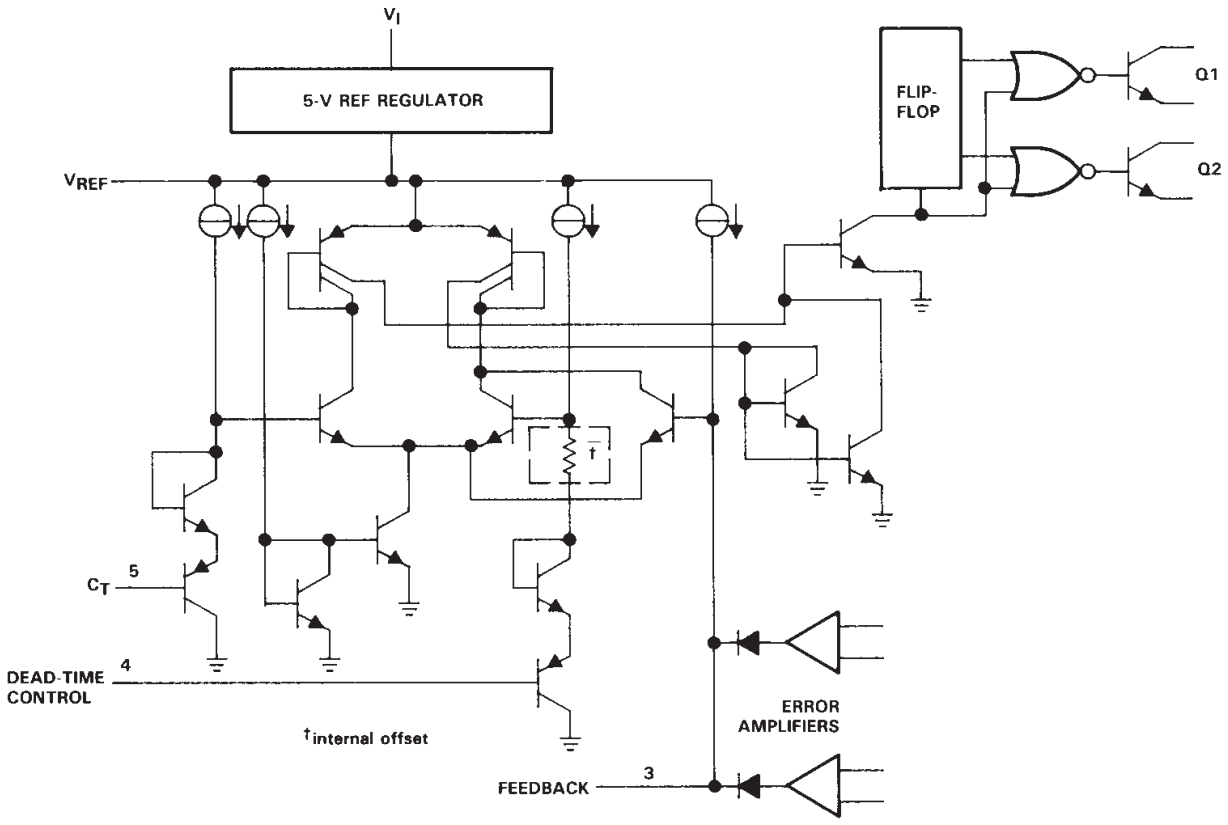


Figure 8. PWM/Dead-Time-Control Comparator

Dead-Time Control

The dead-time-control input provides control of the minimum dead time (off time). The output of the comparator inhibits switching transistors Q1 and Q2 whenever the voltage at its input is greater than the ramp voltage of the oscillator (see Figure 28). An internal offset of 110 mV assures a minimum dead time of $\approx 3\%$ with the dead-time-control input grounded. Additional dead time can be imposed by applying a voltage to the dead-time-control input. This provides a linear control of the dead time from its minimum of 3% to 100% as the input voltage is varied from 0 V to 3.3 V, respectively. With full range control, it allows control of the output from external sources without disrupting the error amplifiers. The dead-time-control input is a relatively high-impedance input ($I_I = < 10\ \mu A$) and should be used where additional control of the output duty cycle is required. The input, however, must be terminated for proper control. An open circuit is an undefined condition.

Pulse-Width Modulation

The comparator also provides modulation control of the output pulse width. For this, the ramp voltage across timing capacitor C_T is compared to the control signal present at the output of the error amplifiers. The timing capacitor input incorporates a series diode that is omitted from the control signal input. This requires the control signal (error amplifier output) to be ≈ 0.7 V greater than the voltage across C_T to inhibit the output logic, and assures maximum duty cycle operation without requiring the control voltage to sink to a true ground potential. The output pulse width varies from 97% of the period to 0 as the voltage present at the error amplifier output varies from 0.5 V to 3.5 V, respectively.

Error Amplifiers

A schematic of the error amplifier circuit is shown in Figure 9. Both high-gain error amplifiers receive their bias from the V_I supply rail. This permits a common-mode input voltage range from -0.3 V to 2 V less than V_I. Both amplifiers behave characteristically of a single-ended single-supply amplifier in that each output is active high only. This allows each amplifier to pull up independently for a decreasing output pulse-width demand. With both outputs ORed together at the inverting input node of the PWM comparator, the amplifier demanding the minimum pulse out dominates. The amplifier outputs are biased low by a current sink to provide maximum pulse width out when both amplifiers are biased off.

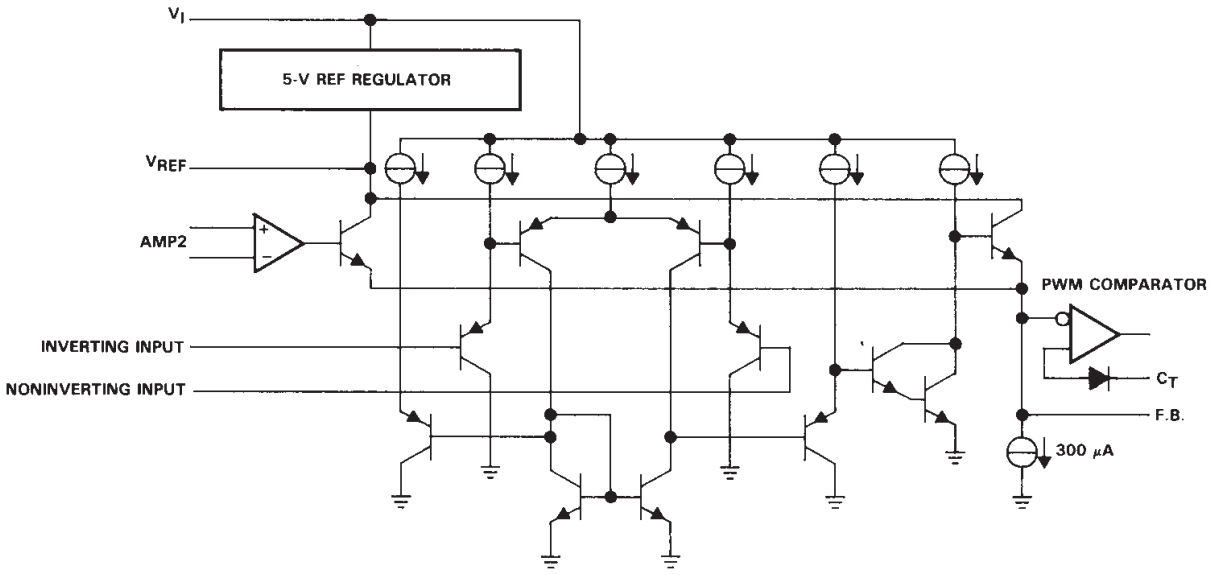


Figure 9. Error Amplifiers

Figure 10 shows the output structure of the amplifiers operating into the 300-μA current sink. Attention must be given to this node for biasing considerations in gain-control and external-control interface circuits. Since the amplifier output is biased low only through a current sink (I_{SINK} = 0.3 mA), bias current required by external circuitry into the feedback terminal must not exceed the capability of the current sink, otherwise, the maximum output pulse width will be limited. Figure 11 illustrates the proper biasing techniques for feedback gain control.

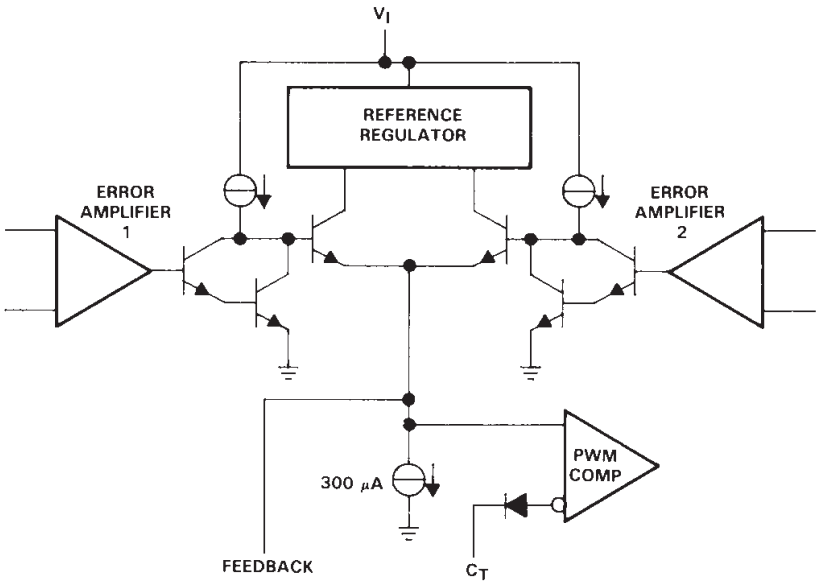


Figure 10. Multiplex Structure of Amplifiers

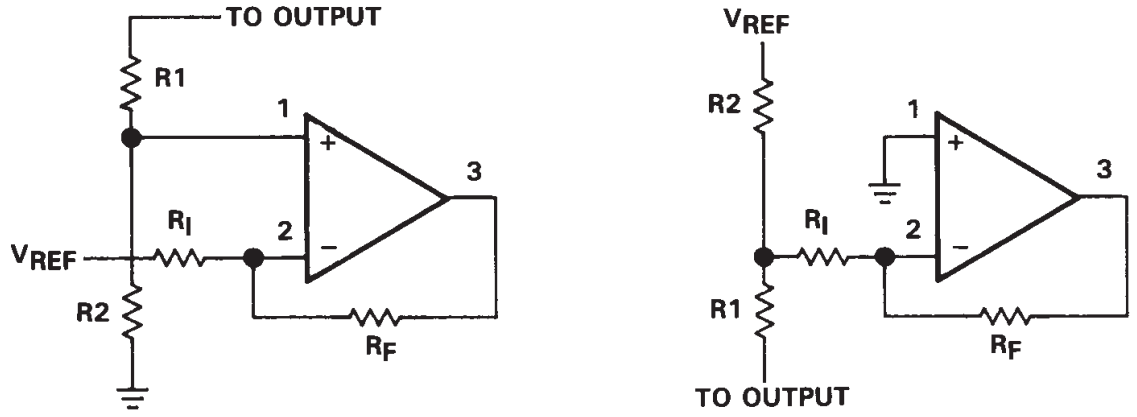


Figure 11. Error-Amplifier-Bias Configurations for Controlled Gain Applications

A plot of amplifier transfer characteristics is shown in Figure 12. This illustrates the linear gain characteristics of the amplifiers over the active input range of the PWM comparator (0.5 V to 3.5 V). This is important for overall circuit stability. The open-loop gain of the amplifiers, for output voltages from 0.5 V to 3.5 V, is 60 dB. A Bode plot of the amplifiers' gain characteristics is shown in Figure 13. Both amplifiers exhibit a response time of approximately 400 ns from their inputs to their outputs. Precautions should be taken to minimize capacitive loading of the amplifiers' outputs. Since they employ active pull-up only, the amplifiers' ability to respond to an increasing load demand can be severely degraded by capacitive loads.

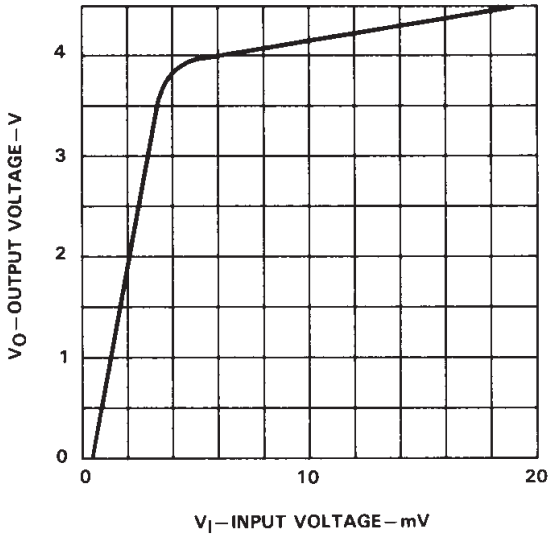
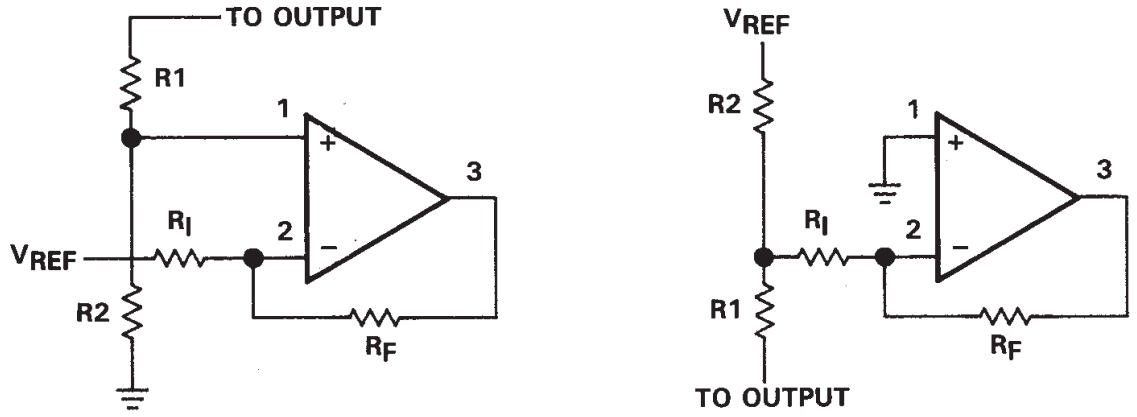


Figure 12. Amplifier Transfer Characteristics



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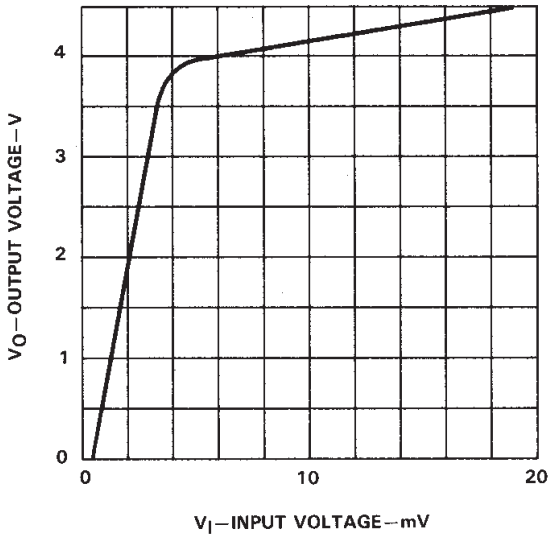


Figure 12. Amplifier Transfer Characteristics

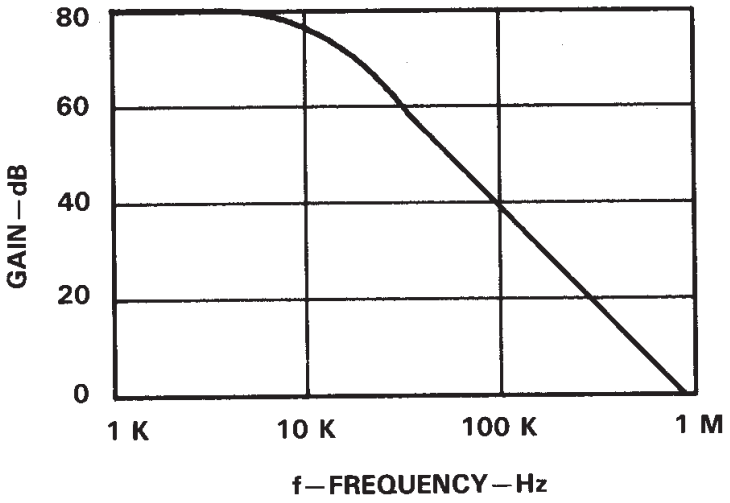


Figure 13. Amplifier Bode Plot

Output-Control Logic

The output-control logic is structured to provide added versatility through external control. Designed for either push-pull or single-ended applications, circuit performance can be optimized by selection of the proper conditions applied to the various control inputs.

Output-Control Input

The output-control input determines whether the output transistors operate in parallel or push-pull fashion. This input is the supply source for the pulse-steering flip-flop, as shown in Figure 14. The output-control input is asynchronous and has direct control over the output, independent of the oscillator or pulse-steering flip-flop. The input condition is intended to be a fixed condition that is defined by the application. For parallel operation, the output-control input must be grounded. This disables the pulse-steering flip-flop and inhibits its outputs. In this mode, the pulses seen at the output of the dead-time-control/PWM comparator are transmitted by both output transistors in parallel. For push-pull operation, the output-control input must be connected to the internal 5-V reference regulator. Under this condition, each of the output transistors is enabled, alternately, by the pulse-steering flip-flop.

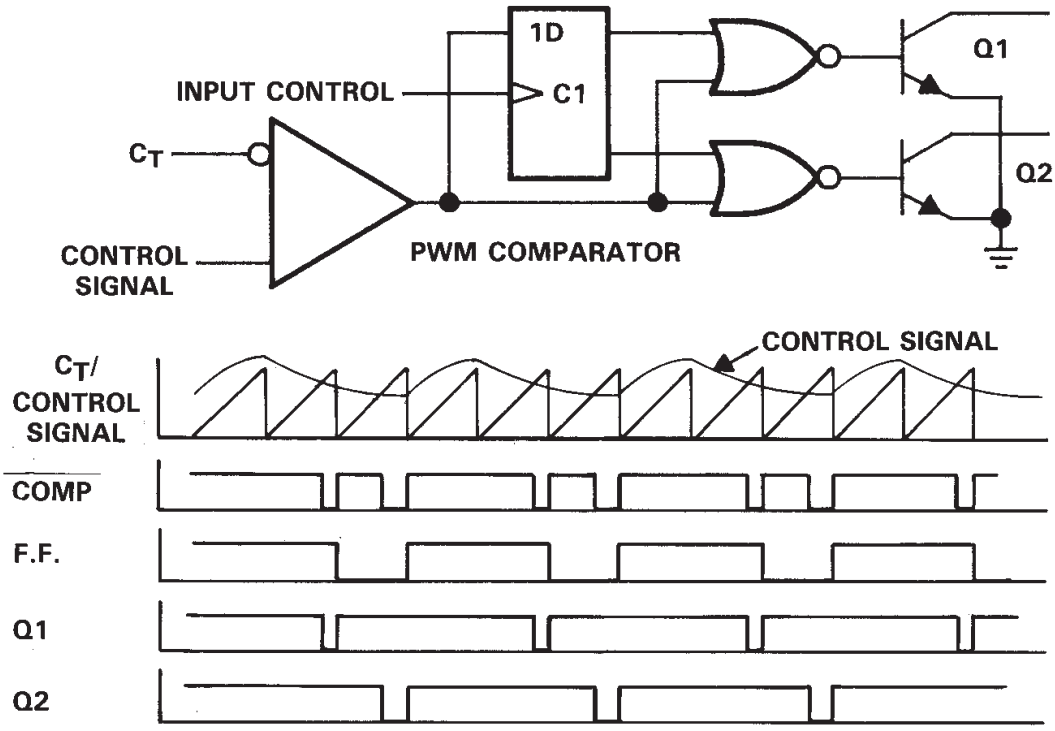


Figure 14. Output-Steering Architecture

Pulse-Steering Flip-Flop

The pulse-steering flip-flop is a positive-edge-triggered D-type flip-flop that changes state synchronously with the rising edge of the comparator output (see Figure 14). The dead time provides blanking during this period to ensure against the possibility of having both outputs on, simultaneously, during the transition of the pulse-steering flip-flop outputs. A schematic of the pulse-steering flip-flop is shown in Figure 15. Since the flip-flop receives its trigger from the output of the comparator, not the oscillator, the output always operates in a push-pull manner. The flip-flop will not change state unless an output pulse occurred in the previous period of the oscillator. This architecture prevents either output from double pulsing, but restricts the application of the control-signal sources to dc feedback signals (for additional detail read 'Pulse-Current Limiting' in this application report).

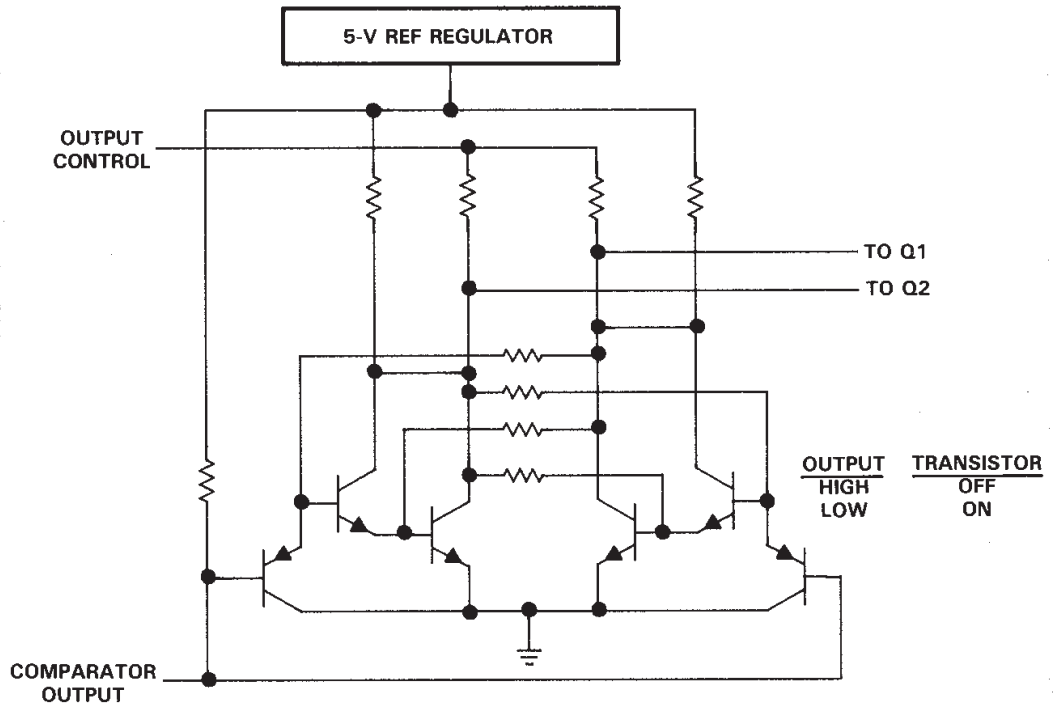


Figure 15. Pulse-Steering Flip-Flop

Output Transistors

There are two output transistors available on the TL494. The output structure is illustrated in Figure 16. Both transistors are configured open collector/open emitter and each is capable of sinking or sourcing up to 200 mA of current. The transistors exhibit a saturation voltage of less than 1.3 V in the common-emitter configuration and less than 2.5 V in the emitter-follower configuration. The outputs are protected against excessive power dissipation to prevent damage but do not employ sufficient current limiting to allow them to be operated as current-source outputs.

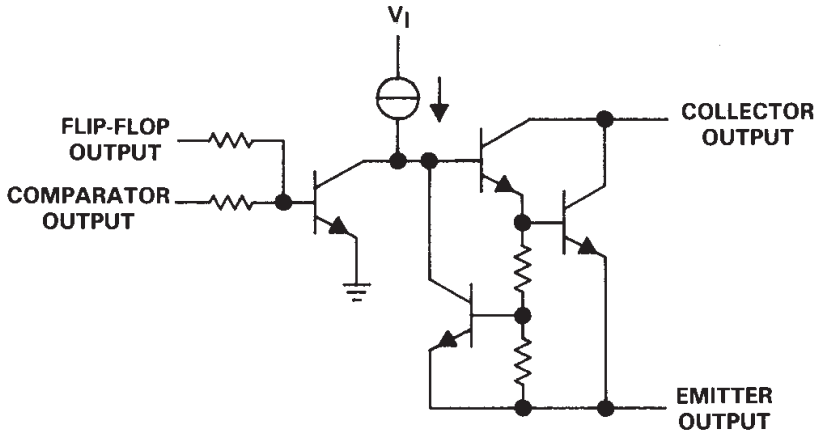


Figure 16. Output Transistor Structure

Applications

Reference Regulator

The internal 5-V reference regulator is designed primarily to provide the internal circuitry with a stable supply rail for varying input voltages. The regulator provides sufficient drive to sustain up to 10 mA of supply current to additional load circuitry. Excessive loading, however, may degrade the performance of the TL494 since the 5-V reference regulator establishes the supply voltage of much of the internal control circuitry.

Current Boosting the 5-V Regulator

Conventional bootstrap techniques for three-terminal regulators, such as the one shown in Figure 17, are *not recommended* for use on the TL494. Referring to Figure 17: Normally, the bootstrap is programmed by resistor R_B so that transistor Q1 turns on as the load current approaches the capability of the regulator. This works quite well where the current in the input (through R_B) is determined by the load current. This is not necessarily the case with the TL494. The input current not only reflects the load current but includes the current drawn by the internal control circuit, which is biased from the reference regulator as well as the input rail itself. As a result, the bias of shunt transistor Q1 is not controlled by the load current drawn by the reference regulator.

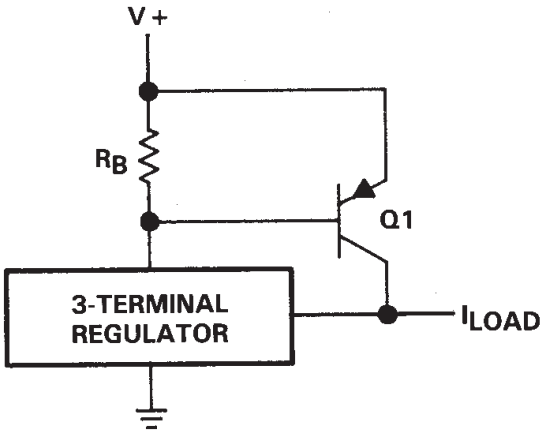


Figure 17. Conventional 3-Terminal Regulator Current-Boost Technique

Figure 18 shows the bootstrapping technique that is preferred for the TL494. This technique provides isolation between any bias-circuit load and the reference regulator output and provides a sufficient amount of supply current without affecting the stability of the internal reference regulator. This technique should be applied for bias circuit drive only since the regulation of the high-current output is solely dependent on the load.

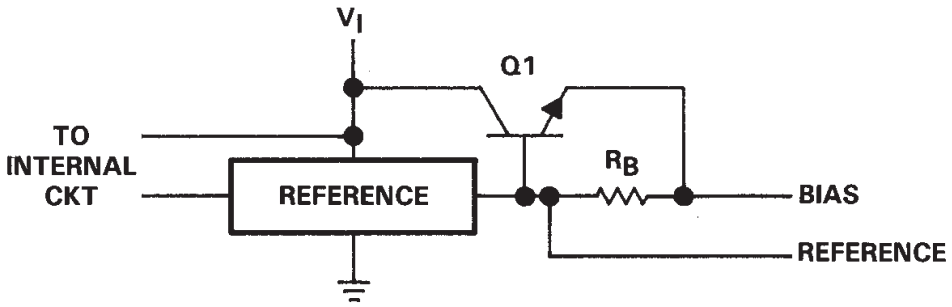


Figure 18. TL494 Reference Regulator Current-Boost Technique

Applications of the Oscillator

The design of the internal oscillator allows a great deal of flexibility in the operation of the TL494 control circuit.

Synchronizing

Synchronizing two or more oscillators in a common system is easily accomplished with the architecture of the TL494 control circuits. Since the internal oscillator is used for no other purpose than creation of the sawtooth waveform on the timing capacitor, the oscillator can be inhibited as long as a compatible sawtooth is provided externally to the timing capacitor terminal. The internal oscillator can be inhibited by terminating the R_T terminal to the reference supply output.

Master/Slave Synchronization

For synchronizing two or more TL494s, establish one device as the master and program its oscillator normally. Disable the oscillators of each slave circuit as explained above and use the sawtooth created by the master for each of the slave circuits, tying all C_T pins together as shown in Figure 19.

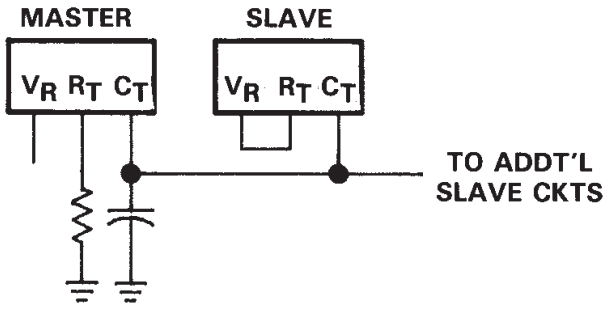


Figure 19. Master/Slave Synchronization

Master Clock Operation

To synchronize the TL494 to an external clock, the internal oscillator can be used as a sawtooth-pulse generator. Program the internal oscillator for a period that is 85% to 95% of the master clock and strobe the internal oscillator through the timing resistor, as shown in Figure 20. Q1 is turned on by a positive pulse applied to its base. This initiates the internal oscillator by grounding R_T and pulls the base of Q2 low. Q1 is latched on through the collector of Q2 and, as a result, the internal oscillator is locked on. As C_T charges, a positive voltage is developed across C1. Q1 forms a clamp on the trigger side of C1. At the completion of the period of the internal oscillator, the timing capacitor is discharged to ground and C1 drives the base of Q1 negative, causing Q1 and Q2 to turn off in turn. With the latch of Q1/Q2 turned off, R_T is open circuited and the internal oscillator is disabled until another trigger pulse is experienced.

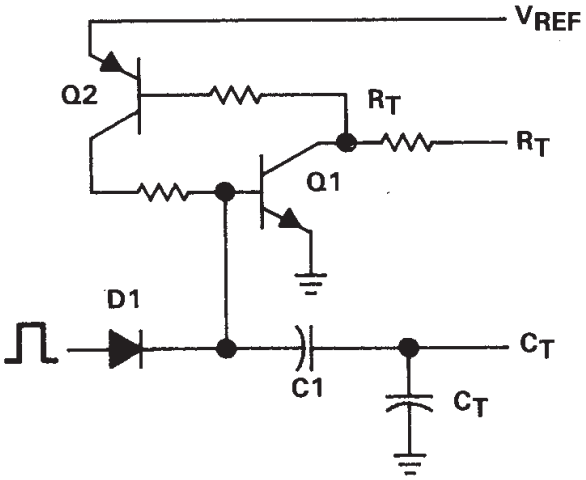


Figure 20. External Clock Synchronization

A common problem when synchronizing the power supply to a system clock occurs during start up. Normally, an additional start-up oscillator is required. Here again, the internal oscillator can be used by modifying the previous circuit slightly, as shown in Figure 21. During power up, when the output voltage is low, Q3 is biased on causing Q1 to stay on and the internal oscillator to behave normally. Once the output voltage has increased sufficiently ($V_O > V_{REF}$ for Figure 21), Q3 is no longer biased on and the Q1/Q2 latch becomes dependent of the trigger signal, as previously discussed.

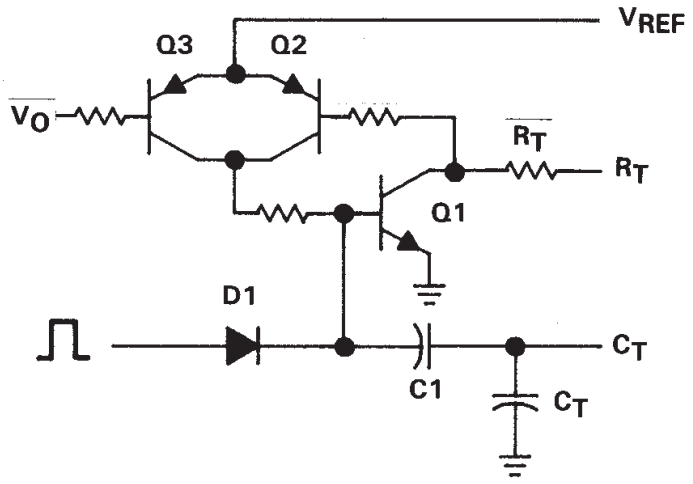


Figure 21. Oscillator Start-Up Circuit

Fail-Safe Operation

With the modulation scheme employed by the TL494 and the structure of the oscillator, the TL494 will inherently turn off if either timing component fails. If timing resistor R_T opens, no current is provided by the oscillator to charge C_T. The addition of a bleeder resistor, as shown in Figure 22, assures the discharge of C_T. With the C_T input at ground, or if C_T short circuits, both outputs are inhibited.

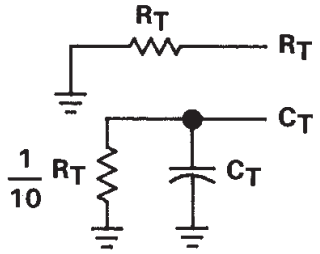


Figure 22. Fail-Safe Protection

Error-Amplifier-Bias Configuration

The design of the TL494 is aligned to employ both amplifiers in a noninverting configuration. Figure 23 illustrates the proper bias circuits for negative and positive output voltages. The gain control circuits, shown previously in Figure 11, can be integrated into the bias circuits.

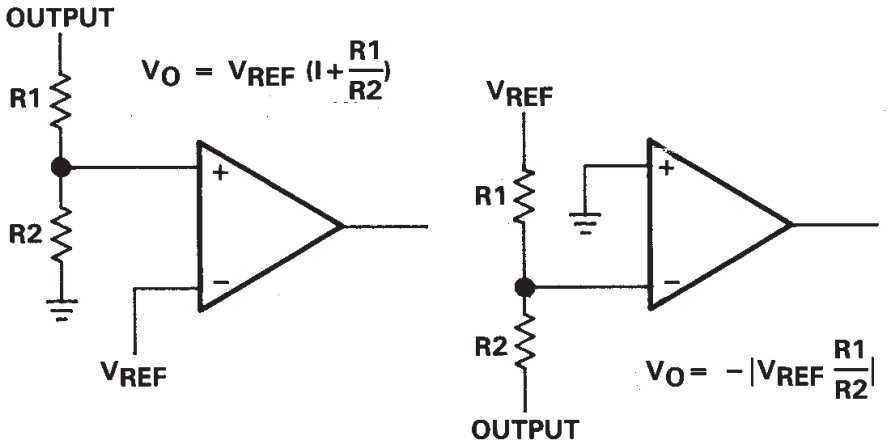


Figure 23. Error-Amplifier-Bias Configurations

Current Limiting

Either amplifier provided on the TL494 can be used for current limiting. Application of either amplifier is limited primarily to load current control. The architecture of the TL494 defines that these amplifiers be used for dc control applications. Both amplifiers have a broad common-mode voltage range that allows direct current sensing at the output voltage rails. Several techniques can be employed for current limiting.

Fold-Back Current Limiting

Figure 24 illustrates the proper bias technique for fold-back current limiting. Initial current limiting occurs when sufficient voltage is developed across R_{CL} to compensate for the base-emitter voltage of Q1 plus the voltage across R1. When current limiting occurs, the output voltage will drop. As the output decays, the voltage across R1 decreases proportionally. This results in less voltage required across R_{CL} to maintain current limiting. The resulting output characteristics are illustrated in Figure 25.

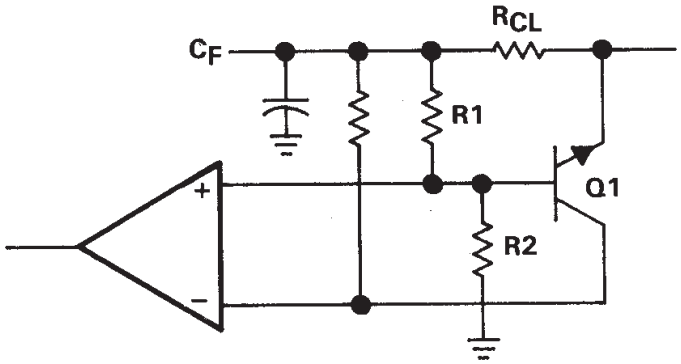
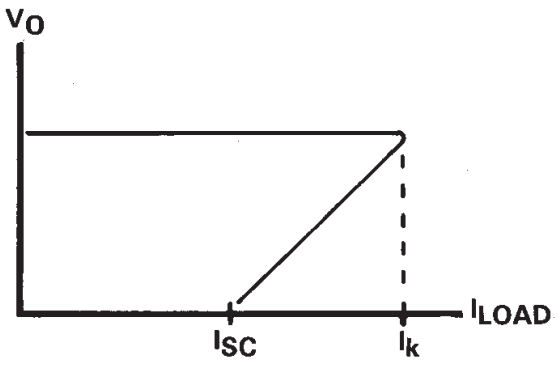


Figure 24. Fold-Back Current Limiting



$$I_K = \frac{V_O\ R1 + V_{BE(Q1)}\ (R1 + R2)}{R_{CL}\ R2}$$

$$I_{SC} = \frac{V_{BE(Q1)}\ (R1 + R2)}{R_{CL}\ R2}$$

Figure 25. Fold-Back Current Characteristics

Pulse-Current Limiting

The internal architecture of the TL494 is not aligned to accommodate direct pulse-current limiting. The problem arises from two factors: 1. The internal amplifiers do not function as a latch, they are intended for analog applications. 2. The pulse-steering flip-flop sees any positive transition of the PWM comparator as a trigger and toggles its outputs prematurely, i.e., prior to the completion of the oscillator period. As a result, a pulsed control voltage occurring during a normal on time not only causes the output transistors to turn off but also toggles the pulse-steering flip-flop. With the outputs off, the excessive current condition decays and the control voltage returns to the quiescent-error-signal level. When the pulse ends, the outputs are again enabled and the residual on-time pulse appears on the opposite output. The resulting waveforms are shown in Figure 26. The major problem here is the lack of dead-time control. A sufficiently narrow pulse may result in both outputs being on concurrently, depending on the delays of the external circuitry. A condition where insufficient dead time exists is a destructive condition. Pulse-current limiting, therefore, is best implemented externally, as shown Figure 27.

In Figure 27, the current in the switching transistors is sensed by R_{CL}. When sufficient current is experienced, the sensing transistor Q1 is forward biased, the base of Q2 is pulled low through Q1, and the dead-time control input is pulled to the 5-V reference. Drive for the base of Q3 is provided through the collector of Q2. Q3 acts as a latch to maintain Q2 in a saturated state when Q1 turns off, as the current decays through R_{CL}. The latch will remain in this state, inhibiting the output transistors, until the oscillator completes its period and discharges C_T to 0 V. When this occurs, the Schottky diode, D1, will forward bias and turn off Q3 and Q2, allowing the dead-time control to return to its programmed voltage.

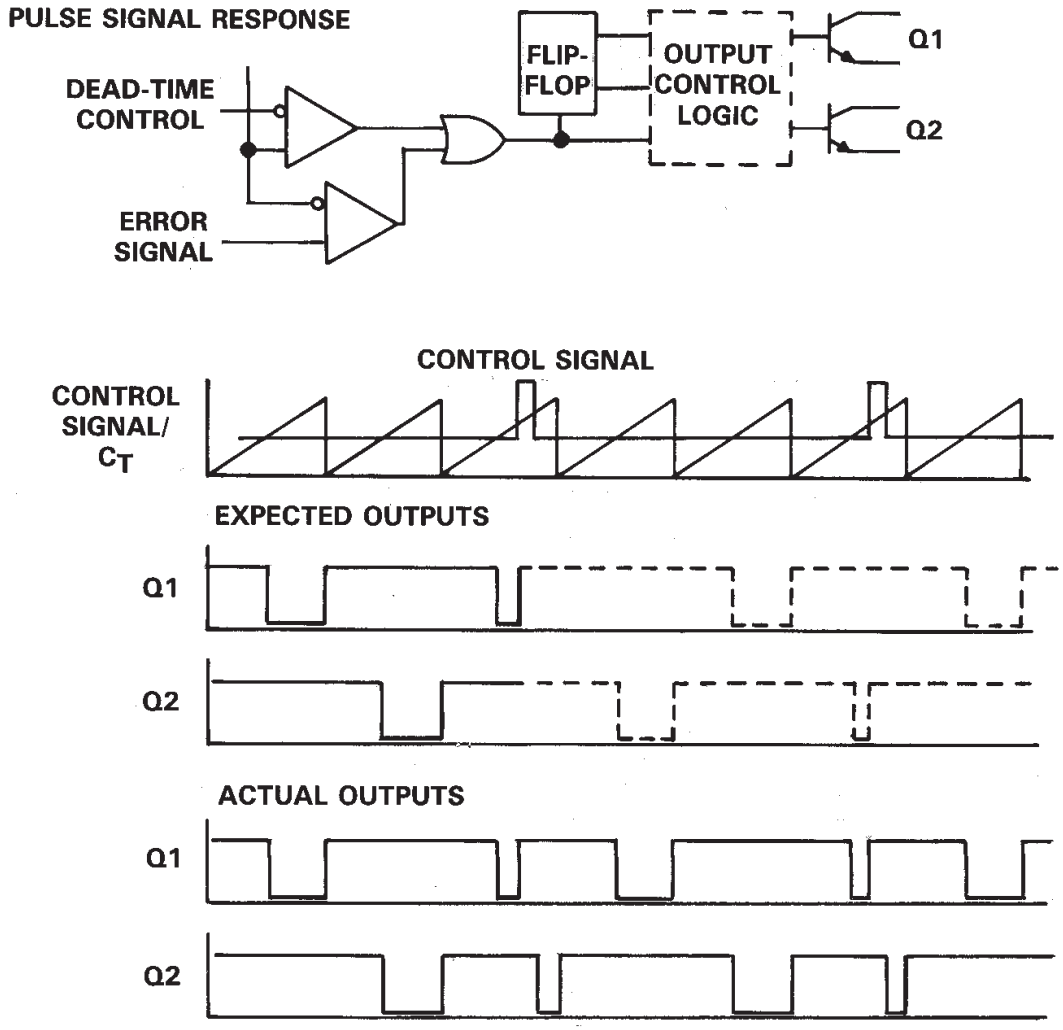


Figure 26. Error Signal Considerations

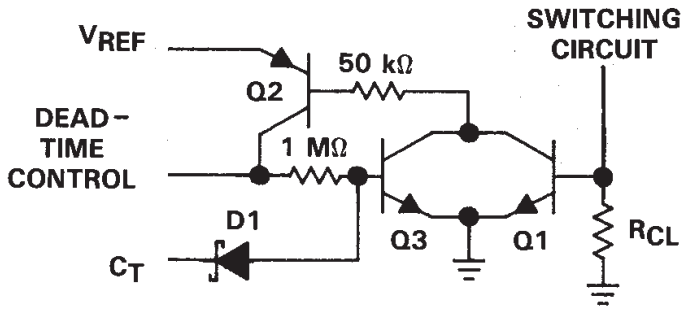


Figure 27. Peak-Current Protection

Applications of the Dead-Time Control

The primary function of the dead-time control is to control the minimum off-time exhibited by the output of the TL494. The dead-time-control input provides control from 5% to 100% dead time, as illustrated in Figure 28.

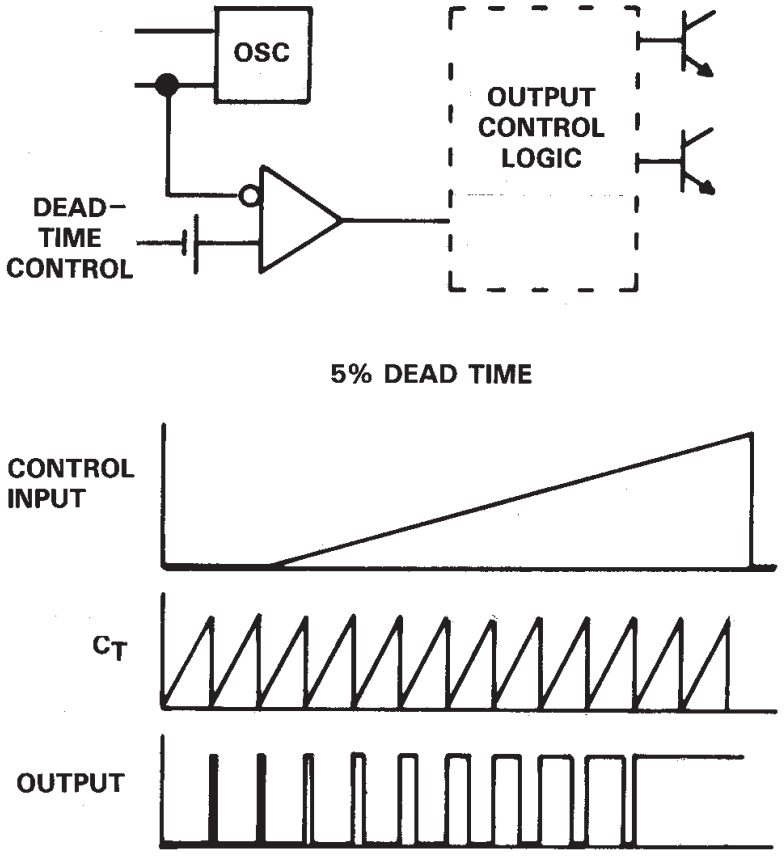


Figure 28. Dead-Time-Control Characteristics

The TL494 can therefore be tailored to the specific power transistor switches that are used to assure that the output transistors never experience a common on-time. The bias circuit for the basic function is shown in Figure 29. The dead-time control can be used for many additional control signals.

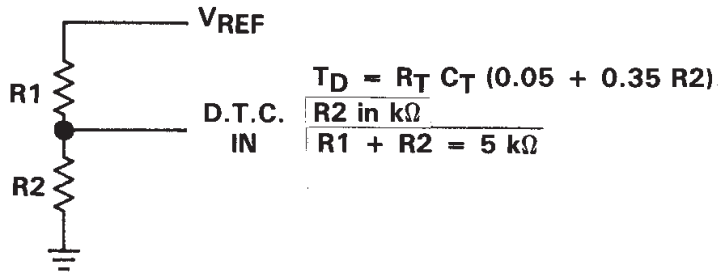


Figure 29. Tailored Dead Time

Soft Start

With the availability of the dead-time control, input implementation of a soft-start circuit is relatively simple; Figure 30 shows one example. Initially, capacitor C_S forces the dead-time-control input to follow the 5-V reference regulator that disables both outputs, i.e., 100% dead time. As the capacitor charges through R_S, the output pulse slowly increases until the control loop takes command. If additional control is to be introduced at this input, a blocking diode should be used to isolate the soft-start circuit. If soft start is desired in conjunction with a tailored dead time, the circuit in Figure 29 can be used with the addition of capacitor C_T across resistor R1.

The use of soft-start protection is recommended. Not only does such circuitry prevent large current surges during power up, it also protects against any false signals which might be created by the control circuit as power is applied.

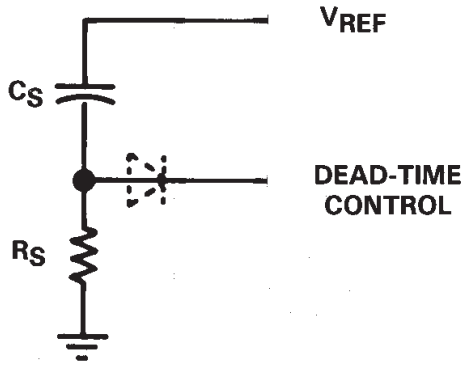


Figure 30. Soft-Start Circuit

Overvoltage Protection

The dead-time control also provides a convenient input for overvoltage protection that may be sensed as an output voltage condition or input protection. Figure 31 employs a TL430 as the sensing element. When the supply rail being monitored increases to the

point that 2.7 V is developed at the driver node of R1 and R2, the TL430 goes into conduction. This forward biases Q1, causing the dead-time control to be pulled up to the reference voltage, disabling the output transistors.

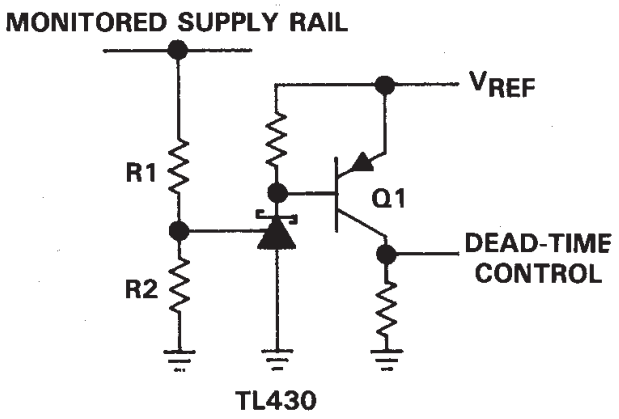


Figure 31. Overvoltage Protection Circuit

Modulation of Turn-Off Transition

Modulation of the output pulse by the TL494 is accomplished by modulating the turn-on transition of the output transistors. The turn-off transition is always concurrent with the falling edge of the oscillator waveform. Figure 32 shows the oscillator output as it is compared to a varying control signal and the resulting output waveforms. If modulation of the turn-off transition is desired, an external negative slope sawtooth, as shown in Figure 33, can be used without degrading the overall performance of the TL494.

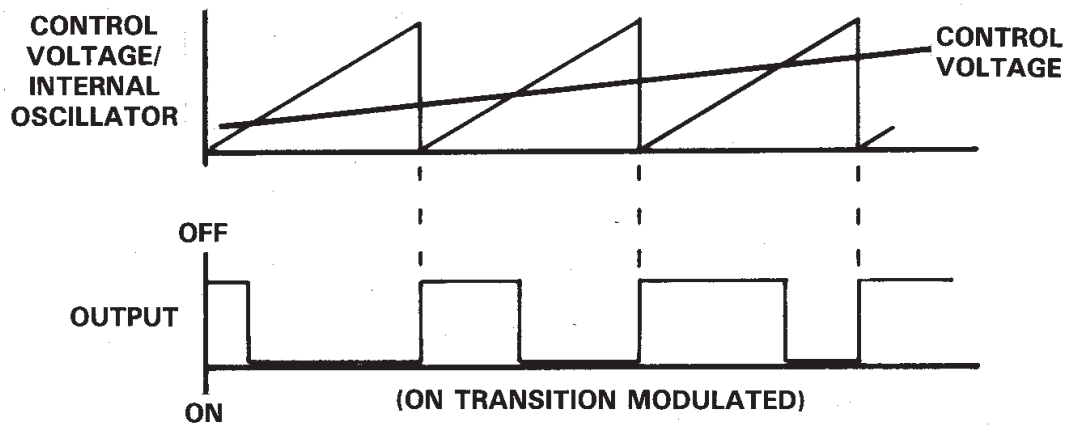


Figure 32. Turn-On Transition

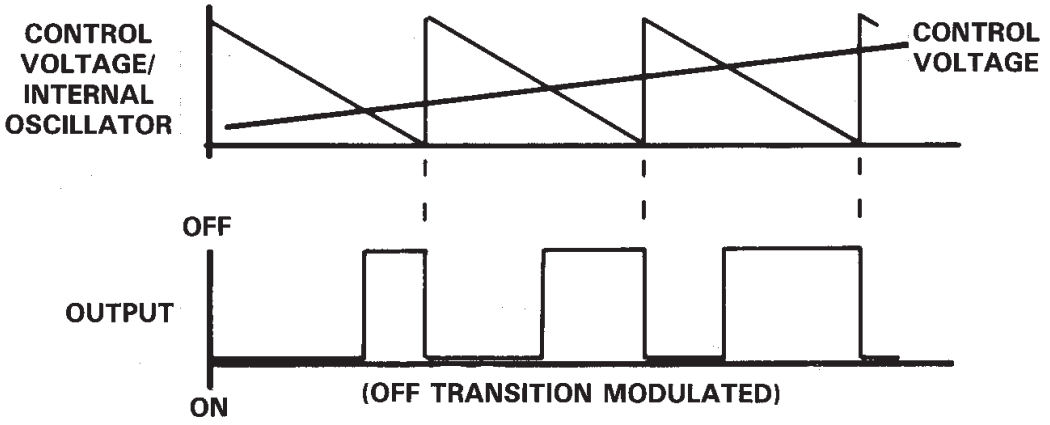


Figure 33. Turn-Off Transition

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