Design Review: 500 Watt, 40W/in^3 Phase Shifted ZVT Power Converter

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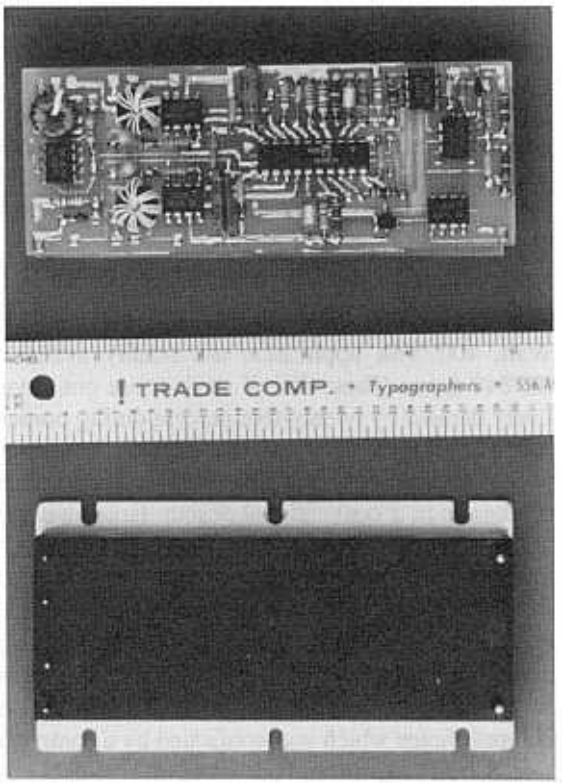
Abstract:

A high power density 500 Watt Phase Shifted power supply design is presented and reviewed. This practical 200 kHz full bridge converter operates from a 385 Volt dc input bus, typical of a Power Factor Correction circuit, and outputs a regulated 48 Volt dc bus for distributed power and Telecommunications applications. Low profile, planar magnetics are featured with full 3750 Vac safety isolation. Over 93% efficiency is achieved. Power density approaching 40 Watts per cubic inch (2.5 W/cm^3) is featured, suitable for load-shared, modular power converter applications. Operating waveforms, printed circuit board layout and measured efficiency of the actual breadboard are also presented.

DESIGN SPECIFICATIONS :

Input Voltage Range :	370 to 410 Vdc
Output Voltage :	48.8 Vdc
Output Current Range :	2 - 10.5 Adc
Output Power Range :	50 - 550 Watts
Efficiency :	93% at full load
Output Ripple :	100 mV pk-pk
Line Regulation :	1%
Load Regulation :	1%
ZVT Power Range :	50% - 100%
Safety Isolation :	3750 Vac
Switching Frequency :	200kHz
Power Density :	40W/in^3 (2.5W/cm^3)
Physical Dimensions (target) :	4.5" x 2.0" x 1.4"



Design Overview and Considerations

The fixed frequency, phase shifted ZVT conversion technique was implemented using the Unitrode UC3875 IC for control. Power to this unit including the IC bias supply is delivered by a universal Ac (85-265 Vac) input ZVT Power Factor Correction module. The phase shifted converter's output voltage feedback path will incorporate an optocoupler to maintain the safety isolation voltage. Wherever possible, standard, commercially available products have been incorporated to simplify development efforts. A goal to achieve a standard 2.375"

by 4.625" footprint, low profile final assembly, suitable for modular power applications has been set. The trend toward half-inch total physical height, while recognized, was not currently possible to achieve for this 500 Watt design.

Topology

A mastery of the basic full bridge topology is needed before initiating the design of this phase shifted derivative. This knowledge allows for some first round approximations regarding the active semiconductor components, passive components and isolation levels required throughout the various sections of the converter. Only items unique to the phase shifted version of the full bridge converter will be covered in significant detail. Based upon conservative design practices, the author has taken the liberty to make a few initial selections which are outlined in the next section.

Semiconductors

The MOSFET switches selected for this 500 Watt, 400 Volt application are readily available IRF840 types. These 500 V devices are conservatively derated by twenty-five percent during normal use. Although the "on" resistance, hence conduction power losses could be lowered by using heftier devices as in a conventional design, large switches are not used in this design. Several factors and tradeoffs have been weighed to arrive at this decision. They are: longer transition times, reduced maximum duty cycle, higher primary circulating currents and potentially lower efficiency. All factors focused on the use of the '840 switches as the optimal choice which was confirmed by a computer spreadsheet program and presented elsewhere in this paper.

The output rectifiers selected are 200 Volt, 16 Amp ultrafast recovery devices to keep power losses low. A series resistor/capacitor (R/C) snubber is used across the transformer secondary windings to minimize voltage excursions. While switching waveforms on the primary are virtually noiseless, the leakage inductance between the secondary windings can lead to ringing and the need to passively snub. The snubber circuit used limits the output rectifier transient voltage overshoot to approximately 150 Volts, leaving an adequate safety margin. The 16 Amp diodes were selected to keep conduction losses reasonable while amply handling the rms current. Recovery time is not critical due to the series ZVT inductance on the primary, but fast recovery assists in keeping losses low.

A series inductor is used on the primary to make the Zero Voltage switching Transitions possible under various output loads. Energy is stored each time power is transferred from the primary to the secondary, and circulated in the primary only during the freewheeling periods. This stored energy is necessary only to accomplish the left leg resonant transitions, and is transparent during the "linear" right leg transition. Additionally, this inductor limits the rate of change in primary current, further softening the power transfer edges.

A dc blocking capacitor is used in series with the primary for this example, primarily because voltage mode operation (duty cycle control) is incorporated. No net voltage was expected to be measured across the capacitor since the applied volt-second products in consecutive switching cycles should be identical. Experiments with voltage feedforward, current mode control and average current mode control were not conducted.

Overcurrent protection has been incorporated by means of a current sense transformer also in series with the primary winding. A standard Pulse Engineering toroidal transformer, model #PE-64977 was used with a single turn primary winding and an isolated 20 turn secondary. This part features low leakage inductance, 1250 VRMS isolation and 20 A peak current sense capability. A full bridge diode array reconstructs the signal referenced to the UC3875 controller "ground" return. A small R/C filter cleans up the waveform which is input to the IC's current sense pin. Resistor R is selected such that a 2.5 V peak signal corresponds to a 15% overload and will trigger the UC3875 current limit protection circuit.

Several low ESR/ESL aluminum electrolytic and ceramic monolithic capacitors are paralleled to form the output filter section. This arrangement yields very low parasitics while providing the correct capacitance value for filtering.

Main Power Stage Design

The focus of this presentation is the design and evaluation of the phase shifted ZVT power stage. A schematic of the main power stage is shown in Figure 2 for clarity. Note that neither external diodes nor capacitors are placed in parallel with the four MOSFET switches. The otherwise parasitic output capacitance (Coss) is fully utilized as the main part of the resonating capacitance, and the MOSFET intrinsic body diode are used to clamp the voltage excursions to the input supply rails. These body diodes are later shunted by the MOSFET on-resistance during the freewheeling portions of the period, lowering the losses.

The design of each of the major components shown in Figure 2 is featured, beginning with the next section covering the main transformer.

Main Transformer Design

The design goal of the main transformer was to minimize leakage inductance while maintaining high repeatability over manufacturing tolerances for this parameter. The power supply industry trends towards high power density and low profile modules steered the decision towards a planar transformer design concept. For the purposes of this presentation, a successful transformer design must be universal and adaptable with minimal design effort. Ideally, the design must meet International Safety Agency isolation requirements and accommodate a wide variety of different output voltages and currents. Accommodating all of these design objectives might be best achieved by going with an existing supplier of planar magnetics as opposed to doing it "from scratch".

Multisource Technology Corporation was contacted to supply the prototype main transformer which was essentially one of their standard products. The specific model selected came from the T-500 series which is rated at 1000 Watts of output power when operated at 250 kHz and 100°C "Hot spot" core temperature. This design example will

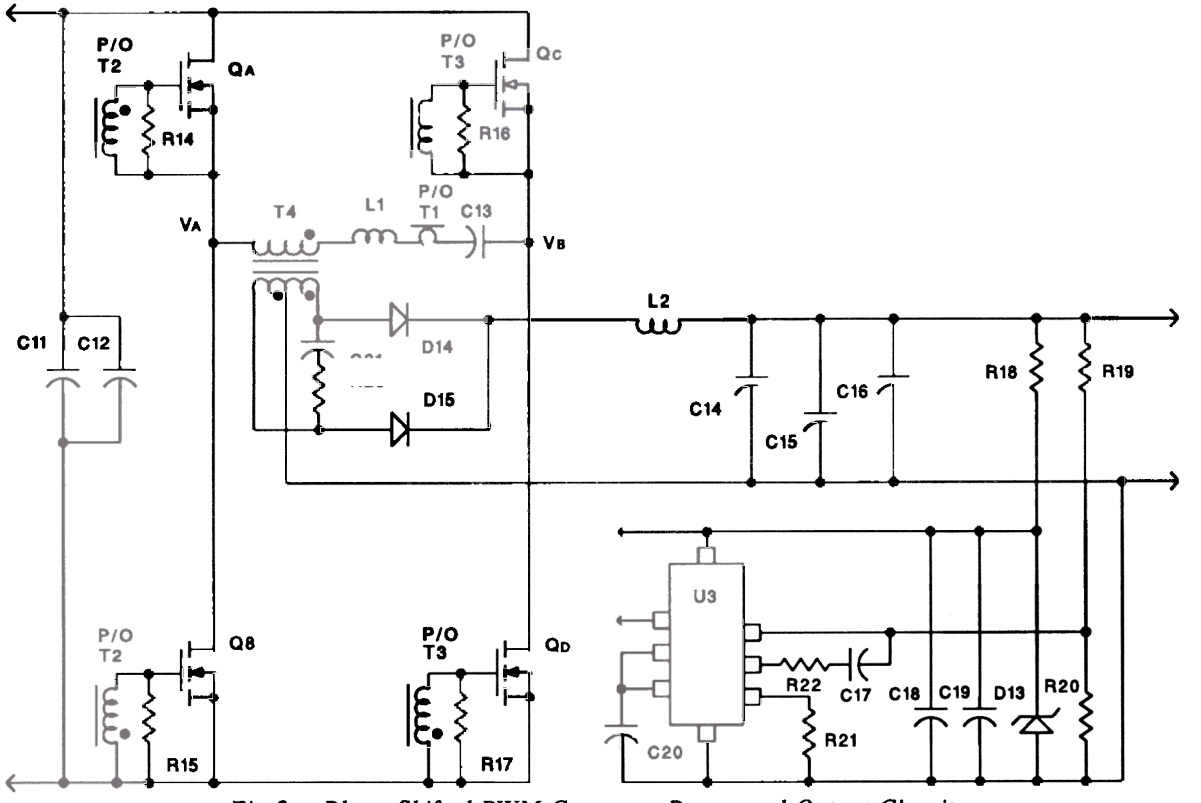


Fig 2. - Phase Shifted PWM Converter Power and Output Circuit

conservatively operate the transformer at one-half rated maximum power, allowing ample room for higher power applications.

Transformer Design Procedure

The starting point of any transformer design should be an estimate of an acceptable temperature rise, and a 25°C total rise is quite typical. Next, the core Area Product can be calculated using the formulas to approximate the core size for a conventional design. However, with planar magnetics, the Area Product (AP) calculation does not equally apply. This is primarily because of two reasons; the reduced core volume (Ve) of these low profile devices in comparison to the full height, standard cores, and the reduced winding area (Aw). The reduced core volume for a given magnetic cross section allows for higher flux density (B) for the same temperature rise. Another option is to use fewer turns for a given temperature rise, which helps to result in a compact, low profile transformer design. For these reasons, it is best to consult and work closely with the transformer manufacturer to "home in" on the best core selection for a planar transformer application.

Fig. 3 - Planar Transformer Characteristics

MTC planar transformers are designed to operate in 120VAC/220VAC environment and to meet UL, CSA, VDE and IEC safety requirements for isolation transformers.

- 4kV Primary-to-Secondary dielectric isolation
- 6-8 mm creepage and clearance distance between primary and secondary windings
- Three ply isolation
- Typical efficiency 98%, low temperature rise
- Low leakage inductance
- Low height 0.53-0.8" (13.5-20 mm)
- High frequency operation 50-1000Hz
- Excellent repeatability, all windings are pretooled
- PWM or resonant topologies
- One to four secondaries
- Efficient cooling
- Low weight from 0.6 oz. (20 g) per 100W
- 200W-1500W power capacity at -40°C ambient temperature

Transformer Selection

The Multisource Technology T-500 series was the most appropriate selection and the specific details will now be highlighted.

Fig 4 - Electrical / Mechanical Specifications

Part Number	T500-AC
Power capacity @ 100-250kHz typ*, @ 90°C operating temp.	800W
Dimensions in inches (LxWxH)	3.3x2.3x0.7
Total weight typ. (oz.)	8 oz. (240 g)
Thermal Impedance:	
"Hot Spot" - Core	.65°C/W
"Hot Spot" - Air	2°C/W
Ae (eff. cross section core area	3.1 cm^2
le (mean magnetic path length)	7.3 cm
Vc (core volume)	24.5 cm^3
A_L typ. ± 30% μH/turns^2	8.5
Max RMS current in one winding	150 A
Typical core losses @ 100-250kHz, 90°C, Bmax=1400-800 G	8W

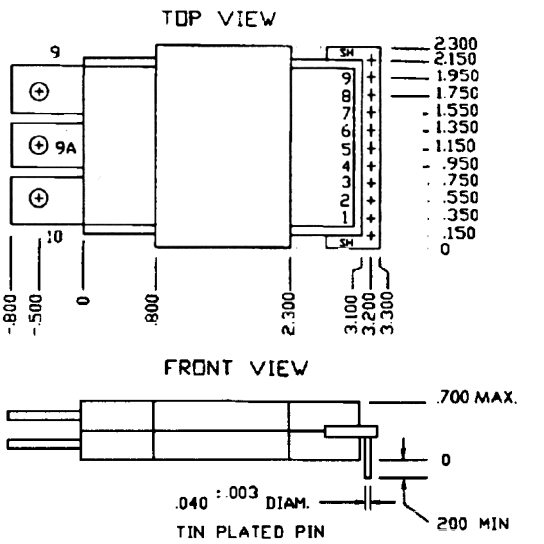


Fig 5. - Mechanical Dimensions

Temperature Rise

A 25°C total core temperature rise will be used to initiate the transformer design. The allowable power dissipation can be determined from the transformer's 10°C/W thermal impedance, RTHETA — hot spot to air.

$$P_{XFMR} = t_{RISE}/R_{THETA} = 25/10 = 2.5 \text{ W}$$

This power loss is the sum of the core and copper individual losses. Usually, losses are apportioned equally between core and copper, a good design practice which will also be used for this design.

$$P_{CORE} = P_{COPPER} = 12.5/10 = 1.25 \text{ W each}$$

Transformer Operating Frequency

Switching frequencies as high as 300 to 600 kHz have been tried with acceptable results, and are worth further consideration. However, in this application, 200 kHz has been selected as a reasonable and practical compromise between minimizing core losses and reduced transformer and output inductor volume. In the full bridge topology, the core flux swings at half the switching frequency. Thus, the transformer operating frequency in this design is 100 kHz.

Flux Density

The operating flux density (B) is determined from the transformer operating frequency, allowable core loss (Pcore), and the core set volume (Ve). First, the core loss in mW/cm^3 is calculated.

$$P_{LOSS} = 1.25\text{W} / 24.2\text{cm}^3 = 52 \text{ mW/cm}^3$$

Next, the manufacturer's "Core Loss vs. Flux Density" curve for the core material is used to determine the correct peak flux density. This example uses Magnetics Inc. "P" type material whose core loss curves are shown in Figure 6. Note that this curve is obtained using a much different core shape than that of the planar design, so some measured verification may be required.

The exact flux density is found where the diagonal 100 kHz frequency line intersects with 52mW/cm^3 core loss on the vertical axis. Dropping down from this point to the horizontal Flux Density

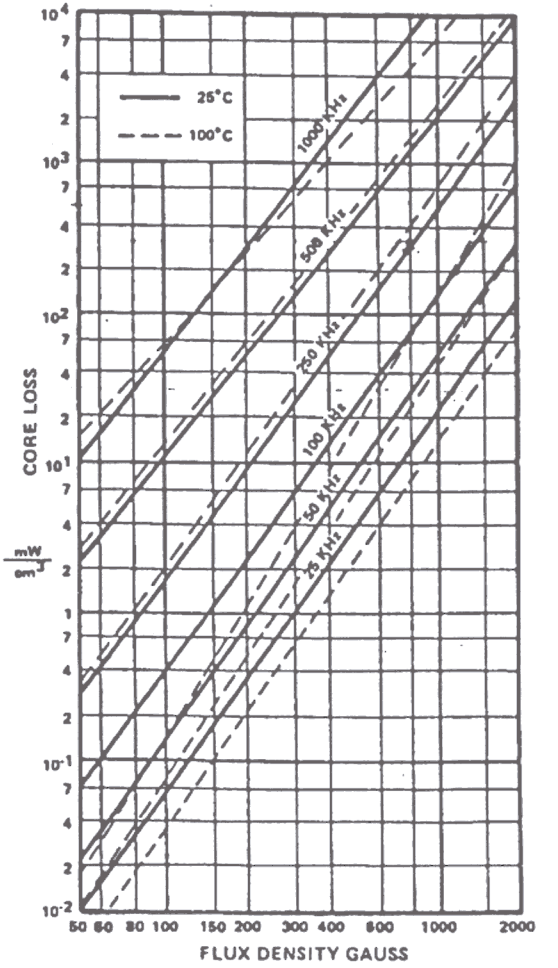


Fig 6. - Magnetics Inc "P" Material

axis, a peak flux density of 0.065 Tesla (650 Gauss) is obtained. Note that the total peak to peak flux excursion, ΔB, is TWICE the peak flux density (which is given in most core manufacturers core loss curves). Thus, in this application, ΔB is 0.13 Tesla or 1300 Gauss.

Primary Number of Turns

The required number of primary turns is calculated by solving Faraday's Law using the known parameters.

Faraday's Law:

$$N_{PRI} = V_{IN} \cdot t_{ON} \cdot 10^4 / (Ae \cdot \Delta B)$$

In this particular design:

V_{IN} = 385 *Vdc(min)*
t_{ON} = 4µsec
f_{XFMR} = 100kHz
Ae = 3.1 cm^2
ΔB = .13 Tesla

Therefore :

$$N_{PRI} = 385 \cdot 4 \cdot 10^{-6} \cdot 10^4 / (3.10cm^2 \cdot .13T)$$

N_{PRI} = 38 turns (estimated)

Turns Ratio Calculation

The number of turns for each secondary winding is calculated knowing the available volt-second product on the primary winding and the desired output voltage. In this application, the output rectifier voltage is a small percentage of the 48 V output level and can be ignored in the turns ratio calculation.

The exact transformer primary to secondary turns ratio (N) is derived from the following relationships used for any Buck derived converter:

$$V_{OUT} = V_{IN(MIN)} \cdot D_{MAX} / (N_{PRI}/N_{SEC})$$

where D_{MAX} is the maximum obtainable duty cycle of the converter which occurs at the minimum input voltage, $V_{IN(MIN)}$.

Substituting the turns ratio $N = N_{PRI}/N_{SEC}$ into the above equation and solving;

$$N = V_{IN(MIN)} \cdot D_{MAX} / V_{OUT}$$

$$N = (385 * 0.80) / 48.5(typ) = 6.3 \text{ (estimate)}$$

The secondary number of turns is straightforward:

$$N_{SEC} = N_{PRI}/N = 38/6.3 = 6.0 \text{ (estimate)}$$

Planar Transformer Design Considerations

Design considerations are much different for planar magnetics as opposed to conventionally wound transformers due to physical limitations. These are: total number of turns, turns ratio, and current per winding. In all fairness to the planar construction technique, designers are faced with some of the same difficulties with traditionally wound units. Integral numbers of secondary turns (without resorting to complex flux shifting techniques) still poses problems with multiple outputs. Tradeoffs and considerations will be highlighted in the next section.

Planar Construction: Planar transformers are formed by series and/or parallel connections of individual planar windings. These windings are generally made from etched printed circuit board material for multiple turns per plane, or from a stamped copper "lead frame" for a single, planar turn. Each of these planes is isolated from adjacent planes by some form of insulation material. Typically, the stamped copper turns are used for the higher current applications such as low voltage outputs. The multiple turn PC boards are commonly connected in series to form higher voltage and lower current windings like the transformer's primary. High voltage, VDE approved isolation between primary and secondary is achieved with a patented bobbin[2] structure as shown below.

Final Transformer Details The final transformer design was an iterative process as with almost all transformer designs. The total number of planar boards able to fit within the structure dictated several details of the design, including turns ratio and number of primary turns. A 6 turn secondary (Ns = 6 T) was selected as optimal for this 48 V output, and several PC boards were connected in parallel to handle the output current. The "winding" room available for the primary side and a rough estimate of the final primary current determined the exact final number of primary turns. A 32 turn primary (Np = 32) would fit, while amply handling the current. This resulted in an overall transformer turns ratio, N, of 32:6, or 5.33:1. While this might be slightly less than ideal, it will actually be necessary once the resonant inductor, needed to facilitate Zero Voltage Transitions, is added to the circuit. As will be later described, this inductance adds a slight penalty in the effective maximum duty cycle, thus requiring the turns ratio to be reduced. Np = 32, Ns = 6, N = 5.33:1.

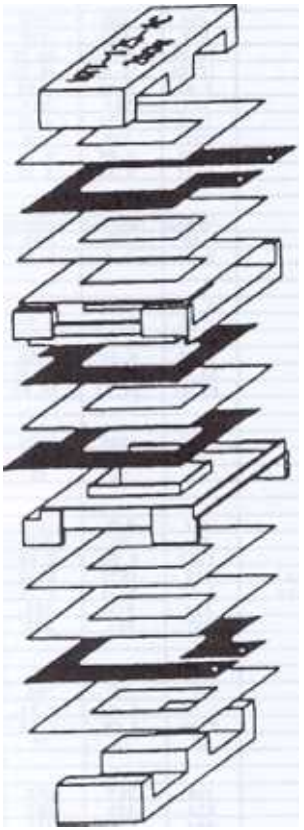


Fig 7. - Planar Transformer Construction

Lossless Switching Range

One goal of this design is to accomplish Zero Voltage Transitions when the output load is above fifty percent of the full power rating. When the load drops below this amount, then ZVT is no longer obtained for the resonant left leg switch pair A and B. Switches C and D will undergo lossless switching at loads below 50% because they are propelled by the constant output current and energy stored in the output choke. At some point, however, these switches will also encounter switching loss at very light loads, and this power level is easily calculated. So, while this design features fully lossless switching above ≈50% of full load, it will have losses below that level. This was a reasonable design compromise, and the exact switch-over point can be adjusted by changing the resonant inductor value.

Resonant Inductor

This design incorporates an inductor in series with the transformer primary to facilitate the lossless transitions within the desired delay times. Further details and tradeoffs of accomplishing this objective are available in another topic in this Seminar Manual[1]. This inductor will also program the power stage dI/dt which softens the switching transitions and noise even further. The influence this will have on the effective duty cycle must be considered since this erodes the full power transfer portion of the conversion cycle. Also, a high value of series inductance could ultimately effect the transformer turns ratio. This case could be considered as extreme, but is possible with designs attempting to ZVT down to very light loads.

Power loss in the core was a concern in this 200kHz inductor design due to the high voltage primary. The few turns required to get the low inductance value corresponds to a higher core flux density during each switching transition. Ideally, this suggests the use of low loss, gapped ferrite material or possibly low permeability magnetic material. Low profile is preferred to keep with the design guidelines, so total height shouldn't exceed the main transformer's 0.62 inch profile.

Transition Details

A spreadsheet program was developed to analyze the ZVT transition effects at various output loads, MOSFET choices and resonant inductor values. (See Figure 8.) Effects on both the "linear" right leg and resonant left leg transitions were tabulated along with the critical minimum load current required to facilitate lossless switching within the programmed delay time.

It was determined that a 50 µH series inductance was needed to achieve the lossless switching objective above half load within the 250 nsec maximum delay time. Note that this only applies to the left leg resonant transition and not to the "linear" right leg, separately programmed for a briefer (150ns) delay time. The 50 µH inductor in conjunction with the IRF840 MOSFET capacitance, transformer capacitance, leakage inductance and 5.33:1 turns ratio facilitates ZVT down to 60% of full load, or 6.3 Amps of output current. More inductance can

be added, but this value works out reasonably well for the purpose of this design example. The required energy storage is 156 µJ at 2.5 A maximum, indicating a fairly small device can be used.

Note that this series inductance limits the primary di/dt and therefore erodes the effective maximum duty cycle. Power transfer takes place during a smaller portion of the total switching cycle, which could require another iteration on the main transformer turns ratio. This design procedure commenced with an initial estimate of 85% and the 5.33:1 turns ratio. The spreadsheet results indicate that the realizable maximum duty cycle is about 86%, and therefore will work fine. Had this not been the case, the easiest way to resolve the situation would be to lower the switching frequency enough to yield the required maximum duty cycle. Another possibility is to take a turn or so off of the primary and recalculate the transition analysis. Adding series inductance to facilitate the transitions seems to be the preferred route with moderate frequency converter designs. High frequency applications, those above 250 kHz may need to resort to other techniques to accomplish ZVT.

PHASE SHIFT ZVT CONVERTER DESIGN	TEST 1	TEST 2	TEST 3
INPUT SUPPLY VOLTAGE, VIN, (V)	400	400	400
OUTPUT POWER, POUT, (WATTS)	512	512	512
OUTPUT VOLTAGE, VOUT, (V)	48.80	48.80	48.80
OUTPUT CURRENT, I OUT, (A)	10.50	10.50	10.50
EFFICIENCY (estimate)	0.93	0.93	0.93
INPUT POWER (estimate) [PIN] (W)	551	551	551
PRIMARY CURRENT [IPRI] estimate (A)	1.62	1.62	1.62
SWITCHING FREQUENCY (kHz)	200	150	100
MAXIMUM DUTY CYCLE (estimate)	0.85	0.85	0.85
TRANSFORMER TURNS RATIO [N = NP/NS]	5.33	5.33	5.33
POWER SWITCHES			
MOSFET TYPE	IRF840	IRFP450	IRFP460
MOSFET OUTPUT CAPACITANCE, Coss, (pF)	160	350	480
MOSFET Rds(on) @ 25 C (ohms)	0.80	0.4	0.27
POWER LOSS ESTIMATES			
MOSFET TOTAL CONDUCTION LOSSES (W)	8.91	4.46	3.01
OUTPUT RECTIFIERS P(LOSS) (W)	9.65	9.65	9.65
MAGNETIC CORE LOSSES (W)	8.00	8.00	8.00
COPPER LOSSES (W)	6.50	6.50	6.50
TOTAL POWER LOSS (W)	33.06	28.61	27.16
FULL LOAD EFFICIENCY (%)	93.94	94.71	94.97
PRIMARY ZVT RESONANT TANK			
XFMR MAGNETIZING INDUCTANCE (uH)	7600	7600	7600
XFMR LEAKAGE INDUCTANCE (uH)	10	10	10
XFMR PRIMARY CAPACITANCE (pF)	15	15	15
RESONANT TANK			
RESONANT CAPACITANCE, Cr, (pF)	442	948	1295
RESONANT INDUCTANCE Lr (uH) * series	50	75	100
RESONANT TANK FREQUENCY (mHz)	1.07	0.60	0.44
RESONANT TANK CIRCUIT PERIOD, T(res), (ns)	933	1675	2260
RESONANT TANK FREQUENCY, wR, (mHz) radians	6.73	3.75	2.78
TANK TRANSITION TIME, t(res), (us)	233	419	565
RESONANT TANK IMPEDANCE, ZR, (ohms)	336	281	278
TANK ENERGY			
CAPACITIVE ENERGY REQUIRED, W(Cr), (uC)	35	76	104
INDUCTIVE ENERGY AVAILABLE, W(Lr), (uC)	35	76	104
CRITICAL PRIMARY CURRENT FOR ZVT (A)	1.19	1.42	1.44
CRITICAL SECONDARY CURRENT FOR ZVT (A)	6.34	7.58	7.67
MINIMUM LOAD FOR ZVT (% OF FULL LOAD)	60	72	73
TRANSITION TIME SUMMARY			
RIGHT LEG TRANSITION TIME, C/D (nsec)	149	267	360
LEFT LEG TRANSITION TIME, A/B nsec)	233	419	565
PRIMARY di/dt SLEW TIME (ns)	297	533	720
TOTAL TRANSITION TIMES, t(tran), (nsec)	679	1219	1645
POWER TRANSFER TIME, (1- t(tran)), (us)	4.32	5.45	8.36
MAXIMUM DUTY CYCLE (ACTUAL%)	86.42	81.72	83.55

Fig 8. - Transition Time Spreadsheet Results

Transition Comparison

The spreadsheet analysis contains a wealth of detailed information about the transitions. Comparisons to using larger MOSFETs, different turns ratios, and resonant inductor values can be made. The three columns on the spreadsheet shown indicate trial designs using the same basic converter and transformer designs, but different size MOSFETs. Reviewing the columns, values are calculated for an IRF840 type (size 4) FET first, and IRFP450 (size 5) FET next, and finally for an IRFP460 (size 6) MOSFET.

The purpose of these examples is to be able to clearly distinguish the repercussions of using a large FET with this phase shifted technique to reduce conduction losses. The penalties paid for the slight increase in overall efficiency are numerous. The larger output capacitance of the heftier size five and six switches requires more primary current to accomplish the transitions within the allotted transition times. A larger series resonant inductor can be added to store the additional energy, but this will impact the primary current slew rate. This, in turn, erodes the maximum effective duty cycle which

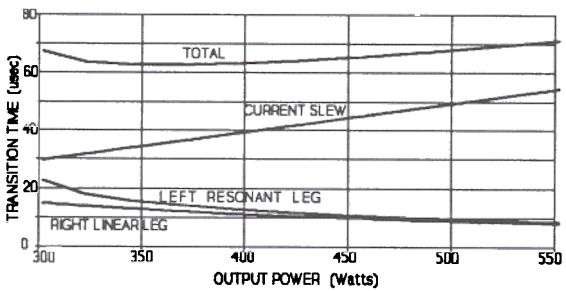


Fig 9. - Transition Times vs. Load

suggests a lower switching frequency, and possibly an increase in the transformer turns ratio. There is nothing wrong with taking this tack, provided that the overall power density is not impacted. In fact, this may be a better approach for very high power applications. The comparison is presented to demonstrate the subtle and obvious tradeoffs which occur during the design process of the phase shifted converter. Numerous other parameters, for example switching frequency, can be quickly evaluated and compared using the spreadsheet format.

Spreadsheet formulae are given in Appendix II

Gate Drive Circuit Design

The destiny of "old" bipolar transistor power supply design was typically determined by the base drive circuitry. While today's families of power MOSFETs have greatly simplified this section of the design, the challenge of designing an optimal gate drive circuit should not be underestimated. High frequency drives allow no provision for leakage inductance. The gate transitions must be sharp, ringing and overshoot must be minimal.

Standard, off-the-shelf PE-64972 "500kHz" gate drive transformers from Pulse Engineering were used in the first round of high frequency experiments, but not the final prototype. As the converter's switching frequency was lowered from 600 kHz to the final 200 kHz to accommodate core losses, the gate drive transformer maximum volt-second product was exceeded. Nevertheless, they performed very well above 350 kHz and delivered clean drive signals to the gates. Design details of the transformers fabricated for this example are included.

Compared to conventional switching techniques, phase shifting offers a few significant benefits and reduces the gate drive complexity. First, all switches are continually running at approximately fifty percent (50%) duty cycle, all of the time. Also, the upper and lower switches within one leg are always driven out of phase, at the same 50/50 duty cycle. High side switches do not experience the wide volt-second product variations as in conventional PWM designs with variable duty cycles. Therefore, the upper switches have greatly simplified transformer coupled gate drives and will not require the back-to-back zener diodes or complex clamp circuits typical of a traditional full bridge. The 50/50 percent duty cycle drive makes it easy to add another winding on the core and obtain the lower switch gate drive with minimal effort. Adding this winding is a small expense, but worth consideration due to potential power to signal ground loops and voltage drops commonly found in a high power converter.

Another benefit of this phase shifted control technique is the lack of "Miller" effects during the zero voltage transitions. The typical gate voltage plateau at around 8 V is gone since the switch is already positioned with zero voltage across it, drain to source. The associated ringing of the gate voltage when confronting the "Miller" effects is likewise gone. Power loss in the switch due to the gate ringing is also eliminated. Finally, the IC driving the four gates is spared from a good percentage of the total gate charge (Qg), so IC power dissipation is even reduced. This is only true for the ZVT portion of operation above 60% of full load, and is not applicable at light loads when the converter is operating in a lossier switching mode.

Only the two upper switches of this converter need high voltage (500 V) isolation from the UC3875 driver outputs. The two lower side FETs can be driven from the IC without galvanic isolation. However, the decision to transformer couple all four gate drive signals was made based on several factors. First, ideal magnetic coupling was needed to insure that the exact programmed delay times were delivered intact across the isolation barrier. This suggested using three windings on a toriodal core wound tri-filar for best results. Keeping these as identical as possible required using the same insulated wire for all three windings, so each was electrically isolated from the core, and each other. Two transformers are used, each with three tri-filar insulated windings.

The toroid core selected for the gate drive application is a Magnetics Incorporated 41206-TC, made using the company's low loss "P" ferrite material. Physical dimensions are shown in the accompanying Figure. Insulated, small diameter wire can be used due to the net low dc currents involved. This prototype incorporated standard

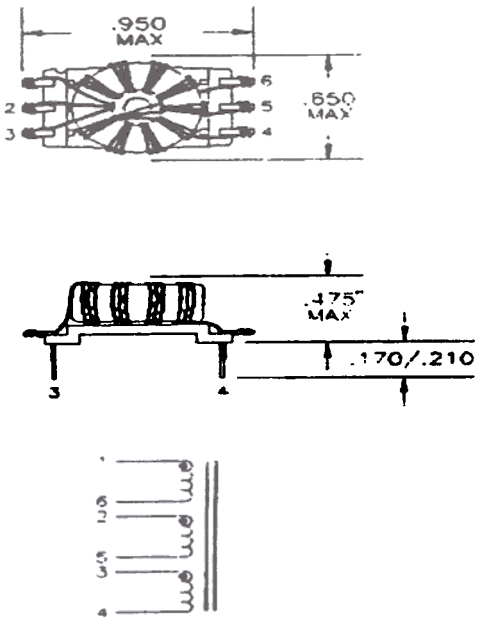


Fig 10. - Gate Drive Transformer

"wire-wrap" wire, AWG#30. KYNAR insulation provides 1000 V isolation for each winding, more than adequate for even high input voltage IGBT designs. Different color sleeving can be used for each of the three windings to simplify fabrication. The three wires can be twisted together first, then wound for possibly better magnetic coupling, although this was not done on the prototype. Twelve turns will be needed for each winding to keep core losses within reason and voltage droop to a minimum. Later in the development cycle, Coilcraft (see SUPPLIER LIST) was contacted to discuss making this transformer a standard product. As a result, a similar 10:10:10 turn gate drive transformer is being made available from Coilcraft as their part number Q3903-A. It features 500 Vrms isolation (minimum) for each winding and demonstrates better magnetic coupling than the author's handmade prototypes.

Each gate transformer is driven in a bipolar technique and is connected between the two applicable UC3875 high current outputs. The 12 V supply rail and a 10 Ohm series resistor limits the peak current to approximately 1 Amp. A series dc

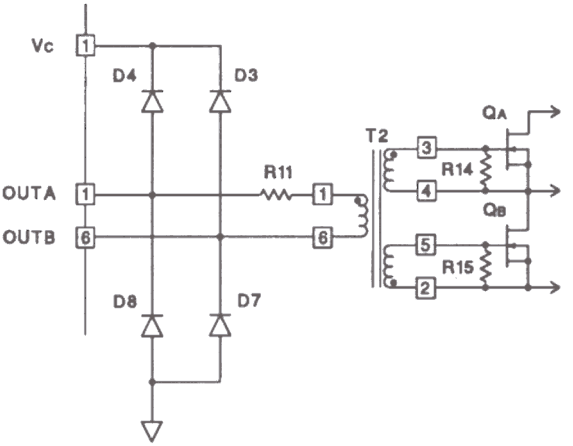


Fig 11. - Gate Drive Circuit

blocking capacitor accommodates any volt-second mismatching of the drivers. Eight Schottky clamp diodes are required, two per UC3875 output, to protect the IC against any voltage excursions below ground or above the collector supply voltage, Vc. These diodes MUST be Schottky types in order to effectively clamp, and a 2 A peak minimum rating is recommended. Details are shown in Figure 11.

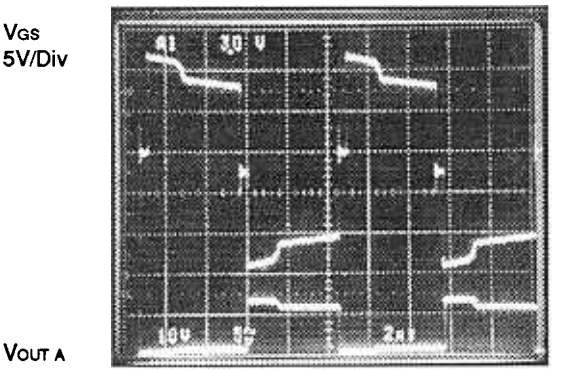


Fig 12. Gate Drive Waveforms

Output Filter Section

Output Inductor: The output inductor selection was kept as simple as possible by incorporating an standard, low cost wound toroid. The preregulated dc input supply from the Power Factor Correction circuit maintains almost a constant duty cycle near the maximum of 85%. Little inductance is needed, even in this 48 V output application due to the brief off-time incurred with high switching frequency. Slight modulation is required to overcome the incremental conduction (I*R) losses and variations in input bulk supply voltage.

$$L_{OUT} = V_{OUT}\, t_{OFF} / \Delta I_{OUT}$$

$$L_{OUT} = 48.8 \cdot 10^{-6} / 1.1 = 44\ \mu H$$

Once again, an off-the-shelf Pulse Engineering part, a high current toroidal inductor model# PE-51511 was used. This is a swinging choke featuring a two-to-one change in inductance, and specified at 85.5 µH without a dc load. At its 10 A rated current, the inductance decays to 43 µH which will double the ripple current to about 1.1 A peak to peak. This choke was selected for its full load parameters and the fact that it swings is a bonus. Use of this part in this 200 kHz, 10.5 A application exceeds the manufacturers intended operating range by 0.5 A. This shortcut was taken to simplify breadboarding the entire unit. Designers should further evaluate this as well as other options. Gapped center leg, low profile, low loss ferrite core geometries deserve consideration.

Output Capacitance: Maintaining the 100 mV maximum specification for peak to peak ripple voltage requires low ESL/ESR capacitors as mentioned in the Design Overview. With 1.1 A ripple current at 200kHz, the acceptable ripple voltage component will be 25 mV.

$$C_{OUT(min)} = I(p\text{-}p) / (8 \cdot f_{CONV} \cdot \Delta V_{OUT})$$

$$C_{OUT(min)} = 1.1 / (8 \cdot 200 \cdot 10^3 \cdot .025V) = 25\ \mu F$$

Two 15 µF low ESR/ESL electrolytic capacitors and two 1 µF ceramic multilayer capacitors are all placed in parallel to filter the output voltage. The electrolytics handle the bulk of the charge storage requirements whereas the ceramic units filter the high frequency parasitic spikes caused by the switching transitions and physical layout. All parts are rated at 63 Vdc and operated well within their ripple current ratings.

UC3875 Phase Shifted Control Circuitry

Programming of the individual functions of the UC3875 controller and UC19432 precision reference and optocoupler driver will be detailed in this section. The control circuit schematic is shown in Figure 13 for reference, and all IC pinouts refer to the 20 lead through-hole package.

Control Circuit Programming Outline:

A. Oscillator Frequency
B. RAMP and SLOPE functions
C. Error Amplifier and Soft Start
D. Current Limit Protection
E. Delay Section
F. High Current Outputs
G. Supply Connections

A. Typically, the control circuit design begins with the IC's oscillator section. Frequency is programmed at the FREQuency SET pin (pin 16) with a parallel resistor (R9) capacitor (C9) from this pin to ground. According to the datasheet curves, a 43K resistor and 470 pF capacitor are needed for the chosen switching frequency.

B. The IC will be used in conventional duty cycle (voltage mode) control without feed forward. Potential users of this technique are strongly encouraged to continue experimention with voltage feed forward, standard current mode control and average current mode control.

To perform the phase shifted modulation, the IC compares the error amplifier output (pin 2) to the RAMP input (pin 19). To facilitate direct duty cycle control the RAMP input requires a sawtooth waveform which is obtainable using the constant current source of the IC's SLOPE (pin 18) feature. The current programmed by Resistor R1 from SLOPE to VREF is internally mirrored to the RAMP pin, and only a capacitor from RAMP to ground (C5) is needed. These components are selected to give a full amplitude (3.8 V) signal within the oscillator's 5 µsec total period. A 75K SLOPE resistor and 75pF RAMP capacitor are used.

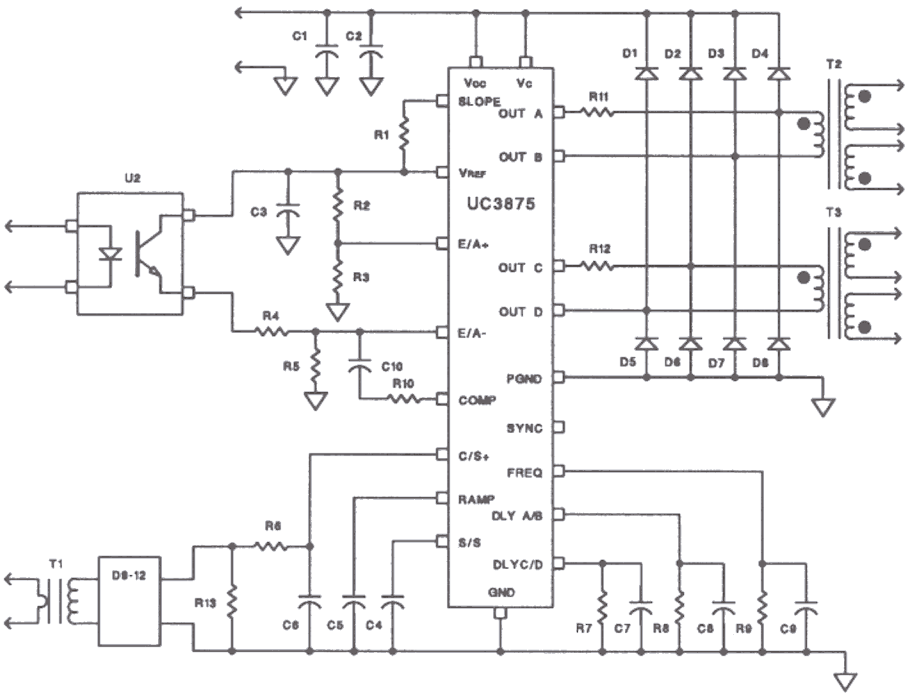


Fig 13. - Control and Drive circuit

C. The error amplifier (E/A) non-inverting dc input (E/A+) is best programmed near the center of its 5V common mode input voltage range, and 3V is used in this design. Two series resistors, R2 (2K) and R3 (3K) divide the 5V reference (Vref) voltage (pin 1) to 3V and feed the E/A noninverting input at pin 4. The reference also is supplied to the optocoupler's (U2) diode to power the feedback signal. This feeds two series resistors, R4 (1K) and R5 (3K) to develop the nominal 3V, closed

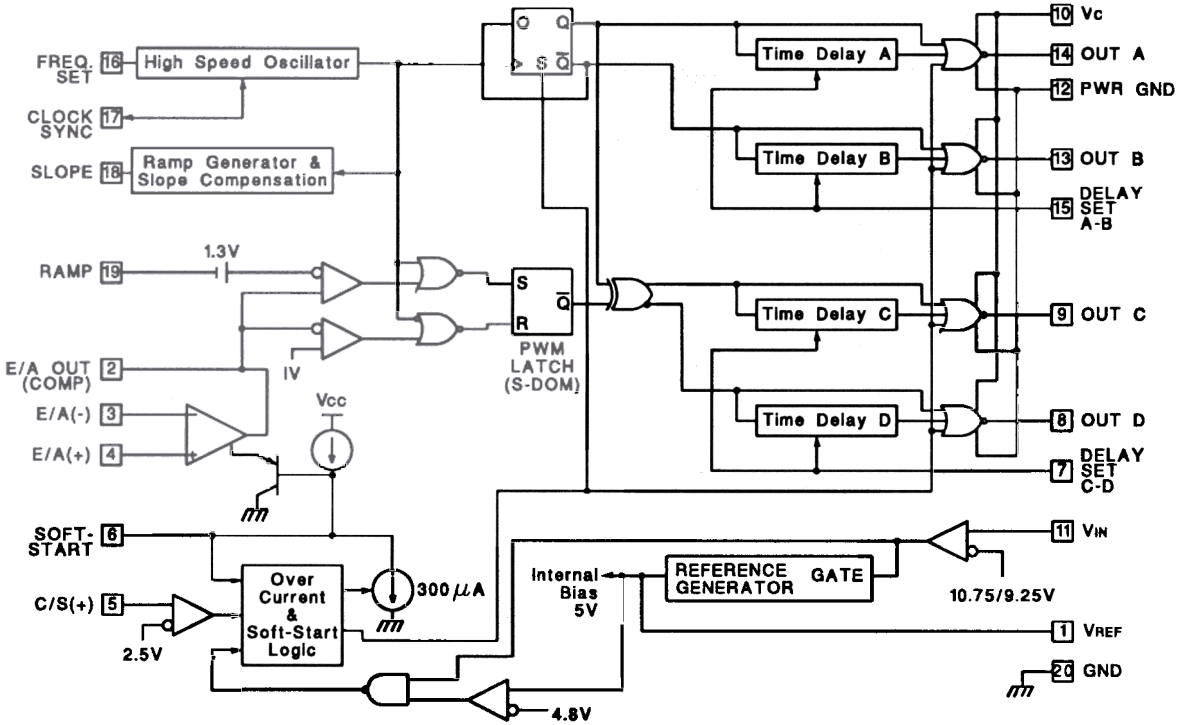


Fig 14. - UC3875 Block Diagram

loop feedback signal. The centerpoint of these resistors is input to the error amplifier inverting (E/A-) input at pin 3.

Compensation around the E/A is a series R/C network consisting of R10 (150K) and C10 (0.1μF). These exact values deliberately keep the amplifier low, as most of the compensation will be done on the secondary side before the optocoupler. Further details about optimization are presented in the feedback section.

D. Two forms of overcurrent protection are possible with the UC3875 controller; a non-latching shutdown with a full soft start cycle restart or a completely latched shutdown. The current sense input (C/S+, pin 5) is compared to a 2.5 V internal threshold and triggers a 300 uA current sink on the soft start (S/S, pin 6) capacitor to ground, holding the outputs low. The soft start capacitor voltage is also monitored to detect which mode of protection has been programmed. It must first drop below the 300 mV lower threshold before the current sink is released. Latched protection is obtained by externally supplying more than 300 uA of pull up current to the soft start capacitor thus not allowing discharge to the lower threshold. Non-latching operation, often called "hiccup" requires no external pull up since the IC contains an internal 9 uA source at this node. A full soft start time constant expires before operation recommences as the capacitor is used for the timing delay function instead of soft start during this time.

E. The ZVT transition delay is programmed at the DELAY SET A-B (pin 15) and the DELSY SET C-D (pin 7) inputs. A resistor to ground from each of these pins separately programs the current used to charge internal capacitors used to set the delay. Note that each leg delay time can be individually programmed which permits higher maximum duty cycles in high frequency converters than otherwise programming all delays for the worst case maximum of the right leg. The resistors (R7, R8) programming the DELAY inputs should be adequately bypassed with capacitors (C7, C8) to prevent noise spikes from modulating the delay functions.

F. Four 2 Amp high speed totem pole outputs within the UC3875 insure excellent gate drives to the full bridge switches. OUT A (pin 14) and OUT B (pin 13) deliver the upper and lower left leg drive signals respectively, whereas OUT C (pin 9) and OUT D (pin 8) are for the respective left leg gate drives. Note that all outputs are with respect to IC ground and that the two "high side" switch drives (OUT A and OUT C) must always be transformer coupled or level shifted. Outputs B and D, the two lower switches of the full bridge do not require isolation from the power stage. Schottky diodes are required to protect each output from being forced beyond the supply rails, as described in the gate drive section of this topic.

G. A 12 V bias is supplied to the V_{IN} (pin 11) and Vc (pin 10) connections from the PFC preregulator stage. These IC power connections should be well bypassed and filtered for best performance, likewise for the 5V reference (pin 1). There are two separate returns paths within the IC, a power ground (PWR GND pin12) for the high current output stages, and a signal ground (GND pin 20) connection for the analog circuitry. Note : These two grounds must be at the same electrical potential and work best when tied together directly at the IC pins. This is also where the bypass capacitor connections should be made. Separate signal and power ground "planes" are incorporated in this prototype to keep noise from each localized, but are connected together at the IC ground pins.

Isolated Output Voltage Feedback

No great efforts were attempted to optimize the voltage feedback path for this design example. A simple 5000 Vdc isolating optocoupler provides the primary side UC3875 error amplifier with the output voltage feedback information. A precision reference and optocoupler driver IC, the Unitrode UC39432 was incorporated for excellent dc output voltage stability and regulation. Power for this circuitry is derived from the 48 V output for simplicity, and a zener diode provides some degree of regulation. The loop was not optimized for this application as the main goal was to evaluate the phase shifted power stage. Further development efforts are needed.

Prototype Assembly

This 500 Watt converter was built on standard single sided PC board material using one etched board (as shown) primarily for the control and another "experimenter" type PC board for the power stage assembly. A base plate was simulated by using the flat sides of aluminum heat sink extrusions supplied by AAVID Engineering, model #61875. Each piece has a thermal rating of 2.7°C/W for a three inch length using natural convection cooling in free air.

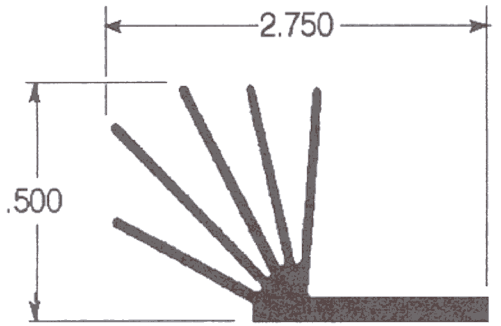


Fig 15. - Heat Sink Dimensions

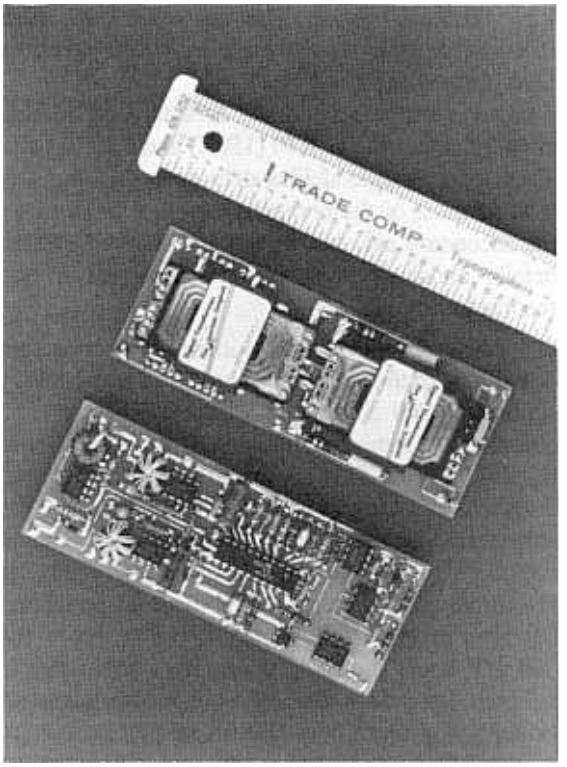


Fig 16. - Mechanical Assembly

Performance Evaluation

The assembled prototype was evaluated over it's intended operating ranges and various parameters were compared against the initial specifications. The 500 Watt power supply meets a majority of the intended goals including efficiency, power density, output ripple, line and load regulation. The unit did fall slightly short of being able to ZVT down to 50% of full load — only about 60% was achieved. This was a tradeoff highlighted in the Transition Analysis section. So while some increase in power loss was experienced near half load and below, the total losses decreased due to the lower current. Cooling and heat sinks should still be designed for full load operation which is the worst case for power loss.

A graph of the measured converter efficiency is shown in Figure 17 for loads above 300 watts. Efficiency remains above 93% in this operating region, but shows a sign of tailing off at the upper end. This could be improved by selecting larger MOSFETs as this increasing loss is primarily conduction loss. Be aware that this may also require lowering the switching frequency or increasing the circulating current which will reduce the benefits of switching to larger FETs in the first place. The spreadsheet program will help designers fine tune the tradeoffs involved. Peak efficiency was over 93.5% with loads between 325 watts and 450 watts, and just below 93% at full power output (500 W).

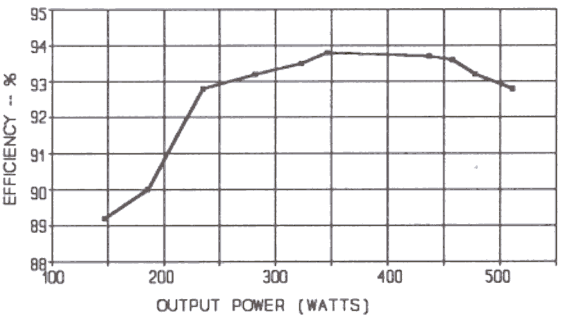


Fig 17. - Efficiency vs. Load

The effects of lossy, non-ZVT operation are clearly demonstrated by the efficiency measurements below 250 watts. Here, the primary circulating current during the freewheeling interval is too low to discharge the left leg switches output capacitance to zero prior to turn-on, and switching loss is incurred. At light loads, the same will hold true for the right (linear) leg switches which become unable to ZVT below about 6 A. Note that this point is generally lower than for the left leg's fully resonant transition, which loses its lossless transitions at about 6.5 A output current.

Total power loss versus load is shown in Figure 18 for reference. This demonstrates that non-ZVT operation is not the worst case for power dissipation in this design, and that full load is still the worst case. Therefore, operation under this lossy condition is acceptable from a thermal standpoint since ample cooling has been provided for much more power loss. Total losses range from about 20W at light load to 40W at full load. Heat sinks are selected for worst case power dissipation at full load, and there is plenty of margin at light loads in spite of the lossy transitions.

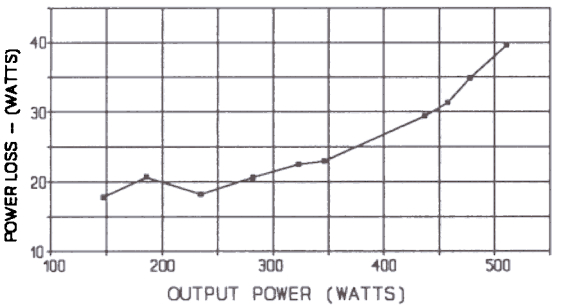


Fig 18. - Power Loss vs. Load

During normal operation with Zero Voltage switching Transitions, efficiency should be somewhat immune to changes in line voltage. This is true to a point, however there are some line dependant losses. The duty cycle does have to vary to maintain regulation. This changes the ratio of switch "on" to freewheeling times, and conduction losses for each mode are different. Additionally, the peak inverse rectifier voltages change with line on the transformer's secondary, also. Therefore, one should expect some change in overall efficiency with input line variations. Three measurements were made for this converter at high power and are shown in Figure 19.

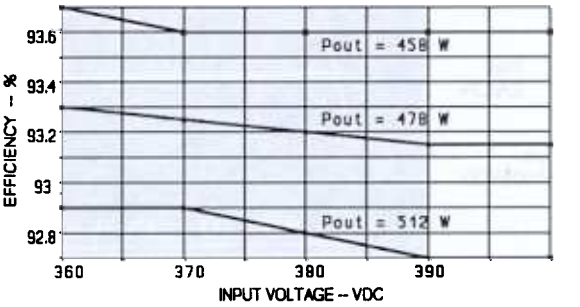


Fig 19. - Efficiency vs. Input Voltage

The results indicate that efficiency is higher with the lower inputs and reduces with increasing input voltage. Highest efficiency is achieved at 360 Vdc, corresponding to the lowest input voltage necessary to maintain the regulated output voltage. For this design, inputs any lower would cause the output voltage to sag since maximum duty cycle has been reached. It is conceivable to actively adjust the PFC preregulator output voltage for highest efficiency of the phase shifted converter. This is possible for all but the highest input line conditions, for example, above about 250 Vac in. Should the ac input mains get above this point, the PFC output voltage can be raised from 360 V nominal to 385 V, or so. A net increase of around 0.2% efficiency (1 Watt) is all that is to be gained, and possibly not worth the additional complexity for this application.

Full load operational primary voltages and current for one complete switching period can be observed in Figure 20. Note that this photo, and others, was taken with a 150 MHz gain-bandwidth oscilloscope at 100 Volts per division vertical calibration. The horizontal time base in Figure 20 (679 nanoseconds/division) is different from most of the others which use 1 microsecond per division, only to fit one complete period on the screen. This photo shows how clear the ZVT waveforms are by the absence ringing and overshoot. A similar photo for two switching periods is shown in Figure 21.

One of the full current right leg "linear" transitions is shown in detail in Figure 22 for clarity. The exact measured transition time corresponds well to

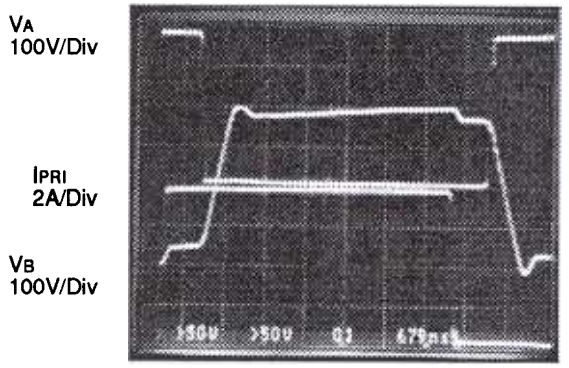


Fig 20. - One Switching Period

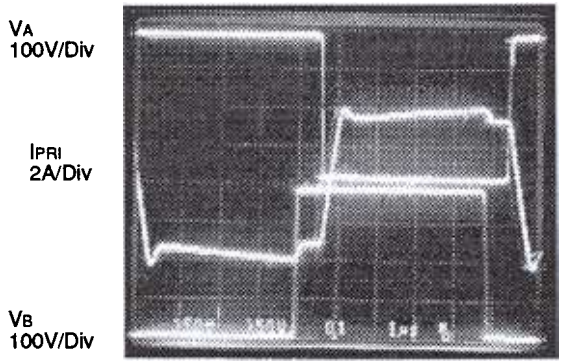


Fig 21. - Two Switching Periods

the spreadsheet value, and any difference is due to the approximated 8/3 Coss multiplier factor.[1]

The secondary side waveforms are shown in Figure 23. The top trace shows the output rectifier current at 10 Amps per division. Notice how this differs from a conventional full bridge. Due to the finite voltage drops in the primary during free-wheeling intervals, the primary current does NOT divide evenly between both diodes. In a phase shifted converter, the diode which was conducting load current continues to conduct until the primary voltage is reversed at the beginning of the next switching cycle. The output ripple voltage and transformer secondary waveforms are also shown. There is a slight overshoot in the voltage waveform as conduction begins, and this is due to leakage inductance between the secondary windings. A simple R/C snubber was used to control the amplitude of this, and no elaborate analysis of this is presented.

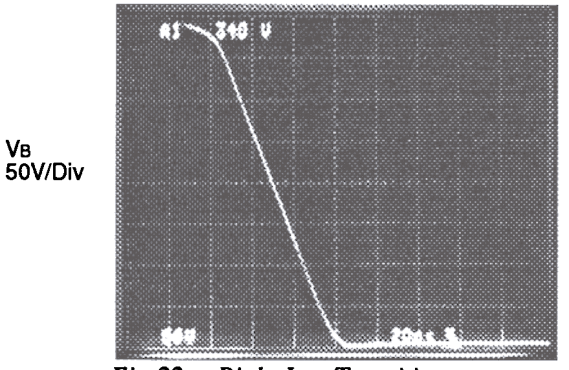


Fig 22. - Right Leg Transition

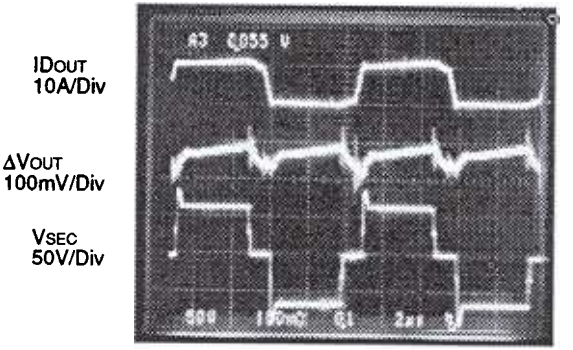


Fig 23. - Secondary Side Waveforms

Non-Zero Voltage Transition waveforms are featured in Figure 24 for the primary voltage and current at a 30 Watt (6%) load. Note that the primary voltage starts its normal linear and resonant transitions, but is then forced to the rail by the control and drive circuitry. It is also clear that enough energy was not stored in the tank to make the transition occur by normal means. Note too, that the power loss is not as bad as it could have been since the tank does drop the switch voltage significantly before turn-on. Spikes on the leading edge of the current waveform are caused by the output snubber circuit.

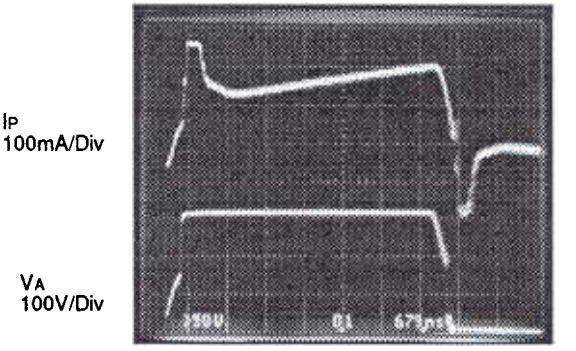


Fig 24. - Non-ZVS, "Hard" Switching

PERFORMANCE COMPARISON

Author [reference#]	Power (Watts)	Freq. (kHz)	Input (Vdc)	Output (V)	Eff. (%)
Steigerwald et al [3]	130	500	180-360	5	90
LoCascio et al [4]	200	200	254-353	12	81
Chen/Lofti/Lee (VPI)[5]	325	100	250-400	5	84
Dalal, Dhaval [6]	350	500	400*	5,3.3	85
Andreycak, B.	**500**	**100**	**400**	**48**	**93.7**
Chen/Stuart [7]	1500	200	260-340	75	90.8
Mweene/Wright/Schlect[8]	1500	500	190-380	40	90
Sabate et al (VPI) [9]	2000	100	550-600	360	94.5
Henze,C. [10]	2000	110	320	5.2	86
Henze,C. [10]	5000	110	320	5.2	80

* = not specified, but implied by use of 500 V MOSFETs

Performance Comparison

This 500 Watt evaluation unit was compared to other phase shifted PWM converters presented by various authors over the past few years. This is not an "apples-to-apples" comparison due to the different switching frequencies, input and output voltages and power levels, but does provide proof of the high efficiency conversion. Shown is a brief list of the other phase shifted PWM designs and results.

Conclusions

This design review presented a typical application for the fixed frequency, phase shifted ZVT switchmode technique. All evidence indicates that there is no reason in the future to intentionally design a conventional, non-phase shifted full bridge circuit. Efficiency is higher, and noise is significantly lower throughout the converter. Even the slight penalty incurred during non-ZVT operation is less that the best of the conventional full bridge. Device parasitics are fully incorporated into the design to perform lossless switching as opposed to the continual combat found with traditional switching. This design example serves as an additional technical reference in support of the phase shifted PWM technique. Also, a working prototype can be made using many "off-the-shelf" components, readily available to power supply designers, with minimal design effort.

Summary

This 500 Watt Design Review demonstrates only one of a vast number of possible applications for this switching technique. It is equally applicable at power levels both above and below 1/2 KW, depending on the circumstances and project goals. Higher output power and higher frequency operation need to be further explored, although the results should end up quite similar to this benchmark example. Needless to say, much higher power densities than today's off-line kilowatt unit standards are attainable.

Modular power supplies below 500 watts can also benefit from the phase shifted switching technique. Although commonly ruled out at 200 or 300 W, use of this full bridge converter should be exploited. Couple the attributes of high efficiency conversion with a very high switching frequency and an extremely dense, modular converter is possible, despite the additional complexity of having four switches. Transformer utilization is optimal, output choke volume is minimal. While first impressions of this technique may lean towards higher power applications, designers are encouraged to consider it also for power levels of a few hundred Watts.

The phase shifted, Zero Voltage Transition PWM technique successfully combines the attributes of fixed frequency conversion, lossless switching transitions and high efficiency operation.

Viva ZVT

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Acknowledgements

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Thanks also to Bob Mammano for his encouragement to prove that this technique really does work as claimed, and John O'Connor for his support.

Supplier List

AAVID Engineering, 1 Kool Path, Box 400, Laconia , N.H. (USA)
Phone # 1-603-524-4443

Coilcraft, 1102 Silver Lake Road, Cary, ILL. 60013 (USA)
Phone # 1-708-639-6400, FAX # 1-708-639-1469

Multisource Technology Corp., 393 Totten Pond Rd, Waltham, MASS. 02154 (USA) Phone # 1-617-890-1787, FAX # 1-617-890-8011

Pulse Engineering, P.O. Box 12235, San Diego, CA. 92112 (USA)
Phone # 1-619-268-2400, FAX # 1-619-268-2515

Signal Transformer Co. Inc., 500 Bayview Ave., Inwood, N.Y. 11696 (USA)
Phone # 1-516-239-5777, FAX # 1-516-239-7208

Appendix I -- UC3875 Full Bridge Phase Shifted Converter

MATERIALS LIST

CAPACITORS

All are 20 VDC Ceramic Monolithic or Multilayer unless indicated.

C1	1 uF
C2	47 uF - 25V Electrolytic
C3	1 uF
C4	1 uF
C5	75 pF- 16V Polystyrene
C6	0.001 uF
C7,8	0.01 uF
C9	470 pF
C10	0.1 uF
C11	1 uF - 450VDC Poly
C12	47uF - 450VDC Electrolytic
C13	1.2uF - 450 VDC Poly
C14	1uF - 100VDC
C15,16	220uF - 63VDC Electrolitic
C17	TBD
C18	1 uF
C19	22 uF - 25 VDC Electrolitic
C20	1 uF
C21	2.7 nF-200V Poly-low ESL & ESR

DIODES

D1-8	1N5820 3A-20V Schottky
D9-12	1N4148
D13	12V 3W Zener
D14,15	15A-200V Fast Recovery

INDUCTORS

L1	47uH-3A
L2	100uH-15A

RESISTORS

All are 1/2 Watt, 1%, Metal Film unless indicated

R1	75K
R2	2K
R3	3K
R4	470 Ohm
R5	3K
R6	100 Ohm
R7,8	6.8K
R9	43K
R10	150K
R11,12	10 Ohm
R13	20 Ohm
R14-17	10K
R18	3.6K, 1 W
R19	36K
R20	1K
R21	TBD
R22	TBD
R23	110 Ohms- 5W Carbon

TRANSFORMERS

T1	I Sense
T2,3	Gate Drivers
T4	Main XFMR

MOSFET TRANSISTORS

QA-D	IRF840 NMOS

INTEGRATED CIRCUITS

U1	UC3875 PWM
U2	Opto Coupler
U3	UC19432

Appendix II -- Excel Spreadsheet Formulae

	A	B
1	PHASE SHIFT ZVT CONVERTER DESIGN	TEST 1
2		
3	INPUT SUPPLY VOLTAGE, VIN, (V)	400
4	OUTPUT POWER, POUT, (WATTS)	=B5*B6
5	OUTPUT VOLTAGE, VOUT, (V)	48.8
6	OUTPUT CURRENT, I OUT, (A)	10.5
7	EFFICIENCY (estimate)	0.93
8	INPUT POWER (estimate) [PIN] (W)	=B4/B7
9	PRIMARY CURRENT [IPRI] estimate (A)	=B8/(B3*B11)
10	SWITCHING FREQUENCY (kHz)	200
11	MAXIMUM DUTY CYCLE (estimate)	0.85
12	TRANSFORMER TURNS RATIO [N = NP/NS]	5.33
13		
14	POWER SWITCHES	
15	MOSFET TYPE	IRFB40
16	MOSFET OUTPUT CAPACITANCE, Coss, (pF)	160
17	MOSFET Rds(on) @ 25 C (ohms)	0.8
18		
19	POWER LOSS ESTIMATES	
20	MOSFET TOTAL CONDUCTION LOSSES (W)	=4*1.5*B17*((B9)^2)*((0.5)^0.5)
21	OUTPUT RECTIFIERS P(LOSS) (W)	=2*0.65*B6*((0.5)^0.5)
22	MAGNETIC CORE LOSSES (W)	8
23	COPPER LOSSES (W)	6.5
24	TOTAL POWER LOSS (W)	=B20+B21+B22+B23
25	FULL LOAD EFFICIENCY (%)	=100*B4/(B4+B24)
26		
27	PRIMARY ZVT RESONANT TANK	
28	XFMR MAGNETIZING INDUCTANCE (uH)	7600
29	XFMR LEAKAGE INDUCTANCE (uH)	10
30	XFMR PRIMARY CAPACITANCE (pF)	15
31		
32	RESONANT TANK	
33	RESONANT CAPACITANCE, Cr, (pF)	=(((8/3)*B16)+B30)
34	RESONANT INDUCTANCE Lr (uH) * series	50
35	RESONANT TANK FREQUENCY (mHz)	=1/(B36*10^-3)
36	RESONANT TANK CIRCUIT PERIOD, T(res), (ns)	=2*3.14*(((B34*10^-6)*(B33*10^-12))^0.5)*10^9
37	RESONANT TANK FREQUENCY, wR, (mHz) radians	=6.28*B35
38	TANK TRANSITION TIME, t(res), (us)	=B36/4
39	RESONANT TANK IMPEDANCE, ZR, (ohms)	=((B34*10^-6)/(B33*10^-12))^0.5
40		
41	TANK ENERGY	
42	CAPACITIVE ENERGY REQUIRED, W(Cr), (uC)	=0.5*10^6*((((8/3)*B16)+B30)*10^-12)*B3^2
43	INDUCTIVE ENERGY AVAILABLE, W(Lr), (uC)	=0.5*10^6*(B34*10^-6)*B44^2
44	CRITICAL PRIMARY CURRENT FOR ZVT (A)	=((2*B42)/B34)^0.5
45	CRITICAL SECONDARY CURRENT FOR ZVT (A)	=B44*B12
46	MINIMUM LOAD FOR ZVT (% OF FULL LOAD)	=100*B45/B6
47		
48	TRANSITION TIME SUMMARY	
49	RIGHT LEG TRANSITION TIME, C/D (nsec)	=B33*B3/(B44*1000)
50	LEFT LEG TRANSITION TIME, A/B nsec)	=10^9*(ASIN((B3*(B37*1000000)*B33*10^-12)/B44)/(B37*1000000))
51	PRIMARY dI/dt SLEW TIME (ns)	=1000*2*B44*B34/B3
52	TOTAL TRANSITION TIMES, t(tran), (nsec)	=B49+B50+B51
53	POWER TRANSFER TIME, (1- t(tran)), (us)	=((1000000/B10)-B52)/1000
54	MAXIMUM DUTY CYCLE (ACTUAL%)	=100*B53/(1000/(B10))

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