Designing a Phase Shifted Zero Voltage Transition (ZVT) Power Converter

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Abstract:

This Topic highlights the design considerations incurred in a Full Bridge topology power supply using the Phase Shifted Zero Voltage Transition (ZVT) control technique. An overview of this switching technique including a comparison to the conventional PWM technique and step-by-step analysis of each timing interval is included.

Numerous design equations and associated voltage and current waveforms supporting this phase shifted technique are highlighted. Practical considerations are detailed regarding the design of the magnetic elements, power switching and control circuits. Information contained within this Topic is used to design, review and compare a 500 Watt converter elsewhere in this manual.

Introduction

The benefits of lossless Zero Voltage Transition (ZVT) switching techniques are well known throughout the power supply industry.[1-5] The parasitic circuit elements are used advantageously to facilitate resonant transitions rather than snubbing dissipatively. The resonant tank functions to put zero voltage across the switching devices prior to turn-on, eliminating power loss due to the simultaneous overlap of switch current and voltage at each transition. High frequency converters operating from high voltage input sources gain significant improvements in efficiency with this technique. The full bridge topology as shown in Figure 1 will be the specific focus of this presentation, with emphasis placed on the fixed frequency, phase shifted mode of operation.

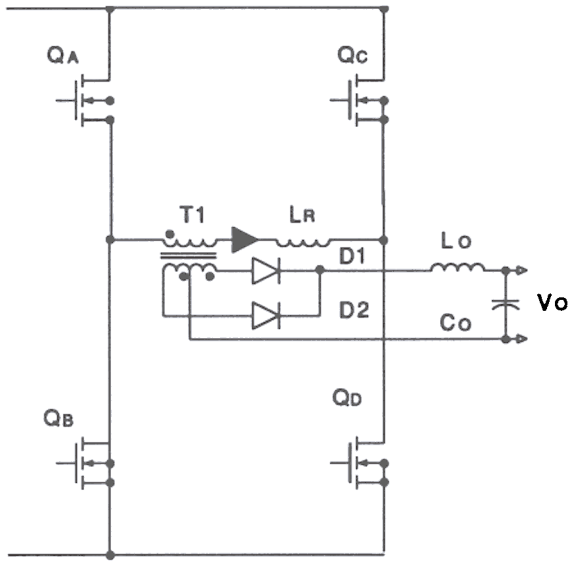

Fig 1. - Full Bridge Topology - General Circuit

Switch Drive Commands

The diagonal bridge switches are driven together in a conventional full bridge converter which places the transformer primary across the input supply in alternating polarity, as shown in Figure 2.

Power is only transferred to the output section during the ON times of the switches, corresponding to a specific duty cycle with fixed frequency operation. The duty cycle range of required for control is unique to the application, and can be estimated from the power supply input and output voltage specifications.

Instead of driving both of the diagonal full bridge switches together, in phase, these diagonal

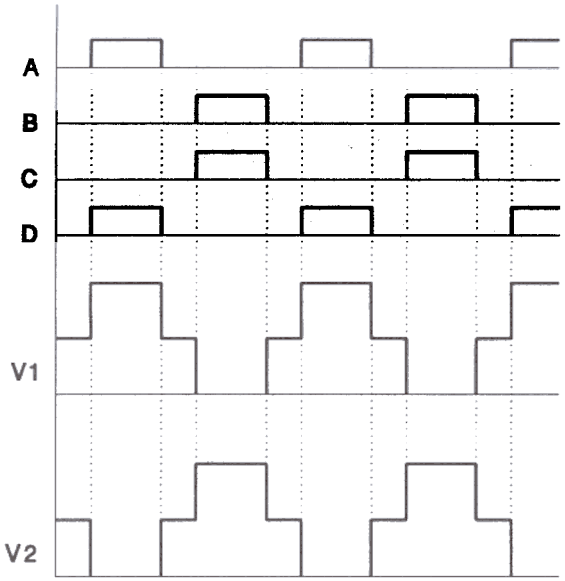

Fig 2. - Conventional Full Bridge Waveforms

switch gate drives are shifted in phase. Thus only one of the diagonal switches is on for some time before the other is activated. The effective duty cycle is controlled by varying the phase shift between these diagonal switch ON commands. So, rather than modulate the actual pulse width of the gate drives, the phase shift between them is modulated as shown in Figure 3.

Unique to this Phase Shifted technique, two of the switches in series with the transformer can be ON, yet the applied voltage to the transformer can be zero. These are not diagonal switches of the full bridge converter, but either the two upper or two lower switches. The transformer primary is essentially short circuited during this time. In reality, finite voltage drops result in a slightly decaying current slope. Primary magnetizing current is maintained at nearly a constant level since the magnetizing inductance is trying to reset into a short circuit. This freewheeling portion of the cycle is the off-time needed to achieve the required output voltage. Switches are held in this state until the beginning of the next diagonal power transfer interval corresponding to the required on-time.

When the appropriate diagonal switch is later turned off, the primary current flows into the switch output capacitance (*Coss*) causing the switch drain voltage to resonate to the opposite input rail. This puts zero voltage across the opposite switch of the particular bridge "leg", thus enabling Zero Voltage Switching when it is later turned ON. This is made possible by maintaining enough circulating primary current, and enough stored inductive energy to completely charge and discharge the FET output capacitances. It is during these bridge "leg" transitions that a brief dead-time or delay is programmed whereby both switches within one leg are held completely off. This delay allows the FET output capacitors to be charged and discharged by the circulating current.

Zero Voltage Switching Fundamentals

The circulating primary current which facilitates the transitions also clamps the switches at zero voltage, provided that enough energy has been stored. When this occurs, the FET body diode conducts the current and clamps the device at zero Volts. The MOSFET can be turned on at this time to lower the conduction loss by paralleling the body diode with its ON resistance, $R_{DS(ON)}$. FET's can conduct current in a bidirectional manner through their channel, and this is advantae8 geous to reduce power dissipation.

This clamped, circulating current

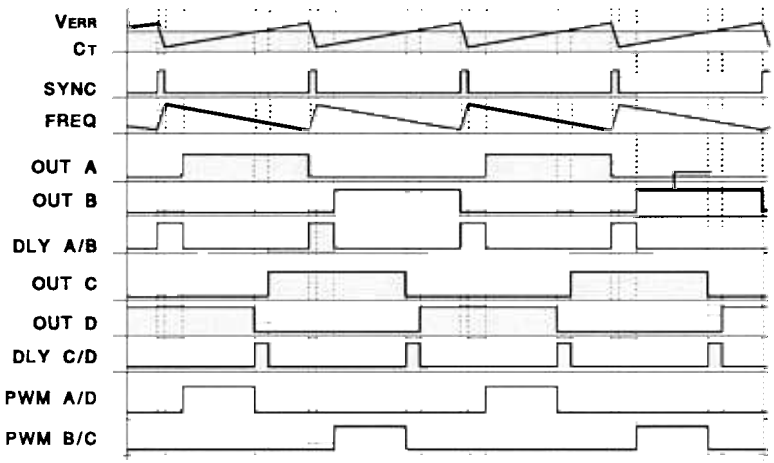

Fig 3. - Phase Shifted PWM Control Waveforms

condition is what facilitates fixed frequency power conversion. The switches are held in this "freewheeling" mode until the control IC's clock initiates the next switching cycle. Then one switch is released, and the circulating current transfers from the FET channel to its output capacitance, resulting in a lossless transition. By storing enough energy to accommodate a wide range of switch off-times, a wide duty cycle range is also achieved. Thus fixed frequency conversion can take place over a defined range of line and load conditions. Note that this freewheeling interval is what enables an otherwise variable frequency power conversion technique operate at fixed frequency.

The design consideration for stored energy required to ensure zero voltage switching occurs at minimum output load (minimum circulating current) and maximum input line as shown in Figure 4. This will be highlighted in detail in a later section.

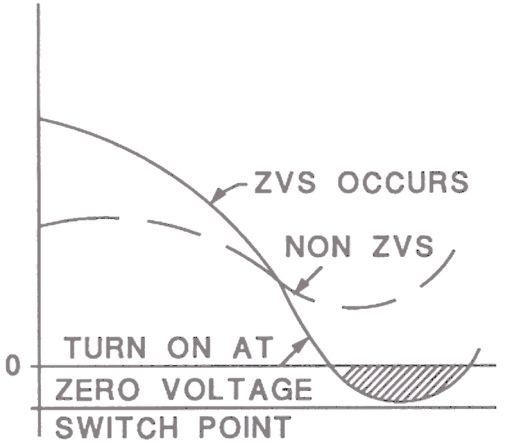

Fig 4. - ZVS Limitations

Phase Shifted Fundamentals

Switches within the Phase Shifted full bridge converter will be utilized differently than those of its nonresonant counterpart. Instrumental to this technique is the use of the MOSFET switch's parasitic elements. The internal body diode and output capacitance (Coss) of each device (in conjunction with the primary current) become the principal components used to accomplish and commutate the resonant transitions.

Circuit Schematic and Description: Detailed operation of the Phase Shifted Converter operation will begin following a description of the circuit elements. The circuit schematic of this technique is shown in Figure 5. including voltage and current designations.

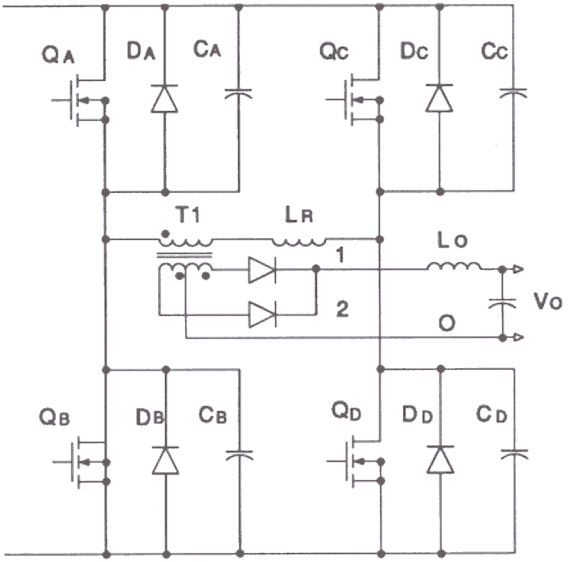

Fig 5. - Phase Shifted PWM Switch Orientation

The basic circuit is comprised of four switches labelled Q_A through Q_D and is divided up into two "legs", the right and left hand legs. Each switch is shown shunted by its body diode (D_A through D_D) and parasitic output capacitance, (C_A through C_D). These have been identified separately to clarify the exact elements and current paths during the conversion interval.

A detailed model of the transformer primary section is presented which separately indicates the primary leakage and magnetizing inductances and currents. The reflected secondary contributors to primary current are also shown for completeness, and divided into two components. The dc primary current I_P is the secondary dc output current divided by the transformer turns ratio N. The secondary ac current should also accounted for by multiplying the output inductance by N^2, or dividing the secondary ac ripple current $I_{SEC(AC)}$ by N as shown in Fig. 6.

Initial Conditions: $t = t_0$

The description of the Phase Shifted operation begins at the conclusion of one power transfer

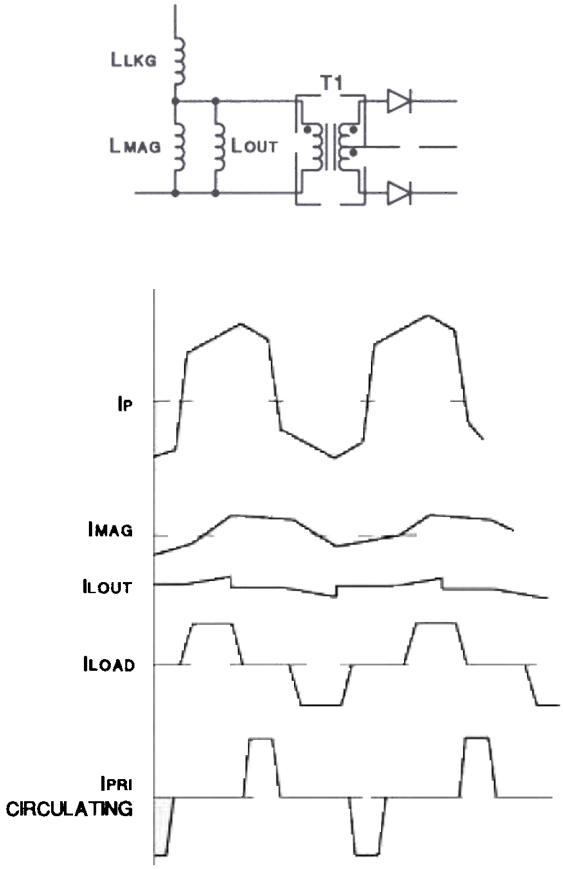

Fig 6. - Primary Magnetic Components

cycle. This occurs after the transformer has been delivering power to the load with two of diagonal switches of the converter conducting. The initial current flowing in the primary is designated as $I_{P(t_0)}$.

Right Leg Resonant Transition: $t_0 < t < t_1$

The primary current flowing at time t_0 is $I_{P(t_0)}(t_0)$ which was being conducted through the diagonal set of transistors Q_A in the upper left hand corner of the bridge and transistor Q_D in the lower right. Instantly, at time t_0, switch Q_D is turned off by the control circuitry, beginning the resonant transition of the right hand leg.

The primary current is maintained nearly constant at $I_{P(t_0)}$ by resonant inductance $L_{P(RES)}$ of the primary circuit, often referred to as the transformer leakage inductance.

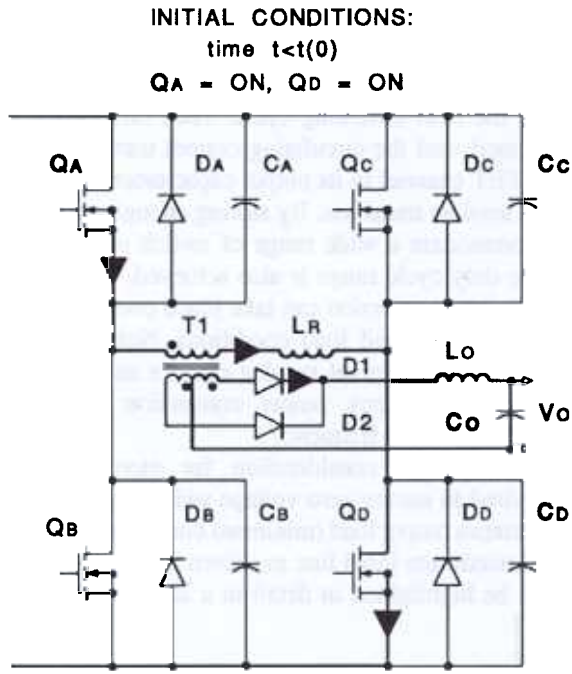

Fig 7. - Initial Conditions

Since an external series inductance can be added to alter the effective leakage inductance value, this presentation will refer to the lumped sum of these inductors as the resonant inductance, L_R.

In a practical application it may be difficult to accurately control the transformers leakage inductance within an acceptable ZVS range, necessitating an external "shim" inductor to control the accuracy. Also, if the transformer leakage inductance is too low to provide the desired transition times, an external inductor can be added to increase the resonant inductance.

With switch Q_D turned off, the primary current continues to flow through the switch output capacitance, Coss. This charges the capacitance of Q_D from essentially zero Volts to the upper voltage rail, $V_{IN}+$. Simultaneously, transformer capacitance C_{XFMR} and the output capacitance of Q_C is discharged as its source voltage rises from the lower to the upper rail voltage. This resonant transition positions Qc with no drain to source voltage prior

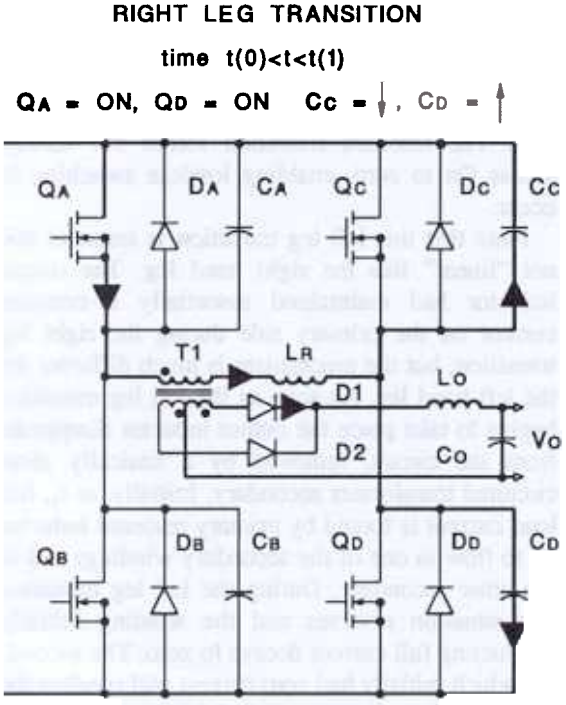

Fig 8. - Right Leg Transition

to turn-on and facilitates lossless, zero voltage switching.

The primary current causing this right leg transition can be approximated by the full load primary current of $I_{P(t_0)}$. The small change due to the barely resonant circuit contribution is assumed to be negligible compared to the reflected full load current. The resulting right leg "linear" transition time is a straightforward calculation of the resonant capacitance (C_R) being charged from a constant current source.

$$I = C\ dV/dt,\ or\ \ dt = C\ dV/I$$

For this specific right leg transition, the transition time can be approximated as:

$$t_{TRAN(RIGHT)} = t_1 - t_0 = C_R\ V_{IN} / I_{P(t_0)}$$

$$dt_{(1\text{-}0)} = C_R\ V_{IN} / I_{P(t_0)}$$

During this right leg transition the voltage across the transformer primary has decreased from V_{IN} to zero. At some point in the transition the primary voltage drops below the reflected secondary voltage, $V_{OUT}N$. When this occurs the primary is no longer supplying full power to the secondary and the output inductor voltage changes polarity. Simultaneously, energy stored in the output choke begins supplementing the decaying primary power until the primary contribution finally reaches zero.

Current changes in the output inductor according to its voltage (V_{OUT} minus the instantaneous applied secondary voltage, V_{PRI}/N) divided by the output inductance, L_{OUT}. Current transfer between the output rectifiers is predominantly determined by the series (winding and wiring) inductance of the secondary current paths whereas the initial di/dt is determined by the primary resonant transition.

Once the right leg transition has been completed there is no voltage across the transformer primary. Likewise, there is no voltage across the transformers secondary winding and no power transferred, assuming ideal conditions. Note that the resonant transition not only defines the rate of change in primary and secondary voltages dV/dt, but also the rate at which current transfers to the output filter network.

Current in the conducting output rectifier D_1 stays constant until t_1. Since the voltage across the secondary winding collapses to zero, both output rectifiers will now share the full load output current I_{OUT} equally. Current in the rectifier that was previously off will quickly rise to $I_{OUT}/2$, while current in the previously conducting rectifier decays by a similar rate to $I_{OUT}/2$.

The primary current remains "constant" although the transferred current is reduced by the load current and output inductor contribution at time t_1. Residual current flowing in the primary causes the body diode of switch QC to conduct, clamping the transformer primary to nearly zero Volts.

Note that the delay time between switch D turning OFF and switch C turning ON corresponds to the right leg transition time. The control IC's right leg delay feature (DELAY C-D) will be programmed for the maximum right leg transition time which will occur at high line and light load.

Clamped Freewheeling Interval: $t_1 < t < t_2$

Once the right leg transition is complete the primary current freewheels through transistor Q_A and the body diode of switch Qc. The current would remain constant until the next transition occurs assuming that the components were ideal. Switch Qc can be turned on at any time after t_1. This shunts the body diode with the FET $R_{DS(ON)}$ switch resistance, thus lowering conduction losses. Although current is flowing opposite to the normal direction (source to drain) the channel of Qc will conduct and divide the current between the switch and body diode.

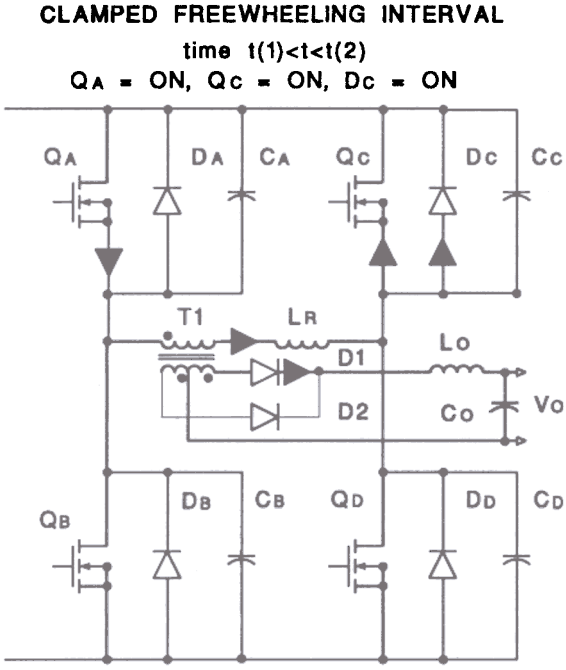

Fig 9. - Clamped Freewheeling Interval

Left Leg Transition: $t_2 < t < t_3$

At time t_2 the primary transformer current (which has been maintained by resonant inductor L_R) is slightly less than $I_{P(t_0)}$ due to small, but finite losses. Switch Q_A has been previously turned ON and switch Q_A will now be turned OFF. The primary current will now flow through the capacitance Coss of switch Q_A instead of through its channel. The direction of current flow causes the drain to source voltage of switch Q_A to increase and lowers its source from the upper to the lower rail voltage. Just the opposite conditions occur with switch Q_B which previously had the full V_{IN} across its terminals. The resonant transition forces the voltage across Q_B to zero, enabling lossless switching to occur.

Note that this left leg transition is resonant and not "linear" like the right hand leg. The output inductor had maintained essentially a constant current on the primary side during the right leg transition, but the mechanism is much different for the left hand leg. As soon as the left leg transition begins to take place the output inductor disappears from the circuit, removed by a basically short circuited transformer secondary. Initially, at t_2, full load current is forced by primary resonant inductor L_R to flow in one of the secondary windings and in the other secondary. During the left leg transition this situation reverses and the winding initially conducting full current decays to zero. The secondary which initially had zero current will conduct the full output current at the end of this transition. Note that the current in each winding never splits in half during the OFF period of power transfer as it does in a conventional, non-phase shifted full bridge converter. One side either conducts full load current, or none.

The left leg resonant transition is fueled by energy stored in inductors on the primary side. Part of this inductor is formed by the transformer's leakage inductance, although many applications will require an separate inductor to store enough energy. In either case, the exact circuit to describe this transition is a series L/C circuit with an initial current flowing equal to $I_{P(t_2)}$. L and C are the total series primary inductance and the effective circuit capacitance, C_R. Primary current during this transition has a sinusoidal shape with the peak amplitude occurring at time t_2. Because of this, solving for the exact transition time will require taking the arcsin of the function describing the transition parameters at time t_2.

$$t_{TRAN(LEFT)} = t_3 - t_2 = dt_{3\text{-}2}$$

$$dt_{3-2} = \frac{1}{\omega_R} \arcsin \frac{V_{IN} Z_R}{I_{P(t2)}}$$

Where Z_R is the resonant tank circuit impedance and ω_R is the resonant tank self oscillating frequency in radians, or:

$$Z_R = (L_R/C_R)^{1/2}$$

$$\omega_R = 1/(L_R C_R)^{1/2}$$

Once switch Q_B is turned ON at time t_3, the transformer primary is placed across the input supply rails and power will commence to transfer to the secondary since switch Qc is already ON. At t_3, the main transformer is connected across the input in reverse of the initial polarity, through the opposite pair of diagonal power switches.

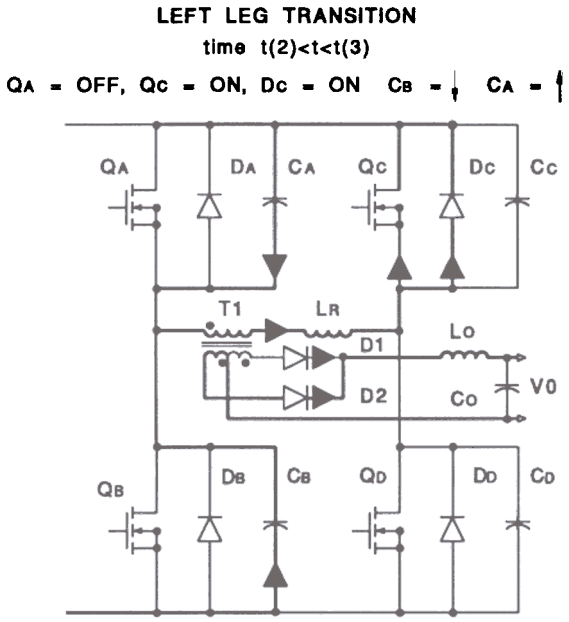

Fig 10. - Left Leg Transition

Note that this left leg transition will require more time to complete than the right leg transition. Conduction losses in the primary switches, transformer winding and interconnections result in a net dc voltage drop due to the primary current. Energy stored in the series resonant inductor and magnetizing inductance is no longer ideally clamped to zero voltage. This loss, in addition to the losses incurred during the previous transition reduce the primary current below its initial $I_{P(t_0)}$ value, thus causing a longer left leg transition time than the right leg.

Unlike conventional power conversion, one transistor in the diagonal pair is ON just before power is transferred, which simplifies the gate drive. An additional benefit can be realized by designating these commutating switches as the high side switches of the converter, usually far more difficult to drive than their lower side counterparts.

Power Transfer Interval: $t_3 < t < t_4$

This interval of the phase shifted cycle is basically identical to that of conventional square wave power conversion. Two diagonal switches are ON, applying the full input voltage across the transformer primary. Current rises at a rate determined by V_{IN} and the series primary inductance, L_R. The two time variant contributors to primary current are the magnetizing current (Imag) and the output inductor current reflected into the primary, L_{OUT}/N^2. The exact switch ON time is a function of V_{IN}, V_{OUT} and the transformer turns ratio N, just as with conventional converters.

Switch Turn Off: $t = t_4$

At time t_4, the upper right hand corner switch Qc is turned OFF, and one switching cycle is concluded. Current stops flowing in Qc's semiconductor channel but continues through the parasitic output capacitance, Coss. This increases the drain-to-source voltage from essentially zero to the full input supply voltage, V_{IN}. The output capacitance of the lower switch in the right hand leg (Q_D) is simultaneously discharged via the primary current. Transistor Q_D is then optimally positioned for zero voltage switching with no drain-to-source voltage.

The current during this interval is assumed to be constant, simplifying the analysis. In actuality, it is slightly resonant as mentioned in the right leg transition, but this is negligible in comparison to the full load current. The power conversion interval is concluded at this point and an identical analysis occurs as for the opposite diagonal switch set which has thoroughly been described for the switch set Q_A and Q_D.

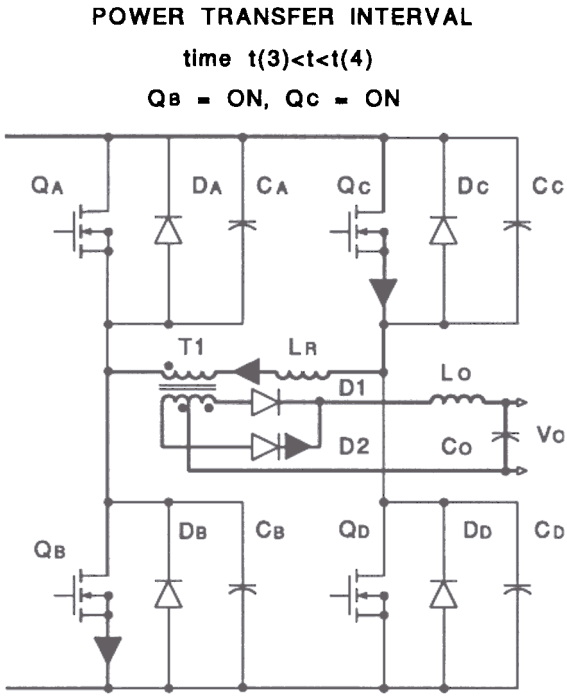

Fig 11. - Power Transfer Interval

The remaining intervals to complete the bipolar power conversion are identical to those previously described. The only difference is that they apply to the opposite diagonal switch pair respectively to execute a full switching cycle. Qc of the right leg will transition first, followed by primary current circulating through the lower switches Q_D and Q_B during the freewheeling interval. Then Q_B of the left leg will undergo a resonant transition, followed by the power transfer when Q_A turns ON.

Resonant Tank Considerations

The design of the resonant tank begins with the selection of a switching frequency which must be capable of achieving the required power density. Second, the maximum transition time must also be established based on achievable duty cycles under all operating conditions. Experience helps provide insight for acceptable results.

Transition Time Summary During ZVT Operation:

The longest transition time always corresponds to the converter's left leg transitions which are fully resonant. The maximum left leg transition time occurs when operating at the minimum (critical) load current for ZVT operation, and at the highest input supply voltage.

The shorter transition times always correspond to the converter's right leg transitions. The minimum right leg transition time occurs at full load with the lowest input supply voltage. Conversely, the maximum right leg transition coincides with light load, high line operation.

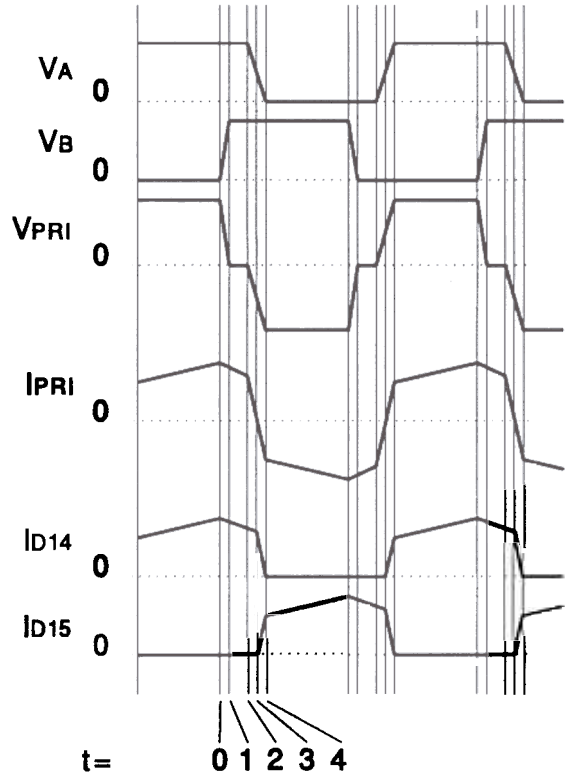

Fig 12. - Operational Waveforms

Resonant Circuit Limitations

Two conditions must be met by the resonant circuit at light load, and both relate to the energy stored in the resonant inductor. One, there must be enough inductive energy stored to drive the resonant capacitors to the opposite supply rail. Two, this transition must be accomplished within the allocated transition time. Lossy, non-zero voltage

switching will result if either, or both are violated. The first condition will always be met when the latter is used as the resonant circuit limitation.

Designers can argue that some switching loss may be of little consequence in a practical application at very light loads - especially considering that there is a significant benefit at heavy loads. While this may be a pragmatic approach in many applications, and a valid concern, this design procedure uses a minimum critical current for the worst case calculations. Lossy operation below the critical point will be discussed elsewhere in the material.

The stored inductive energy requirement and specified maximum transition time have also defined the resonant frequency ω_R of the tank circuit. Elements of this tank are the resonant inductor (L_R) and capacitor (C_R), formed by the two switch capacitances in parallel with the transformer primary capacitance C_{XFMR}. The maximum transition time is one-fourth of the self resonant period. This is the peak of the sinusoidal waveform which corresponds to either the switch voltage minima or maxima depend on its location in the leg, upper or lower. It is at this point where the zero voltage switching condition can be achieved.

The resonant tank frequency, ω_R:

$$\omega_R = 1 / (L_R C_R)^{1/2}$$

$$t_{MAX\ transition} = 1/4(2\pi/\omega_R) = \pi/2\omega_R$$

Resonant Capacitance

The specified MOSFET switch output capacitance, Coss, will be multiplied by a 4/3 factor per the MOSFET manufacturers Application Notes to approximate the correct average capacitance value with a varying drain voltage. During each transition, two switch capacitances are driven in parallel, doubling the total capacitance to $8/3 \cdot C_{OSS}$. Transformer capacitance (C_{XFMR}) must also be added as it is **NOT** negligible in many high frequency applications, especially at lower power levels where smaller switches are incorporated.

The resonant capacitance, C_R :

$$C_R = (8/3) \cdot C_{OSS} + C_{XFMR}$$

The capacitive energy required to complete the transition , $W(C_R)$ is:

$$W(C_R) = 1/2\ C_R\ V_{IN}^2$$

This energy can also be expressed as:

$$W(C_R) = ((4/3) \cdot C_{OSS} + C_{XFMR}) \cdot V_{IN}^2$$

Stored Inductive Energy

The energy stored in the resonant inductance must be greater than the energy required to charge and discharge the FET output and transformer capacitances of the leg in transition within the maximum transition time. The resonant inductor can be an external inductive device added in series with the main transformer, or it can be made entirely from the transformer's leakage and magnetizing inductances.

Inside the transformer, all of the inductive energy is stored in the leakage and magnetizing inductances since the secondary current has clamped the primary voltage to essentially zero. This causes high circulating primary current (as shown in Figure 12) in the physical winding but has no effect on the stored energy used to perform the ZVS transition. More detail about the tradeoffs and design optimization is presented in the Design Procedure.

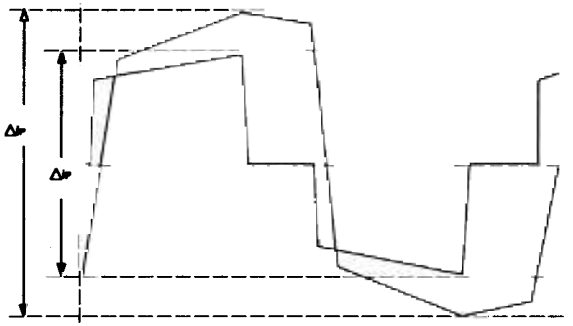

Fig 13. - Primary Current - ZVT vs Square Wave

The energy stored in the resonant inductor, L_R:

$$W(L_R) = 1/2\ L_R\ I_{PRI}^2$$

Note that ANY series primary inductance is considered as resonant inductance. This includes intentional and unintentional inductance associated

with physical connections, wiring harnesses, PC board traces and leakage inductance.

Resonant Circuit Summary

There are several ways to arrive at the solutions for the resonant inductor value and minimum primary current required for any application. Each of these is based upon the following fundamental relationships.

The resonant tank period must be at least four times higher than the transition time to fully resonate within the maximum transition time t_{MAX} at light load.

$$T_{RES} = 4t_{MAX}$$

$$f_{RES} = 1/(4t_{MAX})$$

$$\omega r = 2\pi f_{RES} = 2\pi/(4t_{MAX}) = \pi/(2t_{MAX})$$

The resonant radian frequency (ωr) is related to the resonant components by the equation:

$$\omega r = 1/(L_R\ C_R)^{1/2}$$

Both sides of this can be squared to simplify the calculations and reorganized to solve for the exact resonant inductor value:

$$L_R = 1/(\omega r^2\ C_R)$$

Previously outlined relationships for ωr and C_R can be introduced to result in the following specific equation:

$$L_R = 1/((\pi/(2t_{MAX}))^2 \cdot (8/3 \cdot C_{OSS} + C_{XFMR}))$$

Note that this Figure indicates the exact resonant inductor value required to satisfy only the task of resonant transitions. This resonant inductor is in series with the transformer primary and also defines the maximum primary current slew rate, $d(I_P)/dt$ as a function of input voltage.

$$d(I_P)/dt = V_{IN} / L_R$$

If the resonant inductor value is too large it may take too long to reach the necessary load current within the conversion cycle. The calculated inductor value satisfies the light load condition, however full load operation must also be evaluated. Details of possible solutions to this are highlighted in the Practical Applications section of this paper.

Stored Energy Requirements

As detailed, the energy stored in the resonant inductor must be greater than the capacitive energy required for the transition to occur within the allocated transition time. The governing equations are summarized below.

$$1/2 * L_R\ I_{PRI(MIN)}^2 > 1/2 * C_R * V_{IN(MAX)}^2 \text{ , or}$$

$$L_R\ I_{PRI(MIN)}^2 > C_R\ V_{IN(MAX)}^2$$

Since C_R and V_{IN} are known or can be estimated for a given application, this term becomes a constant and L_R has been quantified.

Minimum (critical) Primary Current

The minimum primary current required for the phase shifted application can now be determined by reorganizing the previous equation. Operating below this critical current level will result in lossy transitions.

$$I_{PRI(MIN)} = [\ (C_R * V_{IN}^2)\ / L_R\ ]^{1/2}$$

This value can be supported by calculating the average current required to slew the resonant capacitor to the full rail voltage. Although this figure will be lower than $I_{P(MIN)}$, it can be used to confirm the calculations.

$$I_{R(AVG)} = C_R\ V_{IN}/T_{MAX}$$

Obtaining the necessary amount of primary current can be done in several ways. The most direct approach is simply to limit the minimum load current to the appropriate level. One alternative, however, is to design the transformer magnetizing inductance accordingly. Also assisting the magnetizing current is the reflected secondary inductor current contribution which is modeled in parallel. Any duty cycle variations modifying the peak charging current must also be taken into account.

Generally the magnetizing current alone is insufficient in many off-line high frequency converters. The transformer is usually core-loss limited which means numerous primary turns and a high magnetizing inductance. Shunting the transformer

primary with an external inductor to develop the right amount of primary current is one possibility, although impractical. Incorporating the output filter inductor magnetizing current to assist resonance on the primary side is also another alternative.

Phase Shifted PWM Control Circuitry

Probably the most critical control aspect in the phase shifted PWM technique is the ability to span the full 0 to 180° phase shift range. Falling short of performance on either end of the spectrum can place unnecessary burdens on the fault protection circuitry or primary switches. Loss of control at either extreme will result in catastrophic consequences by turning on both transistors in a given "leg" simultaneously. The UC3875 Phase Shifted controller features the required circuitry to deliver both zero and effectively full duty cycle. Additionally, the UC3875 is utilized to perform the necessary control, decoding, protection and drive functions for this application. Peak current mode control is implemented for this example although the IC is equally suited for conventional voltage mode control, with or without input voltage feedforward. When used in current mode, the IC accepts a 0 - 2.7 V maximum current sense input and facilitates adding slope compensation.

A synchronizable oscillator is programmed by an R - C network from the frequency set pin to ground. Synchronization is performed by driving the SYNC pin from another UC3875 or external circuitry. The precision 5.0 Volt bandgap reference is available to program the noninverting input of the error amplifier as well as optional external functions. Output regulation is achieved using the 7 MHz gain-bandwidth on-board error amplifier which feeds the high speed PWM circuitry. Soft start is accomplished with a capacitor to ground which gradually increases the error amplifier output, corresponding to pulse width, phase shift or peak current, depending on the exact implementation. This signal is compared to the Ramp input of the IC having a useable input range from 0 to 3.8 V.

Delays between the output drive commands to facilitate Zero Voltage Switching are programmed at the Delay Set inputs. One unique feature of the UC3875 is the ability to separately program the A - B output delays differently from the C - D outputs. This capability allows designers to squeeze out every last percentage of maximum duty cycle, very important in high frequency converter applications. Inability to program each of these delays separately can also result in lossy, non-zero voltage switching of the full bridge converters switches under some operating conditions.

The four UC3875 output totem poles can each deliver 2 A peak gate drive current, more than adequate in a high frequency transformer coupled gate drive application. To minimize noise transmitted back to the analog circuitry, the output section features its own collector power supply (Vc) and ground (PGND) connections. Local decoupling capacitors and series impedance to the auxiliary supply further enhances performance. Fault protection is established by the programmable current limit circuitry. Full cycle

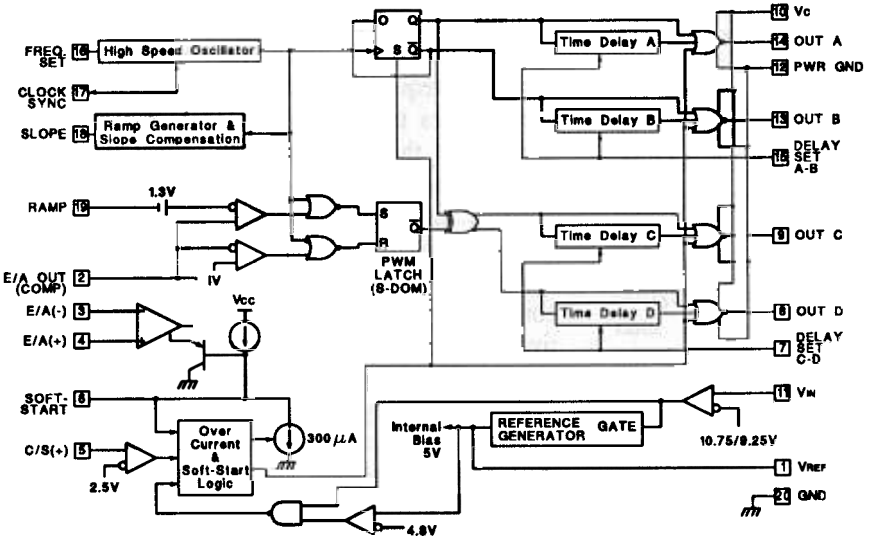

Fig 14. - UC3875 Block Diagram

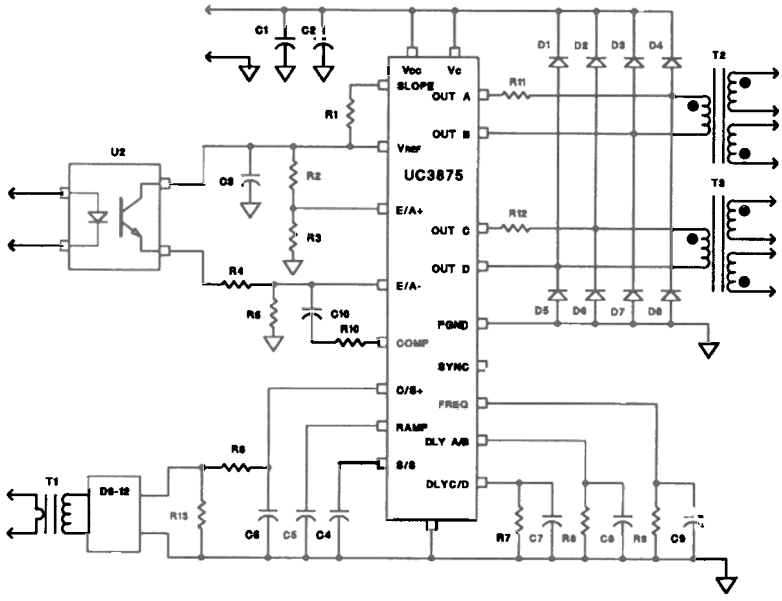

Fig 15. - Control Circuit Schematic

restart corresponding to the time programmed by the soft start interval minimizes power dissipation in a short circuited output.

Practical Application Considerations

General: There are numerous subtleties involved with this control technique that become more apparent as one begins to experiment with a breadboard. The References listed at the end of this Topic should also be consulted before commencing the design, as additional design intricacies are highlighted. Also, before venturing off to reinvent the wheel from the ground up, consider modifying an existing, conventional full bridge power supply first. This does not need to be exactly the supply of your goal, just one to get up and working with minimal efforts. Start with a known working unit, take NOTHING for granted, measure efficiency, regulation and EMI/RFI over various line and load combinations. Go through this section and the references, do all of the required calculations, modify the supply, debug and troubleshoot, then compare the results. The author encourages each designer to share their results with him, in confidence, as demonstrated proof of the merits of lossless Zero Voltage Transition power conversion.

Mosfet Switch Selection and Efficiency: Increased efficiency with little penalty can be obtained easily by using larger MOSFET switches at two locations. Specifically, the right "linear" leg switches (C and D) can deliberately be bigger ones than used for the left "resonant" leg. This is because the full output current propels the right leg transition, and a higher current is almost always present. Therefore, switches with higher output capacitance (*Coss*) and lower conduction losses ($R_{DS(ON)}$) can be substituted with little effect on maximum duty cycle. The savings here could easily amount to a few watts, even at moderate power levels, corresponding to a 1 - 3% increase in efficiency at full load. The spreadsheet program used in the Design Review Topic of this manual can be used to determine the exact numbers.

Facilitating the Left Leg Resonant Transition: There are a few different techniques to make the left leg transition possible, especially within a reasonable time. One technique as shown in the Design Review section of this manual is to add an inductor in series with the transformer primary. This inductor stores enough energy (W_L) to overcome the required capacitive energy (W_C to align the switches to zero voltage each transition. One attribute of the series inductor is that it does not require increasing the primary current as other possible solutions do. It does, however, limit the rate of rise of the primary current which can impact the achievable duty cycle. It is also an additional component in the circuit, but it is the best alternative for lower frequency designs in the author's opinion. There are other options.

One other way to make the left leg transitions possible is to increase the leakage inductance of the main transformer and store the required energy there. This can be facilitated by an intentional, less than optimal transformer design. There are a couple of concerns that designers must face if they pursue

this option. First, sacrificing an optimal transformer design, just to increase primary leakage inductance will probably add parasitic inductances elsewhere in the transformer. These may surface on the secondary side, which may require snubbing and add power loss. Magnetic coupling will suffer in addition to the transformers efficiency. However, if the amount of required leakage inductance is small, this could offer a better solution than adding an external inductor.

It is also possible to add an inductance in parallel with the transformer primary. This inductor stores energy during the power transfer intervals of the switching cycle. During the free wheeling intervals, the inductor current is circulated in the primary, thus facilitating the transitions with the FET output capacitances. This approach may not be practical in most applications. If little energy is needed to facilitate the transition the required inductance gets to be large with a high voltage input supply. Keeping core losses low will generally dictate a large number of turns on the winding as well as needing a large core to begin with. Note too, that the primary current increases by a certain amount which adds conduction power loss to the primary switches. All things considered, adding a parallel inductor to facilitate the transitions may be less than desirable.

Lossy, Non-zero Voltage Transitions at Light Loads: It would be great to be able to design a phase shifted converter to operate over a wide input voltage and output power range under lossless conditions, but this goal is not easily achievable. Generally, most designs will incorporate a crossover point at a reduced power level where lossy switching begins. This is because it is impractical to store enough energy to facilitate lossless transitions at a light load. And there is nothing wrong with this mode of operation. At the crossover point, the left "resonant" leg will first lose its zero voltage switching attribute, and at even lighter loads this will be true for the right hand "linear" transition. Note that the primary resonant tank component values (C_R and L_R) have not changed, only the stimulus — primary current. Therefore, any attempt to modulate or adjust the delay times will have only worsening effects, assuming that they were programmed properly from the onset. This is because the switch voltage waveform will be at its lowest amplitude, hence lowest loss at a delay time equal to one-fourth of its resonant frequency, ω_R. So even while MOSFET switching losses are incurred below the critical primary current, these losses are lower than they would be for conventional forced switching with the full input voltage across the switches. A photo of non-ZVT operation demonstrates this:

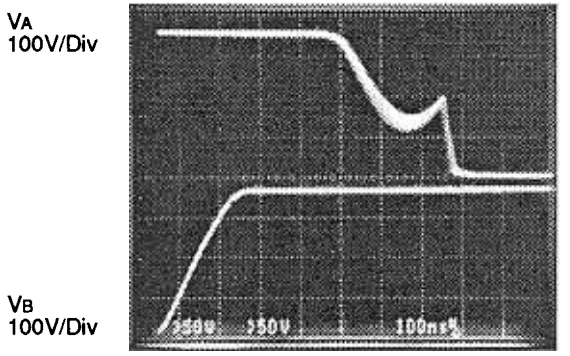

Fig 16. - Non-ZVT Operation

Practical ZVT operation down to about 1/3 of full load power is achievable in most applications. Even though the total power loss increases below this crossover point, the total losses are much less than at full load. Therefore, the heat sinks provided for the main switches are more than adequate. EMI/RFI can increase, but should be less than for the full load case. A curve showing total losses versus output power is shown in Figure 18 of the 500 Watt converter Design Review.

Maximum Duty Cycle: Adding a series inductor to facilitate ZVT transitions does decrease the effective maximum duty cycle for power transfer. The inductance limits the rate of change of the primary current so that full power is transferred for a shorter portion of each cycle. If this becomes an excessive amount, then the transformer turns ratio can be affected. One way to accommodate this is to slightly reduce the switching frequency so that the desired maximum duty cycle is still achieved. This is a reasonable design choice in most low to moderate frequency applications which may not require much adjustment. High frequency converter designs may need to pursue another route to adding series

inductance. Note that any series inductance helps to control EMI/RFI caused by switching current, and may reduce secondary rectifier recovery losses.

Efficiency: High efficiency is one of the major benefits with any Zero Voltage Transition technique. Several phase shifted converters have been built by various authors at power levels between 130 Watts and 2000 Watts, demonstrating efficiencies between 84% and 90%, even with a 5 Volt output. Efficiencies of 90 - 94% have been reached with higher output voltages (40 to 48V) for distributed dc bus and Telecommunication supply applications. Consult the References section for further details.

A 500 Watt power supply was built using the fundamentals described in this text. It delivered a peak efficiency of 94% at full load with very slight degradation at lighter loads. This was achieved with a 360 Vdc input and an output of 48.8 V at 10.5 A switching at 200kHz, as detailed in the referenced Design Review Topic. Clearly, at this relatively high switching frequency, conventional switching could not approach this efficiency due to the lossy discharge of the MOSFET output capacitances alone, never mind the switching loss.

Summary

The fixed frequency phase shifted control technique of the full bridge converter offers numerous performance advantages over the conventional approach. Switching losses due to the simultaneous overlap of voltage and current disappear along with the dissipative discharge of the FET output capacitance. EMI/RFI is significantly lower, also due to the "soft" switching characteristics which incorporate parasitic elements of the power stage advantageously. For most applications, there is little reason to consider the traditional square wave counterpart of this phase shifted PWM technique for future designs.

Using this technique beyond 500 Khz is probably not optimal. Transition times quickly erode the useable duty cycle to a point where the transformer turns ratio has been compromised. This could result in unreasonably high primary currents and power loss in the switches. Any incremental gains in cost or power density by reducing the size of the output filter are probably nullified by the needs for larger MOSFETs and heat sinks.

This phase shifted PWM technique excels in the majority of mid to high power, off-line applications. Although peak efficiency is obtained with moderate (2:1) load ranges, excellent results can also be obtained in designs with load ranges of 4:1 or 5:1. especially when non-ZVS operation at lighter loads is acceptable, considering the advantages under all other operating conditions.

Also, the Unitrode UC3875 Phase Shifted Control IC has been introduced to simplify the control circuit design challenge. Features of the UC3875 include 2 MHz operation and four 2 Amp peak totem-pole output drivers for high frequency applications. Separate programming of the different A-D and B-C leg transition intervals has made available to optimize converter performance. Finally, the flexible control logic permits current mode or voltage mode control, with or without input voltage feedforward. The complexity of control, drive and protection of the fixed frequency phase shifted converter has been fully addressed in a single integrated solution.

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