

Distributed Power Systems

Bob Mammano

Introduction to Distributed Power

Traditionally, power generation for an electronic system was assigned a particular location in the system's structure where a central power supply would reside, powering all the system's elements through a network of cables or buses as shown in Figure 1A. The advantages of this approach include concentrating all the power processing technology – including thermal management – into a single box which could then be designed, sub-contracted, or purchased as a stand-alone item. This was particularly appropriate if the system designer did not own the necessary power processing expertise.

Distributed power, such as an approach shown in Figure 1B, represents a converse technique. In a distributed power system the system's power requirements are allocated to a number of smaller power processing units which are then distributed

throughout the system in a variety of architectures, usually with the intent of bringing power processing closer to where the power will be used. While the ultimate extension of this concept is the "on-card" regulator or power supply, many other solutions for distributing power processing tasks are common. Before discussing the various architec-

tures, however, it is helpful to understand the motivation for considering distributed power.

Advantages of Distributed Power

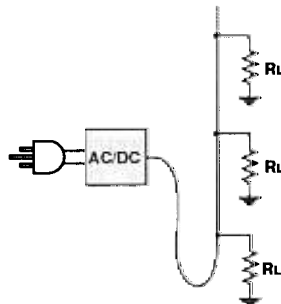
While not all of the following list of potential advantages are common to all distributed power configurations, it is still a list worthy of consideration during any power system definition phase.

1. Standardized designs: A centralized power supply almost by definition must be designed specifically for each new set of requirements. A goal of distributed power is the availability of standardized off-the-shelf modules or designs which could be combined in a variety of ways to meet a specific application. This has obvious benefits in development time and engineering costs as well as the confidence gained from using pre-qualified power components.

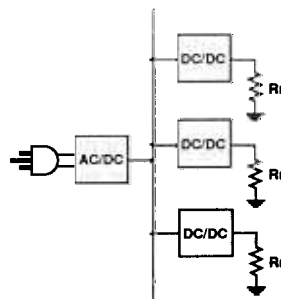
2. Ease of customizing: If unusual requirements are encountered, it is much easier to modify, redesign, or replace a smaller power module allocated to the unique portion of the system than to redesign a larger central power supply. Customizing a supply delivering common load voltages is often as easy as paralleling the required number of standard power modules needed for a given requirement. A corollary of this benefit is the ease of accommodating system growth, or recovering from an overly optimistic initial estimate of the system's power needs.

3. Maintainability: With distributed power it is possible to localize and isolate faults much more readily and, with properly designed parallel systems, on-line replacement (hot-swapping) will allow repairs to be made with a minimum of down time.

4. Packaging: A look inside any kilowatt or larger power supply will impress anyone with the



1A - Central Power



1B - Distributed Power

significant amount of mechanical hardware necessary for high power processing. Clearly, these requirements are greatly diminished as the power level is reduced and the need for heavy bus bars and special heat sinks is diminished. This benefit also has a corollary in thermal management where a distributed power system, by distributing the sources of heat generation, can often rely on conducted or radiated cooling, sometimes eliminating the need for air moving equipment.

5. Power density: If all else is equal, it would probably take considerably more volume to house n modules than a single power supply with n times the power, however all else need not be equal. Specifically, as the power level goes down, the switching frequency can go up without a decrease in efficiency, resulting in greatly enhanced power density for lower power modules. Ongoing improvements in the technology of almost all the components which go into a power supply are continually enhancing this benefit as distributed power modules with power densities of 50 to 100 W/in³ are becoming available.

6. Reliability: The reliability of a power system is obviously enhanced if it consists of a paralleled configuration of $n+y$ modules where n is the minimum number of modules necessary to meet a given load requirement and y is a number of additional units (usually 1) which gives the system the ability to tolerate y failures without impact. While reliability is certainly affected by the relative design philosophies used, it can usually be shown that while the number of components may go up in a distributed system, the lower power levels result in reduced stress levels, both electrical and thermal, benefiting overall reliability.

7. Efficiency: As load voltages are reduced, the IR drops in the power distribution conductors become ever more significant. A major benefit and goal of distributed power should be to generate the high current, low voltages close to where they will be needed and to power the distributed power units with higher voltages and correspondingly reduced current levels.

Applications for Distributed Power

While we may not often think of power utilities in the same context with electronic systems, the most obvious example of distributed power is our nationwide 60 Hertz power grid. Clearly the problems of distributing 110Vac power over hundreds of miles would be insurmountable were it not for the distributed network of step down transformers to process the power from much higher transmission voltage levels to household values.

Smaller examples where power is used at some distance from its point of generation can be seen in ships and airplanes where power is distributed at higher voltage levels and converted at locations closer to the point of use. These applications, like the utilities, are typically designed for ac transmissions where the local power processor involves a 60 or 400Hz transformer, a relatively bulky item. It is interesting to note that a similar technique was initially proposed for the Space Station but with the transmission frequency changed to 20kHz to reduce the size and weight of the line transformers. While an interesting concept, this approach suffered (perhaps fatally) from problems associated with EMI generation and power factor control.

The most obvious example of distributed power in electronic systems is in telecommunications where the initial use of -48V batteries as power backup has led to the standardized application of a 48V dc distribution bus for all types of telecommunication equipment, much of it now digital systems operating from 5V power.

Both military and space systems have had an ongoing need for distributed power systems dictated by the need for reliability rather than distribution efficiency. To aid in this effort, the various defense organizations have spent millions to fund the development of very dense and reliable standard DC/DC power conversion modules.

Certainly large computer systems are prime candidates for distributed power due to their large usage of low voltage power. As logic voltage levels drop below 5V, this need to process the power at the point of use will be almost mandatory. While a ½ Volt drop in the power distribution lines is a costly 10% loss at 5V, it becomes an unacceptable waste at three volts and lower.

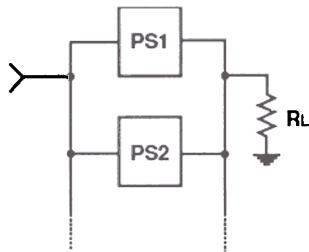
Those familiar with automotive systems are aware of significant power distribution problems as ever-increasing quantities of electronic components are connected to the 12V battery. It has been accepted as a given eventuality that cars will soon have to be equipped with 24V batteries. This will surely spawn a need for local down converters distributed throughout the automobile.

Distributed Power Architectures

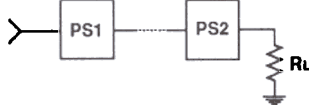
While distributed power architectures can get quite complex and specialized, most are either derived from or combinations of four basic configurations which are shown in Figure 2. These are: parallel, series, split source, or split load. It should be recognized that in addition to different interconnections, each of these approaches represents a solution to a different set of objectives. A description of these architectures and their characteristics is given below:

1. Paralleling:

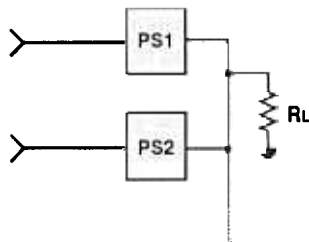
Paralleling power modules infers a common source and load. This usually means retaining a central location where a single high power supply is replaced with a grouping of paralleled lower power modules. While the power processing is distributed, it may not be distributed very far. Parallel connections



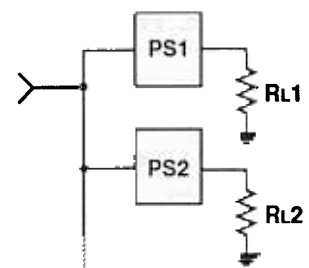
2A - Parallel Modules



2B - Cascading



2C - Source Splitting



2D - Load Splitting

are often generated by the need for standardization and redundancy rather than reducing distribution losses. With higher reliability as an objective, equalizing stresses by insuring load sharing between modules is usually required. Configuring power converters for current sharing when paralleled is not a trivial problem but ICs for that purpose as well as the use of current-mode control methods provide ready solutions.

It should be noted that most approaches to equal current sharing require at least one more interconnection between modules in addition to the common source and load connections. Figure 3 shows current mode control where the output of the voltage sensing error amplifier is used by the PWM modulator to control output inductor current. By using a single error amplifier to control all the paralleled modulators, equal currents from each module can be assured. A more thorough description of current sharing techniques can be found in Reference [1].

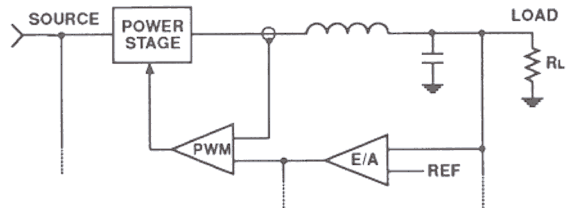


Fig 3 - Paralleling with Current Mode Control

2. Series (or cascading): With a cascaded power system, an intermediate bus voltage is developed with each interconnection. A typical cascaded system would be to follow a power factor correcting pre-regulator with a down converter as shown in Figure 4. Since each block in a series system handles the same current, it would not seem prudent to process the power twice, however there are offsetting benefits. Specifically in the example of

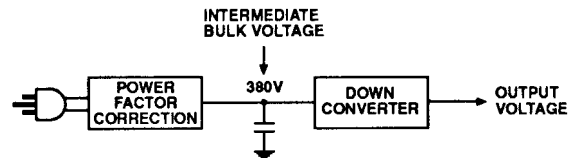
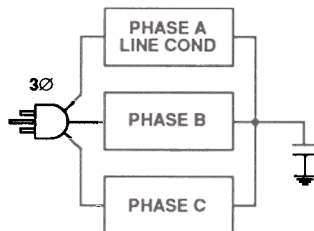


Fig 4 - Cascaded Power Processing

Figure 4, the PFC module, in addition to removing distortion in the input line current waveform, accommodates a wide range of input line voltage variation and provides a semi-regulated intermediate voltage of 380Vdc. Using this voltage on the bulk storage capacitors provides a very efficient means of accommodating long hold-up requirements.

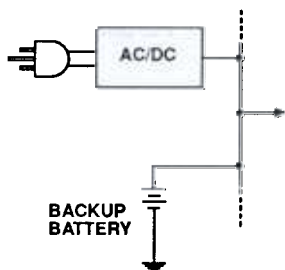
The down converter then reduces the 380V to a more manageable bus voltage but, with minimum input variation, this converter can be designed very efficiently with a large duty cycle and have a fast control loop for good dynamic load regulation.

3. Source splitting: Driving multiple power processing units from different sources is probably more limited in application. Two specific illustrations of this approach are shown in Figure 5. In 5A, a separate line conditioner – which might include a power factor corrector – is used on each leg of a three phase power line. A split source connection is also indicated when there are completely different sources of power such as the battery backup system of Figure 5B.



5A - Three Phase Source

Another use of split source distributed power is in redundant systems where, in addition to redundant power modules, the system will have two or more distribution buses and each bus becomes a source for a portion of the output modules.



5B - Battery Backup

4. Load splitting: The most common understanding of distributed power assumes split loads where different portions of the system are each powered by their own power processing unit. An illustration of load splitting is shown in Figure 6. Note that this gives innumerable options in terms of dividing up the loads and the corresponding requirements on the power processing units. If the

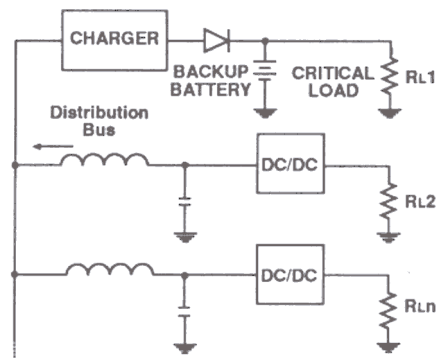


Fig 6 - Splitting Loads

units are on-card regulators then their power capability could be determined by the load on that particular board. Where battery backup is required, it need only be applied to that portion of the system which must stay active during a power fault.

While there is certainly an incentive to standardize, the output power processors could range from simple linear regulators, through non-isolated switching regulators, to a broad range of transformer-coupled DC to DC converter topologies. With converter design optimized for particular sections of the load, load regulation performance can be excellent. An additional advantage is the possibility of isolating noise-generating loads from the rest of the system. A load generated noise signal must pass through *two* converters to get to adjacent portions of the system.

5. Combinations: Many – if not most – systems will be configured using combinations of the above architecture. Figure 7, illustrates a common ap-

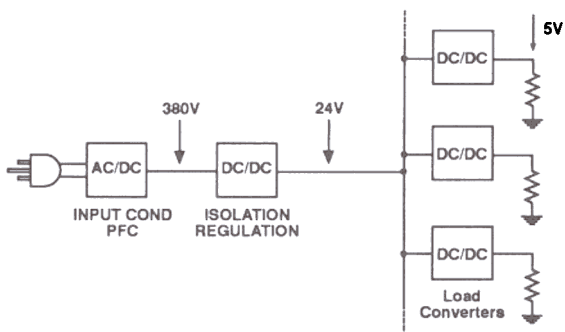


Fig 7 - A Typical Distributed Power System

proach with a cascaded PFC and down converter with split-load output units. A highly redundant architecture which uses all the above alternatives is illustrated in Fig. 8.

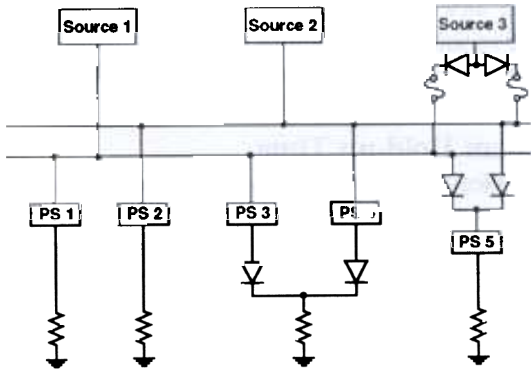
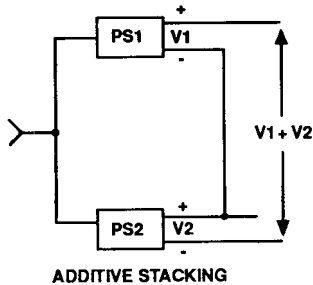


Fig 8 - Highly Redundant, Parallel Bus

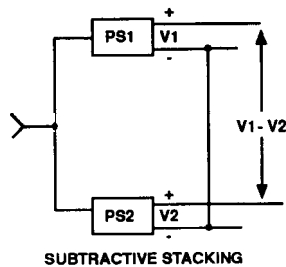
6. Stacked modules:

Mention should be made of one further way of combining power modules – this for the purpose of obtaining additional voltage levels. Figure 9 shows the stacking of two modules so that their individual output voltages either add or subtract. This type of power processing unit must be designed with the capability for floating outputs and consideration must be given to the possibility of reverse output currents.



ADDITIVE STACKING

Fig 9A



SUBTRACTIVE STACKING

Fig 9B

Distribution Bus Voltage Levels

Once the decision is made to use a distributed power system, the obvious next question is the selection of bus voltage levels. With the recognition that losses in the distribution network are usually determined by I^2R , higher bus voltage levels with correspondingly lower currents make for a more

efficient system. The countering arguments usually relate to safety and it is the system designer's task to reach an acceptable compromise. While selections can, and often are, unique to particular systems, several choices have been used often enough to qualify as standards. A review of some of these is outlined below:

1. **AC line power:** Disassociated from the utility network, it is not uncommon to distribute ac line voltage to multiple power units within a system as shown in Figure 10. The obvious advantage is that each distributed element is also a stand-alone item – particularly appropriate if the system consists of an assembly of independently purchased items. Of course, this is not a low cost approach.

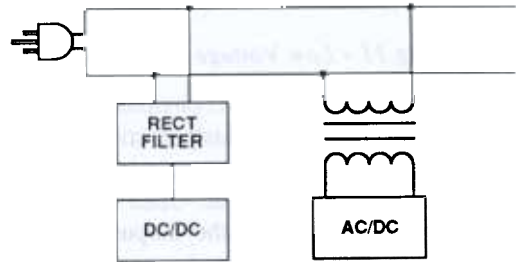


Fig 10 - AC Distributed Bus Voltage

2. **High-frequency AC:** As discussed above, perhaps an idea whose time has not yet come.
3. **High voltage DC:** With a value in the range of 350 to 400V, this is a natural choice as it is the nominal output from a boost power factor and line conditioning block. Clearly, a substantial amount of power can be transmitted at this voltage level with minimal line drops. Just as obvious, safety is a considerable issue. An equally troublesome feature is that this voltage (actually any dc voltage much over 32V) may sustain an arc which makes every switch and connector a significant problem.

While the transmission losses are low with high voltage, each point of use will require a relatively sophisticated DC/DC converter which must include a transformer (albeit at high frequency) for voltage stepdown to load levels.

4. **Low Voltage DC:** An interesting counterpoint to a 300+V bus is the use of a very low voltage dc for distribution. The decision here is to accept some

I^2R losses in the distribution bus in return for very simple, low cost point-of-use regulators. One extreme example is shown in Figure 11, where a computer system distributes power at 6 volts ($\pm 0.5V$). While this demands good regulation of the bus voltage and a well engineered network, the gain is that the local on-card 5V regulators can be simple, low-drop linear types. These provide excellent dynamic load regulation at a very low cost.

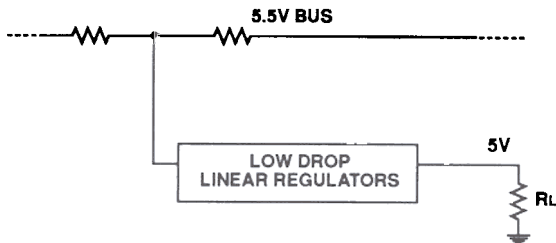


Fig 11 - Low Voltage Bus

Between 360V and 6V there is obviously a lot of room to maneuver. Many industrial controls use 24Vdc while the military and aerospace have a long history of standardizing on 28Vdc. Often the choice of bus voltage is defined by the output level of some difficult-to-change source, for example, the voltage provided by the backup battery.

The -48V batteries which have been in use by telephone companies for years fall into this category. With the backup battery defined, it was easy for the telecommunication industry to select 48Vdc as their bus voltage of choice. This voltage level received added emphasis with the European Telecom Standards EN41003 and UL1950 which designate 60Vdc the maximum SELV (Safety Extra Low Voltage) limit. With agreement on 60V as the maximum voltage which will not create a hazard, a nominal bus voltage of 48V has become a widely accepted value as the best compromise between low distribution losses and safety. As such, if there is any one voltage level which could be considered a standard for distributed power, it would be 48V.

One such standard has been recently defined in the Futurebus backplane distribution specification for computer applications, designated IEEE 896.2 - 1991. In addition to several low-voltage bus levels, this specification defines a 48 volt level with a tolerance of 38 to 54 volts. An additional require-

ment of this standard is that this 48V bus must be a fully isolated power source. That gives the user the opportunity to make it a +48V, -48V, $\pm 24V$, or any other combination which adds up to 48V total differential. This means that the most versatile load modules will in turn be isolated so that the ground will be defined by the load and not the source.

System Hold-up Time

Typically, most power systems have a requirement to maintain some intelligence for a specified period of time after removal of the input supply. Without a backup power source, this means energy storage somewhere in the power path. If only a small and defined portion of the load has the hold-up requirement, it might well be provided with capacitor storage at the point of use; but more often the location of hold-up energy will be on or before the distribution bus. So this may be another important criteria for defining the bus voltage level.

Since energy stored in a capacitor is proportioned to the square of the voltage, it is clear that the higher the voltage, the less capacitance is required for the same energy storage.

To offer a specific example, if we assume a constant load power of 500 W, and ask for 50 nsec hold-up time during which the bus voltage is allowed to drop by no more than 20%, the value of the required storage capacitance is:

$$C = \frac{2P_T}{V_1^2 - V_2^2}$$

If the initial voltage is 350V, then:

$$C = \frac{2 \times 500 \times 50 \times 10^{-3}}{350^2 - 280^2} = 1134 \mu F$$

If, on the other hand, the initial voltage is 24V, then:

$$C = \frac{2 \times 500 \times 50 \times 10^{-3}}{24^2 - 19.2^2} = 242,000 \mu F$$

A Typical Distributed Power System

For all the reasons discussed above, the system shown in Figure 12 is probably illustrative of the

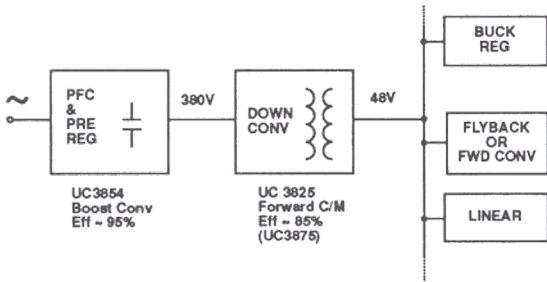


Fig 12 - Distributing a 48Vdc Bus

most common implementation of a distributed power system. The first block – which can be designed for either single or three phase inputs – provides the line conditioning, power factor correction, EMI filtering, line pre-regulation, and energy storage at a high bulk voltage. This block usually consists of a boost converter controlled by an IC such as the UC3854. Its power capabilities can range from a few hundred watts to several thousand, utilize a 50–100kHz switching frequency and, with reasonable effort, achieve a conversion efficiency in the mid 90% range. The boost topology provides a non-isolated, high voltage dc output.

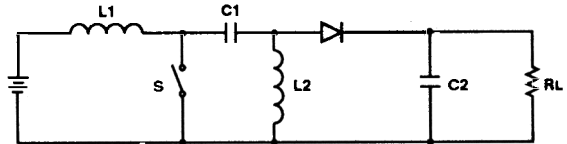
The second block is typically a forward converter operating with current mode control for maximum dynamic response to load variations. A transformer is included for isolation and efficient stepdown to the bus voltage. With a semi-regulated input voltage and an output of 48V, this converter can usually achieve 85% efficiency, even with switching frequencies above 100kHz. The circuit topology can be single-ended for power levels in the range of a few hundred watts, but above a kilowatt, a full bridge topology is usually needed. Control IC's used here would be the UC3844 at low power with perhaps a UC3825 when the application calls for a bridge circuit.

A relatively new consideration for a circuit topology applicable to the down converter block is a zero-voltage switched, phase shifted control for a bridge power stage. The UC3875 has been developed to control this topology providing low-loss switching at high power, even with switching frequencies approaching 1MHz. This technique will provide very efficient power conversion in a high power density configuration.

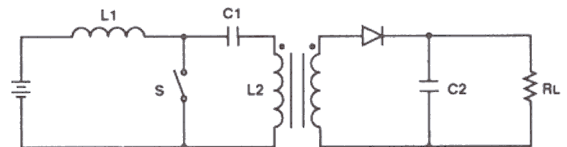
Single Stage Line Conditioners

While we have rationalized the use of two converter blocks in series to provide PFC and down conversion, there are a few power topologies worthy of mention which will do these functions in a single conversion stage. Although these all have some limitations which have prevented widespread use, they may be applicable in specialized applications so a brief overview is given below:

1. A flyback topology can be used to implement a high power factor pre-regulator as long as the power levels are low enough that the high peak switch currents do not become a major problem. By using a transformer as the inductive component, isolation and the ability to achieve a low dc output voltage can then be readily provided in a single switching function.
2. The SEPIC (Single Ended Primary Inductance Converter) circuit shown in Figure 13 is another possible topology. This circuit can be considered as a boost converter with an added LC between the input and output sections.



13A - Basic SEPIC Power Circuit



13B - Transformer Coupled SEPIC

When the second L is replaced with a transformer, again, both isolation and low output voltage are possible. This circuit has the added benefit of inherent short circuit protection due to the series capacitor but, by the same token, because this capacitor transmits full line power, it is often a costly element.

3. The Clarke Converter^[4] as shown in Figure 14 is a third alternative to providing PFC with a low output voltage. This circuit can be considered as a push-pull boost converter with a transformer

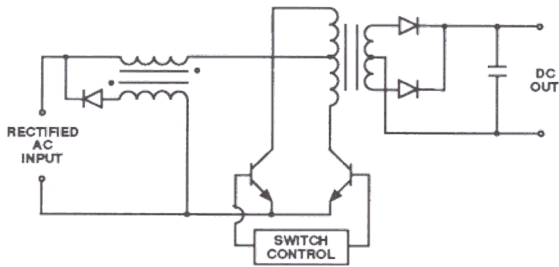


Fig 14 - The Clarke Push-Pull Boost Converter

coupled output. Since the circuit is inductor fed, the switches must have overlapping conduction periods and be capable of withstanding higher voltage levels, but the transformer is efficiently driven and will provide an isolated, low output voltage.

Load Regulators

The options for converting the 48V bus voltage to useful low voltage levels are too numerous to give an in-depth description. Clearly, the choices will be made on the basis of each specific requirement where performance and efficiency can be weighed against cost and simplicity with power level being an additional variable. Some possible choices which might be considered are the following:

1. A **simple buck**, or step-down switching regulator is a choice for non-isolated, single-value output levels. A typical circuit is shown in Figure 15, implemented with a UC2575HV. (The "HV" gives this device 63V input capability). Recognize that the conversion of 48V to 5V means a duty cycle of approximately 10% which will cause efficiency to suffer because of higher peak currents. By way of illustration, when powering a 5 Watt load, the circuit of Figure 15 has an efficiency of 76% with an input of 12V, 75% at 48V, and 68% at 60V.

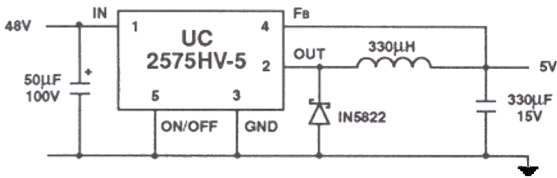


Fig 15 - Stepping Down from 48V to 5V

2. A **discontinuous flyback** circuit implemented with the UC3828 as shown in Figure 16 is a more efficient choice and has the added benefit of potential isolation and multiple output voltage capabilities. Again, the 60V capability of the UC3828 saves this implementation from excessive complexity.

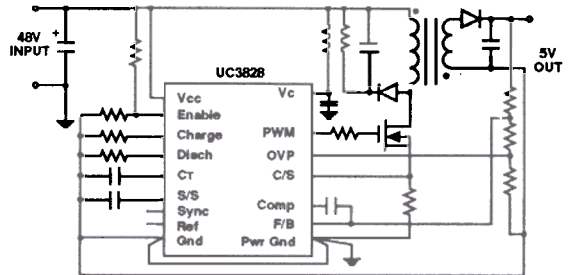


Fig 16 - Flyback Converter with UC3828

3. A **push-pull** converter topology similar to that shown in Figure 17 provides higher efficiencies as the power level rises. This 1.5MHz circuit, implemented with the UC3825, offers good performance in a small package because of its high switching frequency.

4. **Resonant and quasi-resonant** circuit topologies for very dense power modules operating in the megaHertz frequency range have been the object of significant interest. Initially these designs were implemented with zero-current switching for reasonable efficiency levels, but more recent designs with zero-voltage or multi-resonant topologies are showing even greater promise. While their high frequency operation can result in a very small package, the fact that the frequency is not constant can sometimes create problems at the system level.

5. **High voltage linear regulators** are still possible for light loads, with the use of a product such as the UC117HV which will accommodate a 65V input. Of course, with a 10:1 step down of 48V to 5V, the regulator's efficiency is only 10% and heat sinking may be an issue.

System Considerations

All the above discussions have been describing the distributed power blocks as stand-alone power processors, but it should be clear that there are some additional system level factors to consider.

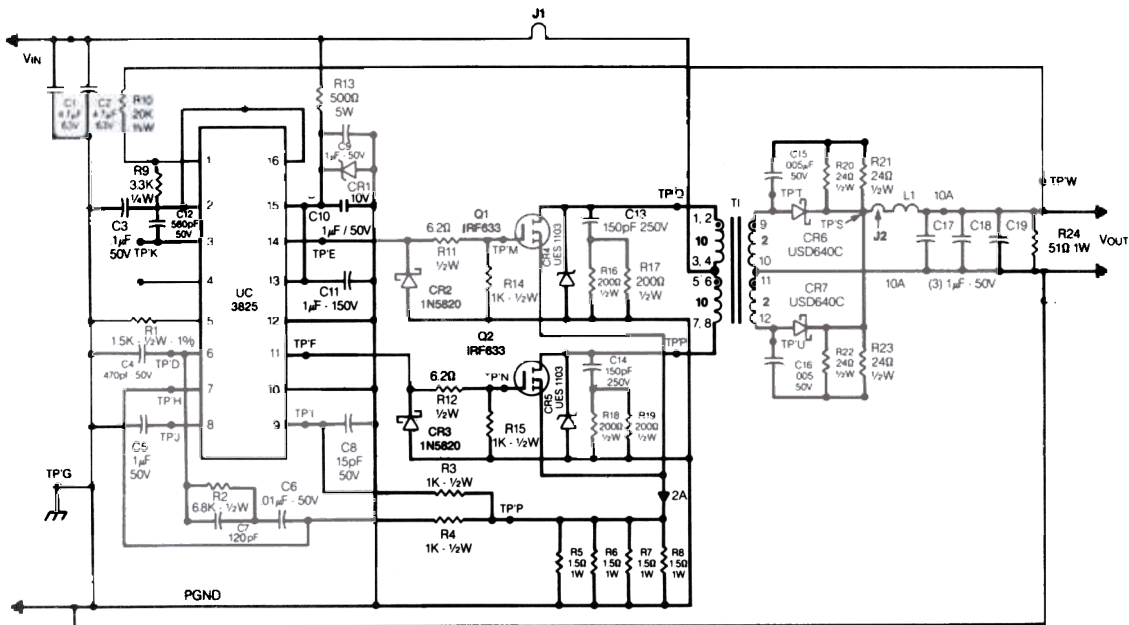


Fig 17 - A 1.5MHz Push-Pull Converter Using the UC3825

One of these is cost. While many cost-saving components, materials, and manufacturing techniques have been developed, the fact remains that one is unlikely to be able to build two converters as inexpensively as one. So it would seem that when compared just on the basis of hardware costs, a distributed power system will most likely be more expensive to procure than a single-box, central supply. Obviously, there are many other factors which enter into the equation and the growing popularity of distributed approaches can only attest to the many offsetting benefits.

An important consideration at the system level are the interactions – and in some cases, instabilities – which can occur when individual power processing units are connected together. A few – but certainly not all – of these characteristics are discussed below.

1. Shared output capacitor: In paralleling power units to deliver shared current to a common load, the location of the output capacitor as shown in Figure 18 can have an effect. While it might be easy to assume that a large capacitor located as close to the load as possible would give the best

dynamic performance, stability then becomes a function of the number of modules. Paralleling multiple modules lowers the total output impedance which can boost the crossover frequency of the overall loop. The preferable approach is to incorporate the output capacitor into the modules where the loop bandwidth will remain constant, regardless of the number of paralleled units.

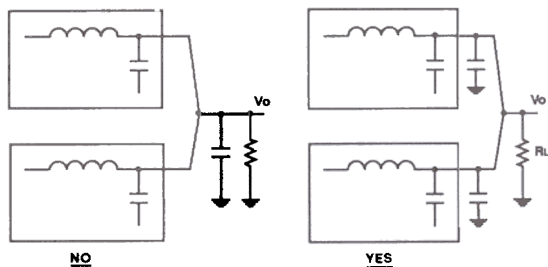


Fig 18 - Output Capacitor Location for Stability

2. Cascaded converters: Figure 19 shows the potential for several instabilities. Since a DC/DC converter is designed to deliver constant power to its load, its input impedance is a negative resistance. A front-end converter optimized for a resis-

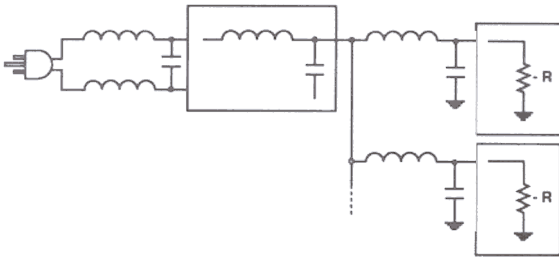


Fig 19 - Instability due to Negative Input Impedance or Multiple EMI Filters

tive load can often become unstable when connected to this negative resistance. If the driving converter is a buck-derived topology, this problem can often be addressed by raising the cross-over frequency of that unit; however, that solution may not be practical with a boost or other topology which contains an right half-plane zero. Under these conditions, substantial reductions in bandwidth may be required. Another way of assuring stability of cascaded converters is to design them so that the magnitude of the source impedance of the driving unit is smaller that of the input impedance of the following converter. Stability would be assured if this criteria could be met over the entire operating bandwidth, however this is often difficult to achieve and overly restrictive. A more typical characteristic is shown in Figure 20 where the impedances do overlap over a limited band of frequencies. Referring to the block diagram of Figure 21, the transfer function for the combined system can be described as:

$$F = \frac{V_2}{V_1} = \frac{G \cdot H}{1 + T_M}, \quad \text{where } T_M = \frac{Z_O}{Z_{IN}}$$

Where Z_O is larger than Z_{IN} , there is a loading effect which can be analyzed using the Nyquist criterion to determine the stability. Drawing a polar plot of the loop gain T_M will help define the phase margins at the points of overlap. With a knowledge of the phase of the source output impedance, a phase band for the input impedance of the following stage can be defined which will ensure both stability and minimal performance degradation. For additional details of this method, see Reference [5].

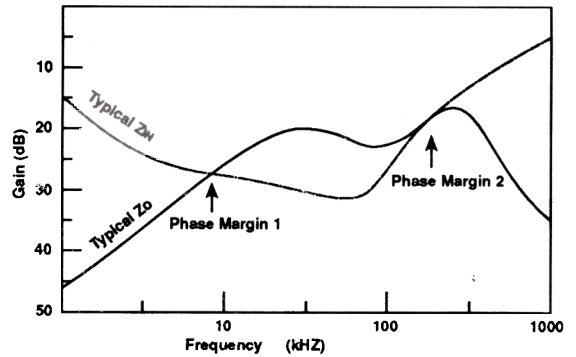


Fig 20 - Impedance Relationship Between Two Cascaded Converters

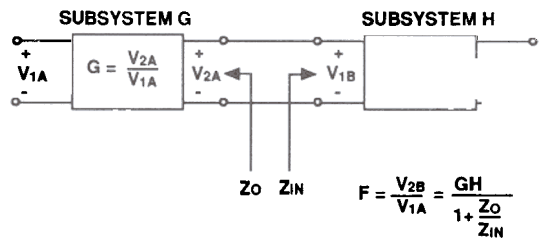


Fig 21 - Determining Phase Margins for Cascaded Impedances to Predict Stability

3. EMI Filter interaction: Most switching converters need some form of input EMI filter for noise suppression. Paralleling multiple converters, particularly when driven from a front-end processor which has its own input EMI filter, can cause undesirable interactions. A possible action to alleviate this problem is to use a two stage filter between cascaded stages as shown in Figure 22. The first stage would be common to all modules while the

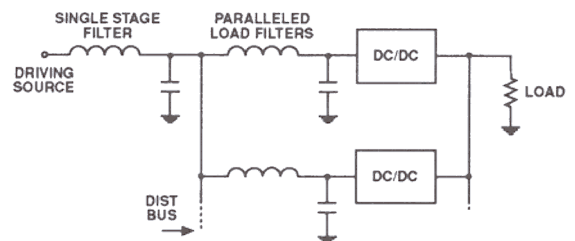


Fig 22 - Stability Enhanced with Single Source Filter Driving Paralleled Input Filters

second stage is built into each module independently. The separate secondary filters will reduce the ripple current on the distribution bus but, even then, some damping may be required to eliminate undesirable effects.

4. Switching frequency interactions: It seems prudent, although perhaps not always necessary, to synchronize the switching frequency of all the power modulators within a system. This can sometimes be difficult, as, for example, when isolation boundaries must be crossed, or where one unit is designed with a switching frequency significantly higher or lower than others within the system. Bruce Carsten^[3] recommends a phase-lock loop system which, in addition to a frequency lock, can be set up with phase shifts to prevent simultaneous switching.

Future Distributed Power Systems

With the present rapid development of all types of power processing module architectures, it seems clear that distributed power is the wave of the future for a broad range of power levels. Much has been accomplished in standardizing on bus voltage levels, improving the efficiency of the modules, and reducing their costs. Additional benefits of standardized packages, high-reliability qualified designs, and competitive vendors provide even greater emphasis that distributed power is an attractive and viable solution to the system power design problem.

References:

- [1] Jordan, Mark, "Load Share IC Simplifies Parallel Power Supply Design," *PCIM Proceedings*, September 1991.
- [2] Tabisz, Jovanic, & Lee,; "Present and Future of Distributed Power Systems," *APEC Proceedings*, February 1992.
- [3] Carsten, Bruce, "Distributed Power Systems of the Future Utilizing High Frequency Converters," *HFPC Proceedings*, April, 1987.
- [4] Clarke, Patrick, "Converter Regulation by Controlled Conduction Overlap," *U.S. Patent 3,938,024*, Feb, 1976.
- [5] Wildrick, C.M., et al, "A Systematic Procedure to Generate Load Impedance Specifications in Distributed Power Systems", *Virginia Power Electronics Center, V.P.I., Blacksburg, VA 24061*.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, license, warranty or endorsement thereof.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations and notices. Representation or reproduction of this information with alteration voids all warranties provided for an associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Resale of TI's products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Also see: [Standard Terms and Conditions of Sale for Semiconductor Products](http://www.ti.com/sc/docs/stdterms.htm). www.ti.com/sc/docs/stdterms.htm

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265