

# Controlled ON-Time, Zero Current Switched Power Factor Correction Technique

*by Bill Andreycak*

**TOPIC 3**

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Bill Andreycak

## Abstract:

A general overview of various Power Factor Correction techniques and typical application issues is first presented. Emphasis is then focused on a controlled on-time, non-resonant zero current switched (ZCS) technique. The control algorithm, design equations, required circuitry and general performance will be detailed. Experimental test results of power factor and total harmonic distortion using this approach and a Zero Voltage Switched (ZVS) derivative will be demonstrated and compared to the more conventional fixed frequency, continuous current boost PFC technique.

## Introduction

Active power factor correction techniques have become an increasingly more demanded feature in off-line industrial equipment. Legislation could soon be enacted to mandate correction of the mains current waveforms<sup>[1]</sup>. A proposed IEC 555-2 revision

specifically targets the high harmonic content of switching power supply capacitor input filters. This proposed spec defines limits for each harmonic component of the mains current, thereby requiring power factor correction circuitry. IEC 555-2 harmonic current limits are proportional to power input below 300W, but current limits are absolute above 300W. This imposes especially severe requirements on high power supplies.

When legislation such as IEC555 does not apply, it is tempting to rationalize that harmonic currents will “get lost” among the other (resistive?) loads connected to the same branch circuit. But in an industrial or office environment, it is not unusual for branch circuits to be loaded by many low power switching power supplies. Harmonic currents will add cumulatively, reducing the load capability of the single phase branch and perhaps exceeding the neutral rating of the 3-phase distribution system.

## PFC Techniques—General Overview

Power factor correction can be accomplished by any one of the numerous power conversion techniques<sup>[2,3]</sup>. The more popular methods used in the industry today incorporate the boost topology operating in the continuous conduction mode (CCM) for high power applications, or the discontinuous conduction mode (DCM) for lower output power. The boost converter output voltage (VOUT) must be

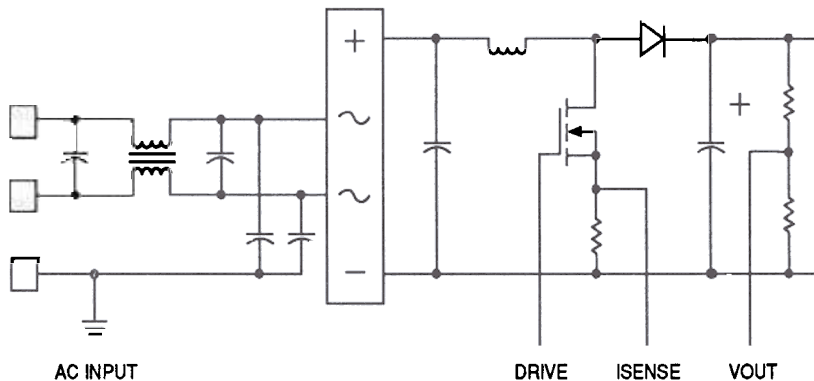
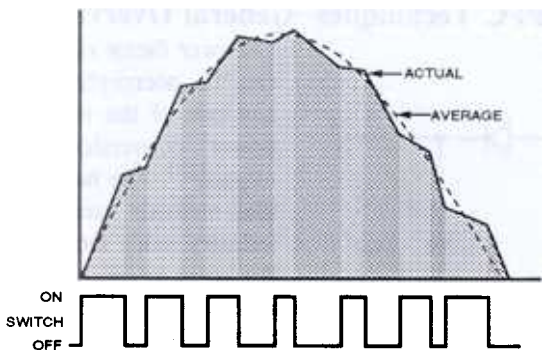


Fig 1. - Boost Preregulator for Power Factor Correction

## Zero Current Switched Power Factor Correction

greater than the peak input voltage ( $V_{IN}$ ) and non-isolated. Other conversion options include the flyback topology, a derivative of the boost converter. With this technique, the output voltage can be greater or less than the peak input voltage depending on the inductor turns ratio. Galvanic isolation can also be obtained since two coupled windings on the inductor are used in the step-up or step-down process. A simple buck regulator can be employed for a low voltage, non-isolated application with favorable results. Isolation with a buck derived topology like the forward converter can be obtained, however is more difficult due to high voltage excursions encountered to facilitate the core reset.

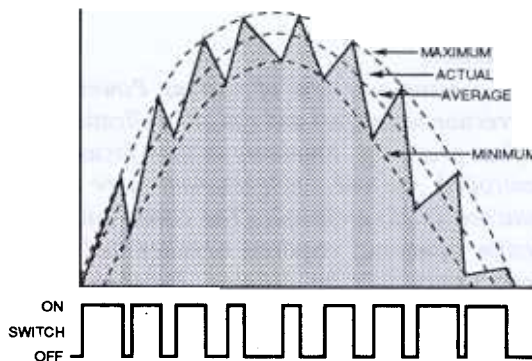
**Continuous Inductor Current Examples:** The continuous inductor current boost topology is usually operated at a fixed conversion frequency and with some form of current mode control. This somewhat "elaborate" technique requires a squarer and multiplier to correct the power factor in addition to the current mode control pulse width modulator. Although conventional "peak" current mode control can be used, adding the necessary slope compensation for stability over the wide range of duty cycles can be difficult to implement. An improved technique known as average current mode control eliminates the need for slope compensation and additionally optimizes the dynamic response of the preregulator.<sup>[4,5]</sup>



*Fig 2. - Continuous Inductor Current  
Fixed Frequency*

Another type of continuous current technique used of hysteretic current control<sup>[6]</sup>. The inductor

current is switched to follow a programmed peak and valley current level which track the sinusoidal line voltage waveshape. The associated current hysteresis band (ripple current) can be a fixed amount or proportional to the instantaneous average current. Variable frequency operation of the switch is required to accommodate the hysteresis band, which may be undesirable in applications requiring synchronization.



*Fig 3. - Hysteretic Control*

The buck regulator can also be utilized for power factor correction, but with greater distortion than the boost converter. If limited to non-isolated low voltage outputs, the buck preregulator will operate during most of the AC line period. The principal drawback to this approach is the buck preregulator quits operation each half cycle when the instantaneous line voltage falls below the output voltage. This degrades the obtainable level of power factor correction and introduces higher order harmonics. Nevertheless, the buck preregulator can be used where relatively crude power factor correction is acceptable.

**Discontinuous Inductor Current Examples:** Discontinuous operation is popular in low to moderate power level applications. Generally, either the boost or flyback topology is incorporated, controlled at either a fixed or variable frequency. Fixed frequency operation is slightly more popular today, allowing synchronization of the pre-regulator to the downstream converter. Simplification of the EMI filter design is a secondary concern. However, the penalty paid for fixed frequency operation is a resultant higher peak current in comparison to other

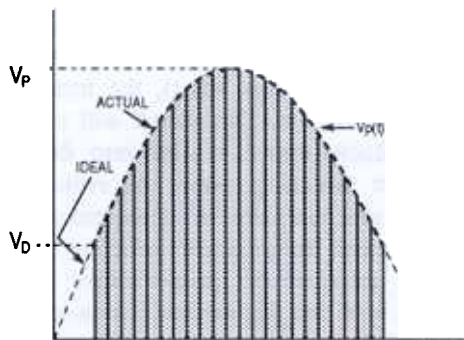


Fig 4. - Buck Preregulator Waveform

techniques. This is due to the dead-time needed at certain input voltages to remain discontinuous over all input line variations.

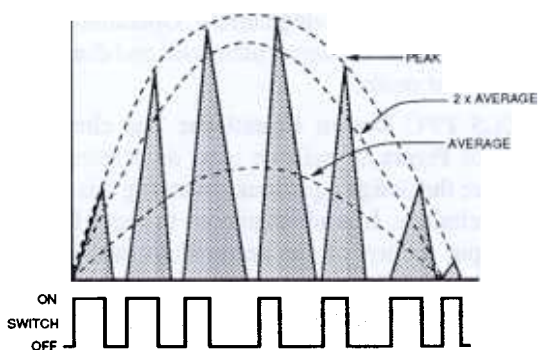


Fig 5. - Discontinuous Inductor Current Fixed Frequency

Variable frequency operation of the discontinuous conduction mode converter offers several attractive advantages over its fixed frequency counterpart.<sup>[7]</sup> First, the conversion technique can be arranged to facilitate zero current switching. In addition to low switching loss, this technique allows the switch to turn on immediately after the inductor current has reached zero. Doing so eliminates the deadband between switching cycles, thereby reducing the peak inductor current in comparison to fixed frequency operation. The converter operates just on the border between continuous and discontinuous current modes.

A controlled on-time technique can be utilized in addition to the zero current detection to program the PFC converters current demand from the AC line. The "fixed" on-time is determined by a error amplifier which monitors the preregulators output voltage and compares it to a precision reference. The amplifier loop response is rolled off at a frequency well below 20 Hertz, so the on-time can be considered "fixed" for one AC line cycle. Therefore, as the AC line voltage traverses sinusoidally from zero to its peak, so does the peak inductor current. With a fixed inductance and on-time,  $t_{ON}$ , the peak switch (hence inductor) current is automatically forced to track the input voltage. This technique can be envisioned as hysteretic current control with the lower current level set at zero. The control algorithm, cost and complexity of the control circuit are greatly simplified in comparison to other techniques.

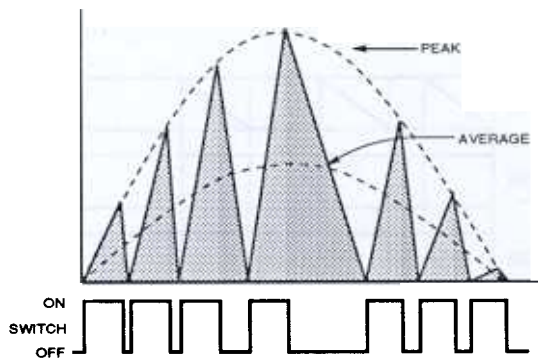


Fig 6. - Controlled ON-Time Zero Current Switched Waveforms

**Zero Current Switching:** Near unity power factor correction (>0.98) can be obtained with this controlled on-time, zero current switched (ZCS) control technique. The necessary control circuit consists of several standard pulse width modulation building blocks arranged as shown in Figure 7. Operation is similar to conventional PWM techniques with the minor difference that the zero current detection is used for retriggering of the PWM latch.

The error amplifier monitors the PFC preregulator output voltage and compares it to an accurate reference voltage on the amplifiers non-inverting input. Loop compensation is arranged such that the

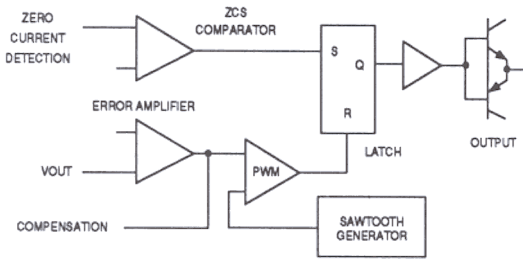


Fig 7. - Control Circuit Block Diagram

bandwidth is low (below 20 Hertz) in order to maintain a constant on-time for a given line half-cycle. The amplifier output is compared to a sawtooth waveform at the PWM comparator to create a "fixed" on-time pulse width from the analog error voltage.

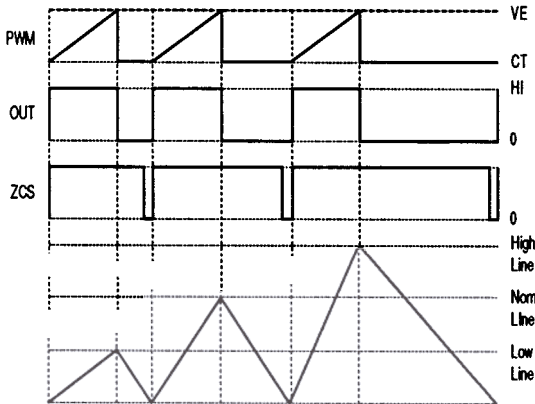


Fig 8. - Control Circuit Operational Waveforms

The output of the PWM comparator triggers a latch which drives a totem-pole output for compatibility with the boost converter MOSFET switch. The output remains high for the duration of the programmed pulse width. With the switch turned on, the boost inductor is placed across the rectified and filtered AC line voltage. The inductor (and switch) current starts out at zero and ramps linearly at the rate of  $V_{IN}/L$ . Current continues to rise during the time programmed by the PWM circuitry pulse width.

Once the proper on-time has been reached, the MOSFET switch is turned off by the ZCS control circuitry. Inductor current decays at a rate determined by  $V_{OUT}$  minus  $V_{IN}(t)$ , the instantaneous peak of line voltage. The switch will remain off until the inductor current reaches zero, the basis of zero current switching. Now, the switch can be retriggered which initiates the subsequent conversion cycle. Although zero current switching generally implies a resonant or quasi-resonant switching technique, note that this method is non-resonant.

With a "fixed" or controlled on-time, the peak inductor current is a direct function of the input voltage,  $V_{IN}$ . As the input voltage sinusoidally varies, so does the peak input current. The average input current value is exactly one-half of the peak triangular inductor current waveshape by geometric relationships. Zero current switching forces a new switching cycle to begin as soon as the old one ends for a continually flowing current. Operation is right at the borderline between continuous and discontinuous current mode.

**ZCS PFC Design Equations:** The circuit diagram of Figure 7 will be used as a reference to generate the design equations governing this conversion technique. It is advantageous to begin from the AC input section of the preregulator and advance towards the DC output.

The applied primary voltage is represented by  $V_P$ ;

$$V_P(t) = V_{PK} \sin\theta \quad (1)$$

where  $V_{PK}$  is the peak rectified line voltage ( $\sqrt{2}$  times the rms voltage).

The primary input current is defined as  $I_P$ , where  $I_{PK}$  is the peak input current.

$$I_P(t) = I_{PK} \sin\theta \quad (2)$$

The input power to the preregulator is the rms component of the line voltage multiplied by the line current, or:

$$P_{IN} = \frac{V_P I_P}{\sqrt{2} \sqrt{2}} = \frac{V_P I_P}{2} \quad (3)$$

The average (DC) output current ( $I_{OUT}$ ) is determined by dividing the output power ( $P_{OUT}$ ) by the



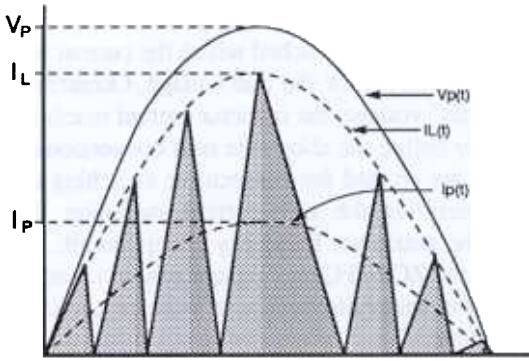


Fig 9. - ZCS Switch Waveforms

specified output voltage ( $V_{OUT}$ ).

$$P_{OUT} = V_{OUT} I_{OUT} \quad (4)$$

The input power can now be equated to the output power with an assumption that the conversion efficiency is very high (>95%).

$$P_{IN} \cong P_{OUT} \quad (4A)$$

$$P_{OUT} = \frac{V_P I_P}{2} \quad (5)$$

Solving for the peak input current,  $I_P$ :

$$I_P = \frac{2 P_{OUT}}{V_P} \quad (5A)$$

It has already been demonstrated that the peak inductor current is twice that of its average primary current for this ZCS/PFC conversion technique.

Therefore, the peak inductor current  $I_{L(pk)}$ :

$$I_{L(pk)} = 2 I_P \quad (6)$$

Substituting equation 5A for  $I_P$ :

$$I_{L(pk)} = \frac{4 P_{OUT}}{V_P} \quad (6A)$$

In its time variant form:

$$I_{L(t)} = 4 \frac{P_{OUT} \sin \theta}{V_P}$$

The inductor current can now be analyzed over changing line and load conditions.

**Timing Intervals:** Using the previously derived inductor current equation in (6B), the preregulator switch ON and OFF times can be calculated. Starting with the general inductor waveform relationships and working specifically towards this PFC example:

$$\frac{V}{L} = \frac{dI}{dT} \quad (7)$$

In steady state, closed loop operation, the required on time is defined by:

$$t_{ON} = \frac{I_L L}{V_P} \quad (7A)$$

Inserting equation 6A for  $I_L$  results in:

$$t_{ON} = \frac{4 P_{out} L}{V_P^2} \quad (7B)$$

where  $L$  is the inductor value in Henries.

The instantaneous off time can be derived by substituting the inductor voltage during its discharge ( $V_{OUT} - V_{IN}$ ) for voltage in equation 7.

$$t_{OFF} = \frac{I_{L(t)} L}{V_{OUT} - V_{P(t)}} \quad (8)$$

which expands to the form of :

$$t_{OFF} = \frac{4 P_{OUT} L \sin \theta}{V_P (V_{OUT} - V_P \sin \theta)} \quad (8A)$$

The switching period is obtained by combining the results of equations 7B and 8A.

$$t = 4 P_{OUT} L \left( \frac{1}{V_P^2} + \frac{\sin \theta}{V_P (V_{OUT} - V_P \sin \theta)} \right) \quad (9)$$

## Control Time Summary

**ON Time:** The on time ( $t_{ON}$ ) should be considered as constant for any one line cycle. The voltage (error) amplifier which controls the on time is rolled off at a very low frequency, typically below 20 Hertz to enforce this. As with most conventional converters, the on time is at its maximum under the conditions of low line and full load. Conversely,  $t_{ON}$  is at its minimum at high line when operating at the lowest output power.

|          |                      |                          |
|----------|----------------------|--------------------------|
| $t_{ON}$ | $\frac{V_P}{V_{IN}}$ | $\frac{I_{OUT}}{I_{IN}}$ |
| min      | max                  | min                      |
| max      | min                  | max                      |

**OFF Time** is directly determined by the flyback voltage across inductor as it discharges,  $V_{OUT}-V_{IN}$ . As the AC line voltage goes to zero the corresponding flyback voltage is at its maximum,  $V_{OUT}$ . The time required to discharge the inductor ( $t_{OFF}$ ) is then at its minimum.

$t_{OFF(min)}$  occurs at  $V_{P(t)} = 0$

As the instantaneous line voltage reaches its peak (each line cycle), the inductor reset (flyback) voltage is at its minimum, since  $(V_{OUT}-V_{IN})$  is small. This determines the maximum off time required to get the inductor current back to zero.

$t_{OFF(max)}$  occurs as  $V_{P(t)} = V_P$

**Conversion Period:** Both the switch on and off times should be calculated over all line and load conditions to determine the minimum and maximum conversion intervals. Before doing so, an examination of the interval near zero crossings of the line voltage will be presented.

**Maximum Frequency:** In some applications, its more advantageous to limit the maximum conversion frequency than to perfectly track the line voltage completely to zero. Doing so could result in wide range of conversion frequencies which approach a minimum period equal to the controlled on-time. As the line voltage nears zero the inductor reset voltage reaches its maximum of  $V_{OUT}$ . This corresponds to the control circuits minimum off-time, and also, the maximum conversion frequency.

Programming a maximum frequency via clamp circuitry is an alternative to operating at otherwise

higher frequencies as called for by the zero current detection circuitry. The consequence is that a point in the AC cycle is reached where the current will no longer ideally track the line voltage. Occurring at a "dropout" voltage, the inductor current reaches zero slightly before the allowable next conversion cycle. Voids are created the consecutive switching cycles by overriding the zero current switching feature with the maximum frequency clamp circuit. At this point, the ZCS/PFC technique starts to resemble the fixed frequency discontinuous inductor current PFC technique.

An interesting subtlety of this technique occurs when the "dropout" point is reached. First, as the AC line tails off to zero, the power being processed is only a small fraction of the total. If unity correction is not obtained during this region it has minimal effects on the overall power factor. A reasonable dropout voltage can be determined to minimize the frequency span without compromising high power factor. "Dropping out" in the neighborhood of ten to twenty volts (AC) will still achieve excellent results. While this does introduce minor amounts of distortion, better results are achieved than with the buck regulator which completely turns off.

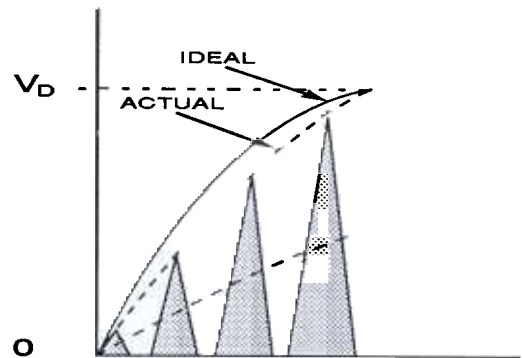


Fig 10. - Input Current at Dropout

## Controlled On-Time, Zero Current Switched 175w Application

The controlled on-time, zero current switched power factor correction technique will now be used in a 175 Watt industrial lighting application. A standard commercial mercury vapor lamp housing containing an electronic ballast drive circuit was obtained for development. This switchmode ballast design utilizes a DC bus which is obtained by rectifying the AC line input and filtering it with a high voltage electrolytic capacitor. Most switching power supplies incorporate the same type of circuitry. Therefore, although the ZCS/PFC technique will be evaluated in a lamp housing, it is equally applicable to switchmode power supplies.

Normally, the mercury vapor lamp will draw a fixed amount of power from the AC input with no dynamic load changes as in a power supply application. The only unusual characteristic of this lighting example involves the startup property of the lamp. During its initial "warm-up" period (which lasts several minutes) the bulb draws less power than its nominal value. Initially, about 65W is required which gradually increases to the final power level of 175W. The PFC preregulator will be designed to accommodate the full power range of 65W to 190W.

A suitable conversion frequency range needs to be selected. The converter should operate above the audible range, yet not too high where efficiency would be impaired. Conversely, the inductor volume shrinks significantly with increasing frequency, and numerous acceptable solutions are possible depend-

ing on size, cost and efficiency differentials. For this design, a lower frequency limit of 30kHz was agreed upon, which would only occur during the bulbs warm-up. In normal operation at 175 Watts, the converter will operate in the 50 - 200kHz span. Once the dropout voltage has been selected and input/output specification listed, a family of curves displaying  $t_{ON}$ ,  $t_{OFF}$  and  $t_{PERIOD}$  can be generated over the full operating ranges. For this example, a dropout voltage of 15VAC has been selected and the following specifications will be used for this 175 Watt lighting application.

### Preregulator Specifications:

$$V_{IN} = 100 \text{ to } 130 \text{ VAC}$$

$$P_{OUT} = 65 \text{ to } 190 \text{ Watts}$$

$$V_{OUT} = 320 \text{ VDC } \pm 5\% \text{ (nominal)}$$

$$F_{CONV(min)} = 30\text{kHz at } P_{OUT} = 65\text{W}$$

Given these specifications, the design equations were used to calculate the inductor value of 200 $\mu$ H. Note that the inductor is designed to withstand only the high frequency switching current, and not the rectified line frequency as with a continuous conduction mode converter. The ZCS technique minimizes inductor volume as the core is completely reset upon completion of each switching cycle.

A computer program written in BASIC language was developed using the equations previously given to simplify the task of calculating the ranges of on, off and conversion period times. These values are useful for optimal programming of the sawtooth generator and maximum frequency clamp circuit. The results of conversion frequency versus instantaneous line voltage are shown in Figure 12. Displayed are conversion frequency for normal operation at an output power of 175 Watts for three line input voltages of 100, 115 and 130 Volts.

An experimental prototype using the Zero Current Switched, controlled on-time technique was constructed to correct the power factor of the 175 Watt Mercury vapor lamp and ballast. First, Figure 13 displays the uncorrected input current waveform which resulted in a typical power factor of 0.62, far

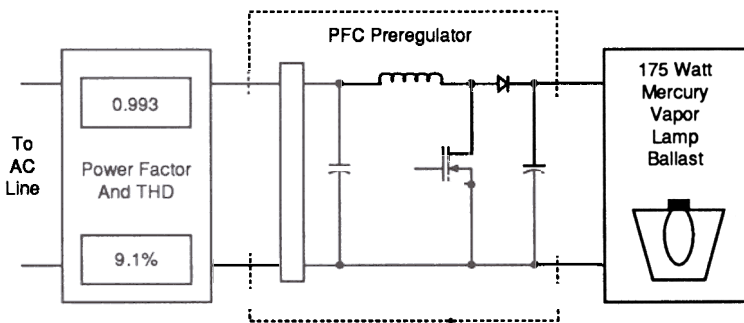


Fig 11. 175W ZCS/PFC Circuit Diagram



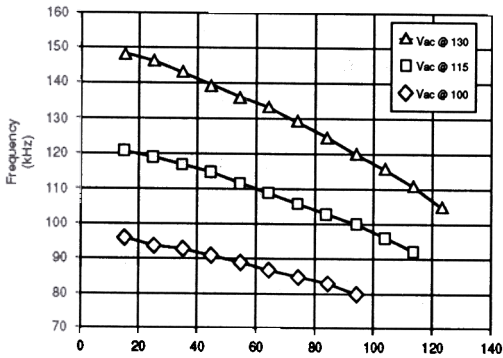


Fig 12. - Conversion Freq. vs. Inst. Line Voltage

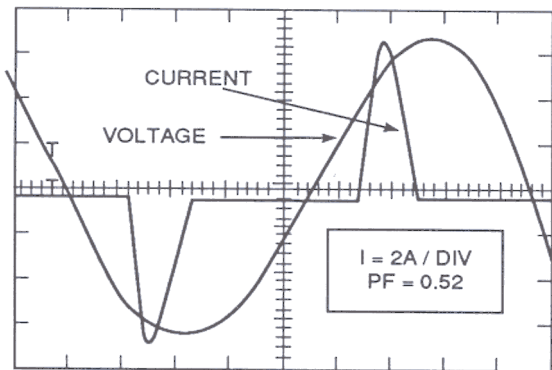


Fig 13. - Input Current - Uncorrected

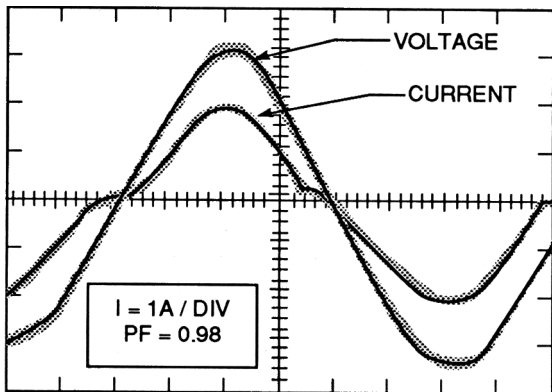


Fig 14. - Input Current - Corrected

from ideal. The ZCS/PFC converter breadboard delivered a typical full load power factor of 0.991 as demonstrated in Figure 14.

**Zero Voltage Switching:** The unique properties of this application warrant the investigation of methods to facilitate zero voltage switching and further enhance efficiency. Zero current switching has reduced the switching loss at turn-on. Since no current is flowing, there is no power lost due to the overlap of switch voltage and current. However, the MOSFET output capacitance ( $C_{OSS}$ ) is charged to  $V_{OUT}$  at the instant that zero current is reached and must be discharged at turn-on.<sup>[8,9]</sup> This results in an unnecessary waste of power which can be quantified as:

$$P_{COSS} = \frac{1}{2} C_{OSS} V_{OUT}^2 F_{CONV} \quad (10)$$

A typical application might incorporate a 400V, 0.5 Ohm ( $R_{DS}$ ) FET, perhaps an IRF740 or its equivalent. Similar size geometry devices exhibit  $C_{OSS}$  figures in the neighborhood of 200pF. For the sake of simplicity, a switching frequency of 100kHz will be used in equation 10 to calculate the  $C_{OSS}$  power loss. A little over one Watt is lost in the conversion process, due entirely to the discharging of the MOSFET output capacitance. Zero voltage switching is a relatively new technique which eliminates this  $C_{OSS}$  loss contribution. A quasi-resonant L/C tank circuit will be formed which resonantly brings the voltage across the switch ( $V_{DS}$ ) to zero at the conclusion of the switching cycle, thus eliminating  $C_{OSS}$  loss.

**ZVS Design Considerations:** A vast majority of the zero voltage switching converter research and development has been with continuous inductor current designs. Although somewhat disguised by its name, zero voltage switching is caused by an initial current flowing through a resonant L/C tank circuit. Current is the stimulus. Typically this is the load current flowing in the switch while its on, which is later diverted to the shunting resonant capacitor at turn off.

In the discontinuous current mode, the load current is zero at the time when this resonance should occur, eliminating the traditional ZVS stimulus. Further complicating matters, the typical output voltage of the boost preregulator is only slightly greater than the peak input voltage. This

generally makes it easier to retrofit into existing power supply designs since the bulk voltage is only slightly above what it was at high line. With this set of conditions—where  $V_{OUT}$  approaches the peak input voltage—zero voltage switching cannot be facilitated with a minor modification to the zero current switching PFC technique.

However, zero voltage switching can be added to the ZCS/PFC circuit—under certain conditions. Provided that  $V_{OUT}$  is at least twice instantaneous input voltage, enough stimulus is developed in the resonant tank to force ZVS to occur. Consider the circuit shown in Figure 15. When  $V_{OUT}$  is greater than twice  $V_{IN}$ , the voltage across the inductor (when the current goes to zero) is  $V_{OUT} - V_{IN}$ , which is greater than  $V_{IN}$ . This circuit will resonate about  $V_{IN}$  with an amplitude of  $(V_{OUT} - V_{IN})$  which has been designed to be greater than  $V_{IN}$  itself. The L/C tank will resonate down to zero volts and try to go negative if left unattended. The zero detection comparator will be fed the switch voltage waveform instead of the inductor current to modify the technique for zero voltage instead of zero current switching.

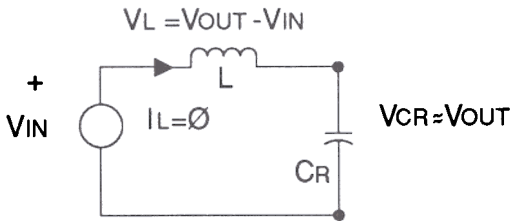


Fig 15. - ZVS Boost Diagram

To accommodate this ZVS arrangement, a specific deadtime must be inserted between the ZCS detect and turn on of the output. This delay allows resonance to position the switch correctly with zero voltage across it, facilitating lossless turn on. This intentional off time between pulses does slightly modify the control algorithm and peak to average inductor current ratio. However, when the additional off time is kept small in comparison to the overall switching period it introduces a negligible error. The slight "rounding off" of the current waveform may

also be beneficial in lowering the EMI/RFI noise generated.

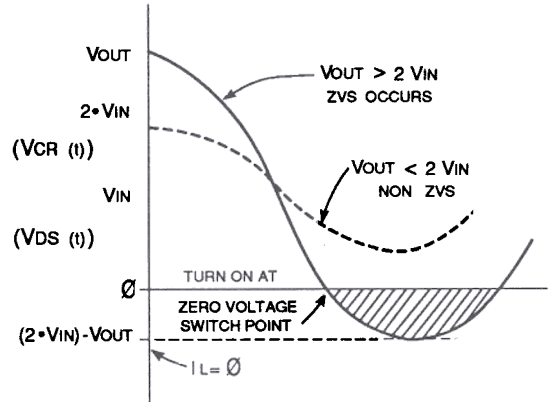


Fig 16. - ZVS Resonant Capacitor Waveform

Therefore, in the zero current switched, discontinuous inductor current PFC technique, zero voltage switching will occur whenever  $V_{OUT}$  is greater than twice that of  $V_{IN}$ . In this 110VAC input application, the output voltage requirement of 320VDC makes it a likely candidate for adaptation of zero voltage switching.

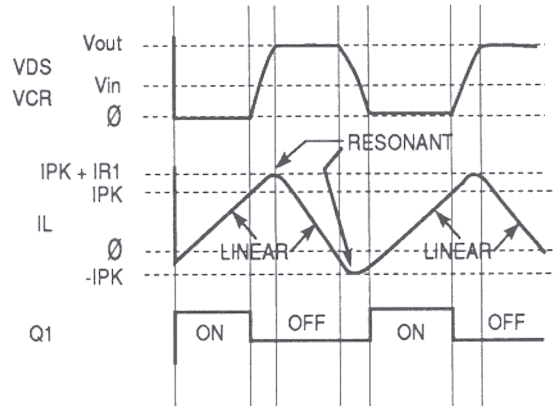


Fig 17. - ZVS Boost Waveforms

The MOSFET output capacitance ( $C_{oss}$ ) can be used as the resonant capacitor or shunted with an external capacitor to alter the resonant timing period. For this experiment, a 2nF capacitor was added. This neatly accommodated the actual delay of the circuit breadboard between the actual ZCS

detect comparator and turn-on of the switch. This was also enough capacitance to divert current from the switch to the resonant capacitor at turn-off, thus reducing the corresponding FET losses.

**Test Results:** Three different power factor correction preregulators were constructed and tested at 175 Watts. The first model utilized the UC3854 PFC controller and used continuous inductor current as shown in Figure 2 and average current mode control. This would serve as a reference for comparison to the other approaches. A second unit was built to facilitate the zero current switched, controlled on-time technique. Last, an identical unit to this was modified to perform zero voltage switching by adding a resonant capacitor across the main switch and altering the zero detection circuit input. Each of these units was tested for power factor, and harmonic distortion components (to the 40th harmonic) at 115 VAC. No EMI/RFI filter was used, however all used a 1uF filter capacitor after the AC input bridge rectifiers.

Table 1 - PFC TECHNIQUES - COMPARISON AT 175W

| PFC Technique                              | UC3854 Fixed Frequency | Zero Current Switched | Zero Voltage Switched | Uncorrected Ballast (no PFC) |
|--|------------------------|-----------------------|-----------------------|------------------------------|
| Power Factor                               | 0.999                  | 0.993                 | 0.987                 | 0.629                        |
| T.H.D.                                     | 3.81%                  | 9.1%                  | 15.5%                 | 113.5%                       |
| <b>CURRENT ANALYSIS</b>                    |                        |                       |                       |                              |
| Fundamental                                | 1.523A                 | 1.516A                | 1.511A                | 2.371 A                      |
| Harmonics (as a percentage of fundamental) |                        |                       |                       |                              |
| 3rd  | 1.67%                  | 7.72%                 | 13.3%                 | 84.5%                        |
| 5th  | 2.10%                  | 2.4%                  | 10.8%                 | 62.5%                        |
| 7th  | 0.57%                  | 2.8%                  | 3.9%                  | 36.4%                        |
| 9th  | 1.26%                  | 3.13%                 | 0.7%                  | 15.5%                        |
| 11th                                       | 0.98%                  | 1.2%                  | 1.4%                  | 1.71%                        |
| 13th                                       | 1.55%                  | 1.1%                  | 1.4%                  | 4.03%                        |

## Conclusions

The controlled on time, zero current switched PFC technique is applicable to numerous low power applications and offers promising results. Additionally, the inherent simplicity of this technique is also attractive, luring the attention from cost sensitive industries, such as the under 300 watt power supply and even industrial lighting manufacturers. Experimental laboratory results demonstrate an obtainable power factor in excess of 0.99 at a power levels of 175 Watts in an typical application. Finally, with proper selection of output voltage, based on the input AC mains, the conversion technique can be expanded to exhibit lossless Zero Voltage Switching of the PFC preregulator switch. The continuation of research and development in low cost power conversion solutions will overcome the challenges of obtaining high performance in a variety of low power and cost sensitive applications.

## Acknowledgements

The author acknowledges and appreciates the use of:

Voltech PM3000 power analyzer,  
Valhalla Scientific PFC meter and  
Lights of America 175W lamp housing.

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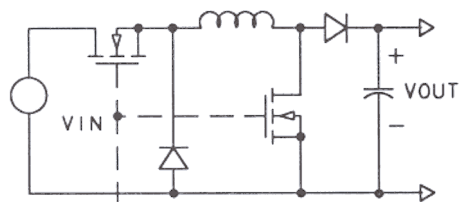
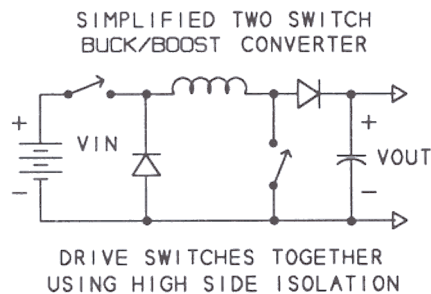
## Addendum -- PFC Low Voltage Outputs

One problem with many power factor applications is that the AC input voltage is both above and below the optimal voltage of the preregulator output bus rail. Some examples of these are the 28, 48 and 160 - 270VDC "standard" rails. The boost and buck converters are generally discarded in favor of the flyback (buck/boost) topology. The inductor windings can be arranged for either a step-up or step-down input to output voltage conversion. Most of

the PFC techniques shown in the beginning of this paper are equally applicable to the flyback topology.

The main drawback to the single switch version of this approach is the high voltage across the transistor switch during reset. This is a result of operating over a wide duty cycle range to achieve line current correction. The transformer flyback voltage adds to the input voltage across the switch creating a very high potential as the inductor discharges. This may exclude the use of today's MOSFETs for several reasons, but emerging IGBT transistors offer attractive possibilities since they can handle both the high peak voltage and current at moderate cost. Other concerns like safety agency isolation spacing, EMI/RFI, and efficiency all pooled together might make this switching technique seem unattractive from a practical standpoint.

One way to avoid the high voltage problem is to use a two switch flyback converter design as shown below. Although this adds another MOSFET switch and isolated gate drive, the high reset voltage is eliminated. Clamped across the input terminals, the peak transistor voltages can never exceed  $V_{IN}$ . Either continuous or discontinuous inductor current operation can be employed, as with all flybacks. More experimentation can result in zero voltage switched quasi-resonant adaptations.



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