1 MHz 150 W Resonant Converter Design Review

by Bill Andreycak

TOPIC 2

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Abstract:

This paper is intended to explore in significant detail the intricacies of the quasi-resonant half bridge topology. Voltage and current waveforms and transferred charge and energy will be analyzed as functions of time and input/output conditions. Specific and generalized design equations are given, which are also applicable to other topologies by those skilled in modern power supply design.

Introduction:

The pioneers of resonant mode power conversion have generated a tremendous amount of interest in this new and emerging technology and approach to power conversion. Expectations of lossless switching and multi-megahertz operation are rapidly approaching realization. Given this recent stimulus, a new control IC, the UC3860, has been introduced for controlling many of the various resonant and quasi-resonant design approaches.

Despite the differences among the numerous resonant and quasi-resonant switching topologies, all have one common denominator -- the need for a high speed, complete and versatile resonant mode control IC. The ideal candidate would incorporate modular functions or building blocks that could be easily configured by the user to control various circuit topologies and implementations.

This paper will show one application of this resonant control IC in a typical power supply design example. Described in the text is a 150 watt off-line converter switching at a maximum frequency of 1 megaHertz. This results in an effective 500 kiloHertz utilization of the main transformer. Delivering 15 volts at 10 amperes of load current, it operates from a 110/220 AC input, or from a 220 to 370 V dc bus at high efficiency.

Design Specifications:

An off-line 150 watt, single output design has been selected as a typical application for the purposes of this paper. Several items common to most designs will not be highlighted, for example, primary to secondary isolation and input filter calculations. However, this discussion will concentrate on relevant calculations and new material regarding the quasi-resonant converter.

Input Voltage:
(110 VAC) : 85 -- 132 VAC
(220 VAC) : 170 -- 265 VAC
(DC Input) : 220 -- 375 VDC

AC Line Frequency: 50 Hz min

Output Voltage: 15 VDC

Output Current: 2.5 -- 10 Amps

Line Regulation: 15 mV

Load Regulation: 15 mV

Output Ripple: 100 mV p-p, dc-20 MHz
Efficiency: 85 % at full load

Quasi-resonant Circuit Operation

The quasi-resonant Buck regulator circuit shown in Fig. 1 is applicable to high frequency power conversion systems and will be described in detail. Initial conditions are given with the switch Q open, and no current flowing from the input source V. The resonant current I_r is zero, and no voltage is across either of the resonant components L_r or C_r. There is an output current I_{out} and voltage V_{out} delivered entirely by the output filter components L_o, C_o and D_o. For the purposes of this model, assume that each component is ideal.

Switch Q is closed at time t_0 applying voltage V_{IN} across the circuit input. The input current I_{in} begins at zero and rises linearly at the rate of V_{IN}/L_r until it reaches output current I_{out}.

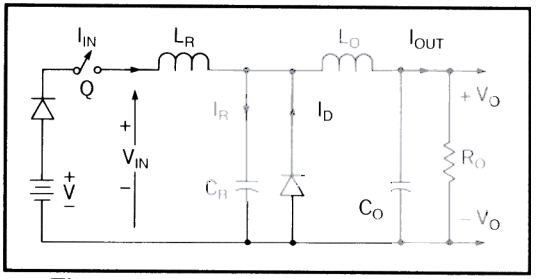

Fig. 1 - Quasi-Resonant Buck Regulator

Simultaneously, the output diode current I_d which began at I_{out} linearly decreases to zero. At this point, the input power source is supplying the full output current I_{out}. This occurs at time t_1 which will vary linearly with I_{out} and V_{IN}. During the interval between t_0 and t_1, no resonant current I_r flows in capacitor C_r.

Beginning at t_1 the resonant circuit current component I_r sinusoidally flows through C_r. This adds to the output current, making the input current the summation of both. Peak input current occurs at $t_1 + \pi/(2\omega)$. It later intersects the I_{out} level at t_2, corresponding to $t_1 + \pi/\omega$.

The sinusoidal input current continues until t_3 where it reaches zero. Here, the switch is opened and turn-off is initiated at *zero current* which facilitates lossless switching. Since t_1 varies with I_{out} and V_{IN}, the zero current switch point t_3 varies also with these changing parameters.

A zero current detection circuit can be used to facilitate turn-off at precisely zero current. Another technique utilizes a fixed *on* time at the primary switches. This time constant is set above the maximum required *on* time of the resonant network over all line and load combinations. While this technique is easier to implement, it may compromise overall design at the maximum conversion frequency. The inability to switch consecutively at maximum rate hurts transformer turns ratio optimization. Higher currents will result due to the lower turns ratio, degrading overall efficiency at all frequencies.

During the interval between t_3 and t_4, C_r discharges, providing a constant current I_{out} to the load. The capacitor voltage decreases linearly, reaching zero at t_4.

The output filter section releases its stored energy between t_4 and t_5. The conversion period ends at t_5, which corresponds to the beginning of the next cycle, t_0. A detailed analysis of the voltages and currents during each interval is provided in the Appendix.

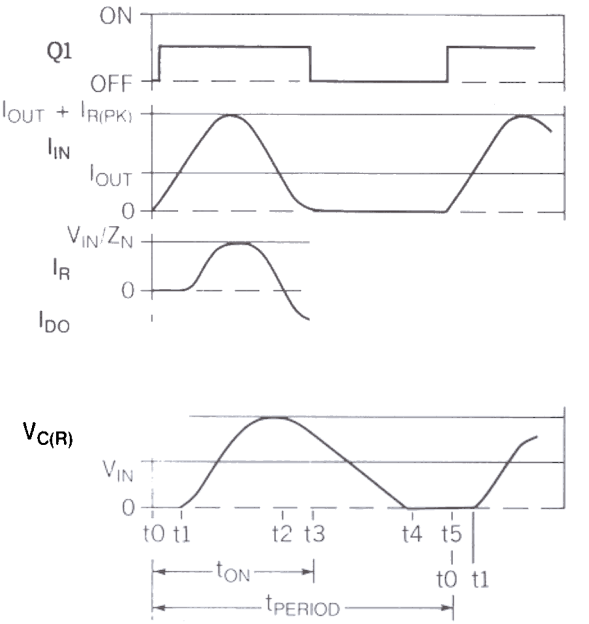

Fig. 2 - Quasi-Resonant Waveforms

Quasi-Resonant Half Bridge -- Topology Fundamentals and Overview

The general circuit diagram for a quasi-resonant half bridge converter using secondary side resonance is shown in Fig. 3. The resonant half bridge portion and its associated waveforms are shown in Figs. 4 and 5.

Transistors Q_1 and Q_2 are alternately driven from the control circuitry at a repetition rate, or frequency determined by the error voltage.

Q_1 turns on, connecting the transformer primary across capacitor C_1 with voltage $V_{IN}/2$. This rectangular voltage waveform is divided by the turns ratio N (N_{pri}/N_{sec}) and coupled to the secondary side(s) of the transformer. Diode D_1 is forward biased, and secondary current I_{sec} flows through L_{r1} and D_1. This can be expressed as two individual components, the "constant" output current I_{out} and the sinusoidal current I_r through C_r. During this interval, D2 is reversed biased and is essentially out of the picture.

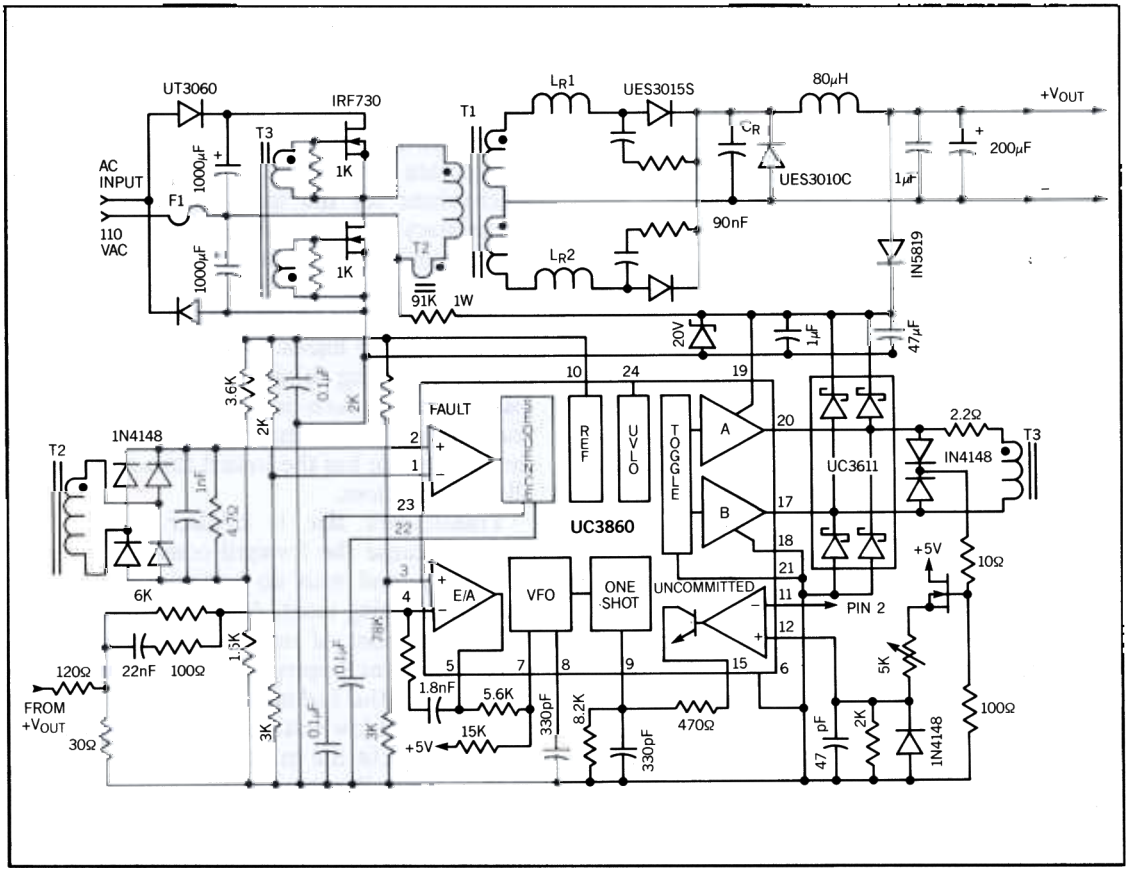

Fig. 3 - 150 Watt Off-Line Quasi-Resonant Half Bridge

The secondary current starts at zero at time t_0 and ramps up linearly, reaching I_{out} at t_1. I_{sec} then becomes sinusoidal, peaks at $I_{sec(peak)}$, and intersects the output current again at t_2. At t_3, zero current is reached sinusoidally and Q_1 is turned off.

Peak voltage across C_r occurs at t_2 and diminishes during the remainder of the interval ending at t_5. When the voltage across C_r reaches zero, all of its stored charge has been transferred to the output load, thus completing the conversion cycle. This process is repeated for transistor Q_2, resulting in similar operation.

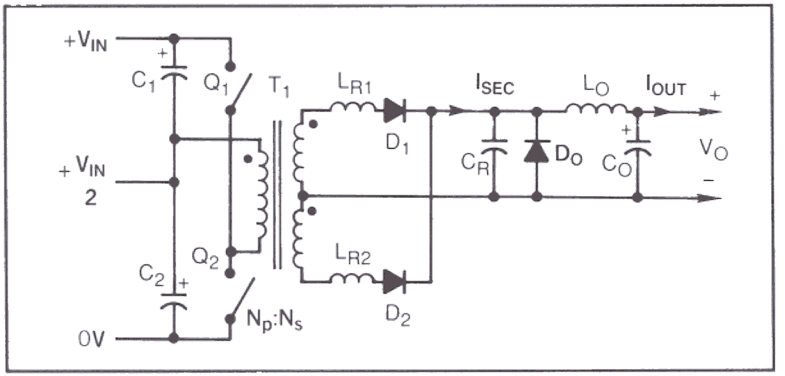

Fig. 4 - Quasi-Resonant Half Bridge

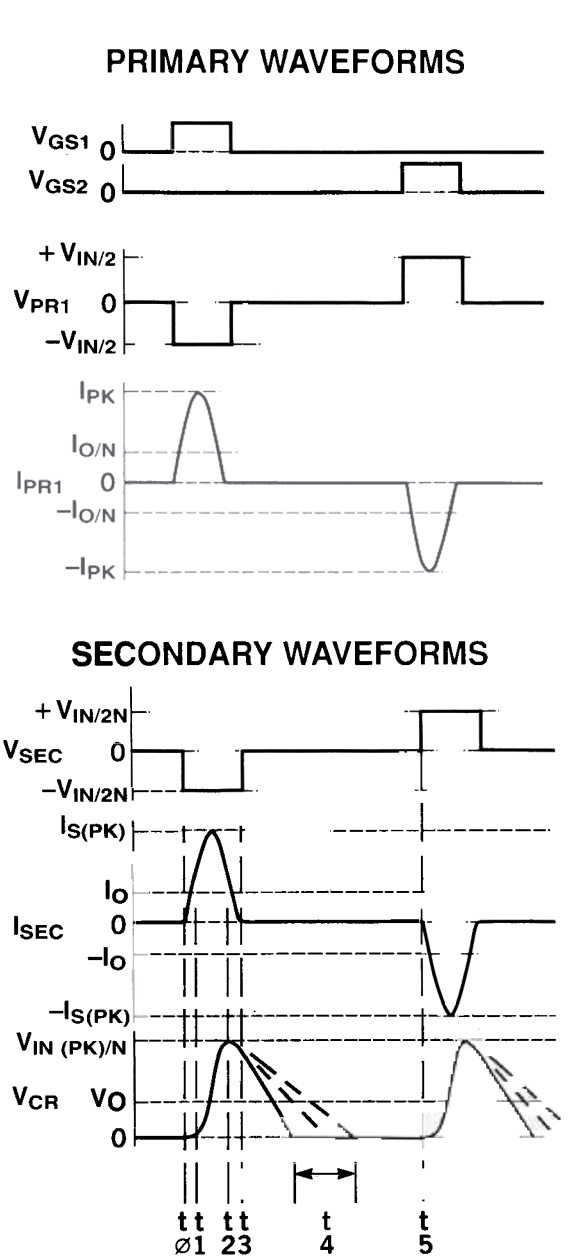

Fig. 5 - Primary and Secondary Waveforms

Half Bridge Advantages and Alternatives

The thrust towards resonant mode power supply designs has been fueled by the demands for higher power densities and high overall efficiency. Although several basic topologies deserve consideration in this off-line application, the Half Bridge configuration offers many key advantages.

Unlike the single-ended forward converters, the half bridge provides bidirectional utilization of the transformer. This eliminates the need to incorporate dissipative or complex flux reset mechanisms for the main transformer. Also, the primary switched voltage is one-half that of its single ended or full-bridge counterpart, halving the transistor voltage rating requirements.

In addition, the reduced voltage significantly reduces turn-on losses. Bear in mind that zero current switching minimizes *only* the turn-off losses. During turn-on, however, the current rises linearly before resonance commences, and the half bridge has the lowest turn-on losses of all configurations.

Transformer size is smaller for the half bridge because the forward converter "wastes" half the period with no power transfer while the core is being reset. Also, all windings have half the number of turns compared to a forward converter approach. This could significantly lower the leakage inductance in certain designs where low voltage, high current designs stand to benefit the most.

Half Wave Resonance: The half-wave resonant mode of operation facilitates a unidirectional current flow from the primary to the secondary. The major advantages of this can be seen near the primary switches. When a reverse current flows through the Mosfet, its parasitic drain-body diode conducts, exhibiting slow reverse recovery characteristics. To prevent this, the reverse current is generally directed to an external fast recovery diode that shunts the Mosfet. A Schottky diode must be added in series with the Mosfet to guarantee that the external diode will conduct. This "elaborate" network is not lossless, and can significantly impact the power supply overall efficiency.

Secondary side half wave resonance eliminates the need for these components. Reverse current flow is restricted on the secondary side of the transformer by the series rectifiers. Serving a dual purpose, these diodes isolate the resonant tank from the primary in addition to rectifying the secondary waveform.

Full wave designs return excess tank energy back to the primary, and require bidirectional

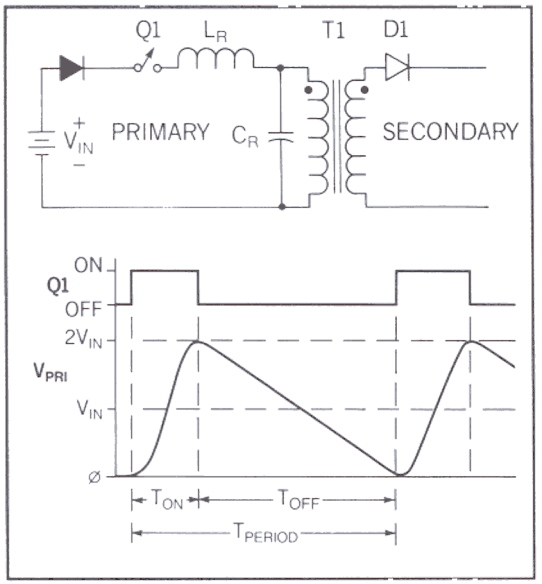

Fig. 6 - Primary Side Half Wave Resonance

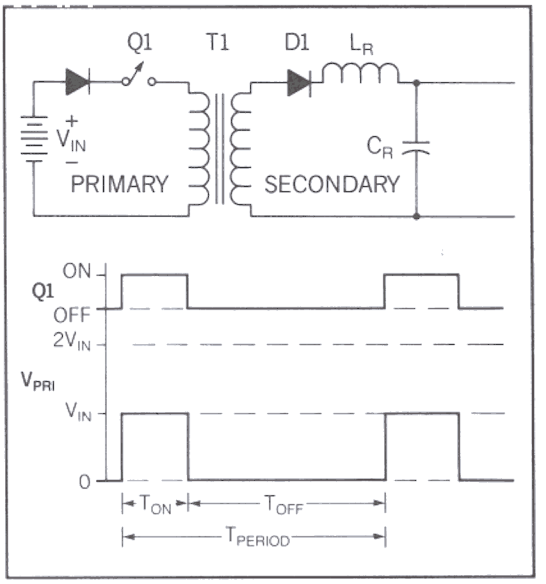

Fig. 7 - Secondary Side Half Wave Resonance

switches on the primary. One merit, however, is that the switching frequency range is fairly narrow over various line and load combinations. On the other hand, the half wave resonant approach must span a fairly wide range of switching frequencies to maintain regulation for the same input and output variations, since all resonant tank energy must be delivered to the output.

Secondary Side Resonance: Secondary side resonance helps minimize transformer size. With the resonant capacitor located on the transformer secondary side, the volt-second product depends only on the input voltage and transistor *on* time. During the remainder of the period, or *off* time, the transformer is not supporting the resonant capacitor discharge. Lower core losses are attained with this configuration, and are easier to analyze. The waveform is rectangular and is a function of input voltage, *on* time and switching frequency.

Resonant Control Circuit

Refer to the simplified block diagram and waveforms of Fig. 8.

Error amplifier: The error amplifier is used to generate an output voltage proportional to the error between the amplifier inputs. A precision reference voltage is at the noninverting input, while the power supply output voltage is applied to the inverting input. The difference between the two is amplified and will respond to millivolt changes in power supply output voltage, providing tight regulation. The error amplifier output is high when the supply output voltage falls below its setpoint, and a low amplifier output indicates the output voltage is higher than ideal. This variable error amplifier output voltage indicates the need for correction to maintain regulation.

Variable frequency oscillator: This device converts a variable input voltage to a variable frequency output pulse train. Increasing input voltage yields an increase in the frequency of the output pulses. Regulation of the output voltage is thus obtained over various line and load combinations by varying the switching (conversion) frequency. The VFO is driven by the error amplifier output voltage and is used to trigger the one-shot pulse generator.

One shot pulse generator: This module generates an accurate pulse width, or duration corresponding to the *on* time required for the resonant tank circuit switches. In fixed *on* time quasi-resonant applications this time constant is set slightly longer than one-half of the full resonant period. Another approach utilizes zero current switching (ZCS) which turns off the switches at zero current. In this application, the one shot is programmed for the maximum circuit on-time and modulated to facilitate ZCS.

Toggle flip flop and gating circuitry: Alternating outputs for "bridge" applications require a toggle flip-flop to divide the VFO frequency by two. This provides out-of-phase drive signals to each of the resonant switches with the proper on-time. In single ended applications like the Buck, Forward and Fly-back topologies, a toggle function is not used.

High power Mosfet drivers: High peak gate currents are required to deliver sharp Mosfet turn-on and turn-off transitions. The driver accepts low power (TTL) logic inputs and delivers high power (1 to 3 amp peak) Mosfet gate drive compatible outputs.

Zero current switching circuitry: Primary current is monitored and used to turn off the one shot–hence the outputs–when zero current is crossed. This minimizes the switching losses in the primary switches.

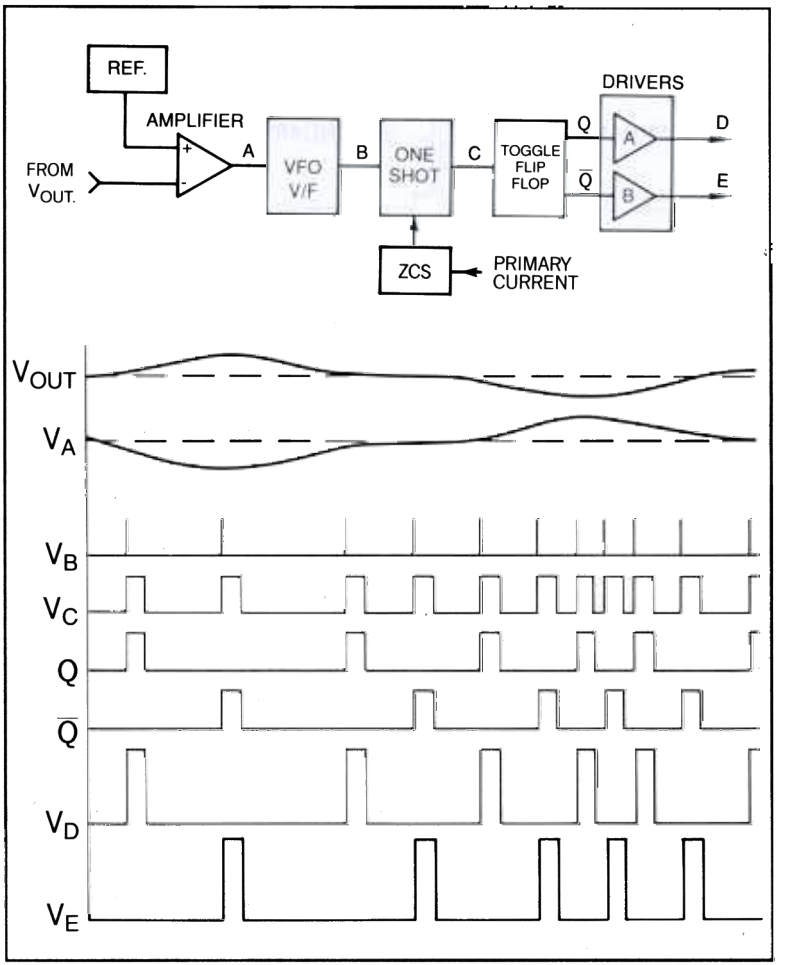

Fig. 8 - Control Circuit Fundamentals

Quasi-Resonant Circuit Limitations

One obvious circuit constraint is that the peak resonant current component I_r *must* be greater than I_{out}. Otherwise, zero current will not be reached as shown in the figure below. This relationship specifies the limits of V_{IN} and I_{out} of the resonant tank as a function of the L_r–C_r resonant tank characteristic impedance, Z_r.

Increasing the resonant current component far above I_{out} max is one solution, but an inefficient one. The primary switch losses vary with primary current squared, and techniques to minimize this current are required.

The ideal ratio of the output current I_{out} to the minimum resonant peak current $I_{r(pk)}$ min is unity. This insures resonance at all loads while preventing excessively high peak resonant tank currents and losses. The resonant component initial tolerances and temperature variations need to be analyzed and accommodated by adjusting the ratio of $I_{out\ max}$ to $I_{r(pk)}$. A twenty-five percent safety margin is used in this

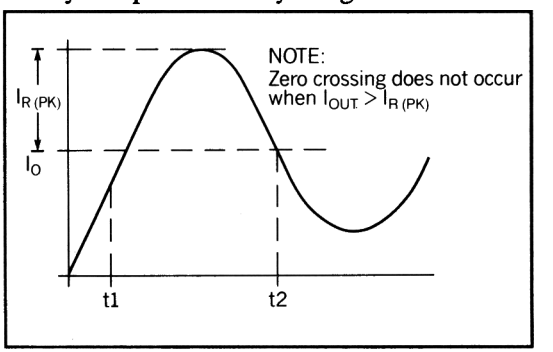

Fig. 9 - Input Current - No Zero Crossing

design corresponding to a ratio of 0.75:1.

The resonant L–C elements are now defined *uniquely* by the power supply output voltage and load current for a specific resonant tank frequency and current ratio $I_{out\ max}$ to $I_{r(pk)}$.

$$I_{r(min)} = \frac{V_{IN\ min}}{Z_r}, \text{ or } Z_r \leq \frac{V_{IN\ min}}{I_{out\ max}}$$

Substituting $Z_r = \omega_r L_r$ and $V_{IN} = V_{sec}$ for secondary resonance, the resonant inductor L_r and C_r are defined by :

1. $L_r = \frac{0.75 V_{sec\ min}}{\omega I_{out\ max}} \Rightarrow \frac{0.12 V_{sec\ min}}{f_{res} I_{out\ max}}$

2. $C_r = 1/(\omega^2 L_r) \Rightarrow .025/(f_{res}^2 L_r)$

3. Verify that $Z_r < V_{out}/I_{out\ max}$. If not, the ratio of the resonant to output current may need to be altered.

Transformer Turns Ratio

The transformer turns ratio is derived by equating the circuit input and output volt-second products. A topology coefficient K_t is introduced which specifies the ratio of the maximum switching frequency to that of the resonant tank frequency. It is somewhat analagous to maximum duty cycle in a square wave converter. Allowing K_t to approach unity in a resonant converter maximizes the turns ratio, thus lowering the primary current.

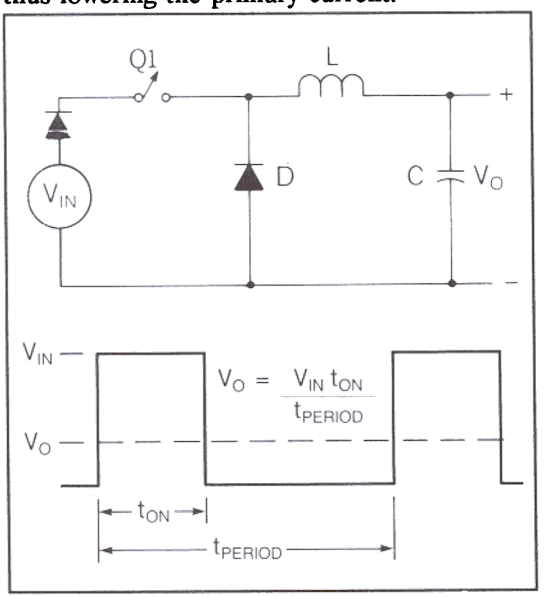

Fig. 10 & 11 - Square Wave Buck Regulator

As switching frequencies approach 1 MHz, diode recovery times and Mosfet rise and fall times prevent the topology coefficient from reaching unity. In addition, the resonant capacitor requires time to discharge into the output load. A K_t value of 0.8 is suggested by several of the references listed in the Appendix. The turns ratio can now be calculated from the volt second relationship described previously.

The transformer turns ratio N =

$$V_o = \frac{V_{IN} K_t}{2N}, \qquad N = \frac{K_t V_{IN\ min}}{2 V_o}$$

Accounting for the voltage drops,both the primary and secondary:

$$N = \frac{K_t}{2} \cdot \frac{V_{IN\ min} - V_{loss\ pri}}{V_{o\ min} + V_{diode} + V_{loss\ sec}}$$

The actual transformer secondary voltage has now been defined by V_{input} and the turns ratio N. The conversion period or frequency can be extracted from the energy transfer equations in the Appendix by substituting V_{sec} for V_{IN} in the given equations.

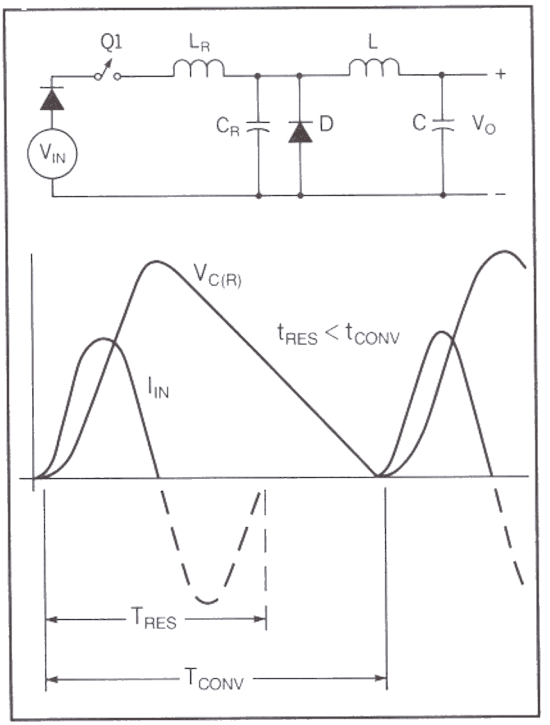

Fig. 12 & 13 - Resonant Mode Buck Regulator

Conversion Frequency

As the output load current I_{out} and input voltage V_{IN} vary, the control circuit adjusts the conversion frequency to maintain a constant output voltage, V_{out}. The maximum conversion frequency will occur at low line and full load, where by design, the frequency equals the resonant tank frequency divided by K_t, the topology coefficient.

$$K_t = \frac{f_{conv\ max}}{f_{res}} \qquad f_{conv\ max} = K_t\, f_{res}$$

Minimum frequency will occur at high line $V_{IN\ max}$ and light load $I_{out\ min}$ which can be estimated by the following relationship:

$$1/f_{conv\ min} = T_{conv\ max} = \frac{V_{IN\ min}\ Q}{2NV_oI_{o\ min}}$$

$$Q = \left[\frac{2NL_rI_{o\ min}^2}{V_{IN\ min}} + \frac{V_{IN\ min}\ C_r}{N} + \frac{\pi I_{o\ min}}{2f_{res}}\right]$$

Quasi-Resonant Circuit Relationships

SUMMARY OF APPENDIX 1

Timing relationships:

t_o = time when the cycle is initiated
$t_1 = L_r \cdot I_{out}/V_{sec}$
$dt_{21} = \pi/\omega_{res}$
$t_2 = t_1 + dt_{21}$
$dt_{32} = 1/\omega_{res} \cdot \sin^{-1}(I_{out}\ Z_r/V_{sec})$
$t_3 = t_2 + dt_{32}$
$dt_{43} = v_{Cr(t3)}\, C_r/I_{out}$
$t_4 = t_3 + dt_{43}$
$t_5 = [V_{sec} Q_t/(V_{out} I_{out})]$ (approx)

The charge transferred per cycle, Q_t, is approximated by :

$$Q_t = L_rI_{out}^2/V_{sec} + 2V_{sec}Cr + \pi I_{out}/\omega$$

Design Procedure and Calculations

The design specifications listed on page 1 will be used for this 150 watt application. A maximum switching frequency of 1 MHz has been selected as a good compromise between the attempts to obtain high power density (small size) and high overall efficiency.

1. Select the maximum switching frequency:

$f_{conv\ max}$ = 1.0 MHz

This also determines the resonant tank circuit frequency using the topology conversion coefficient, K_t.

$K_t = f_{conv\ max}/f_{res}$. Use K_t = 0.8

2. Calculate the resonant tank frequency, f_{res}

$f_{res} = f_{conv\ max}/K_t$ = 1 MHz/0.8 = 1.25 MHz

3. Determine the transformer turns ratio, N

$N = N_{pri}/N_{sec} = K_tV_{IN\ min}/(2V_{out} + V_{diode})$
= 5.19 (use 5:1)

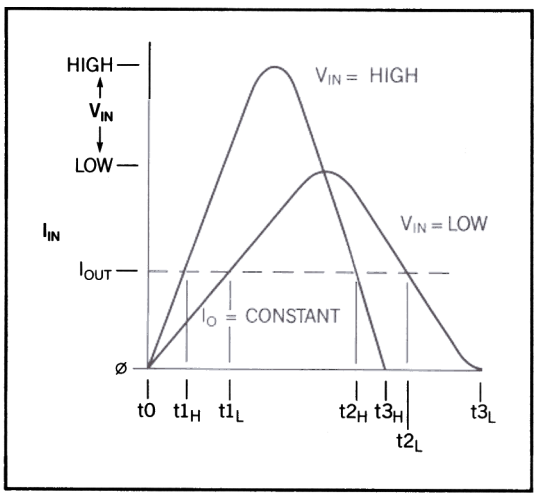

Fig. 14 - Effects of Line Change on I_{in}

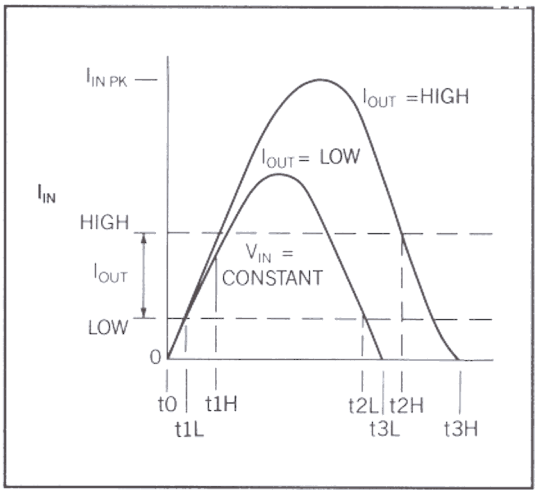

Fig. 15 - Effects of Load Change on I_{in}

4. Calculate $V_{in\ min}$, the minimum input voltage referred to the secondary:

$$V_{in\ min} = V_{s\ min}/2N = 220V/(2 \cdot 5) = 22\ V$$

The resonant inductor and capacitor values are calculated using the minimum input voltage to the secondary.

5. Calculate the resonant inductor value, L_r

$$L_r = 0.12V_{in\ min}/f_{res}I_{out\ max} = 176\ nH$$

6. Calculate the resonant capacitor value, C_r

$$C_r = .025/f_{res}^2 I_{out\ max} = 90.9\ nF$$

7. Calculate and check resonant impedance Z_n

$$Z_n = (L_r/C_r)^{1/2} = 1.39\ \Omega \text{ (yes, <1.5 ohms)}$$

The basic sections of the circuit are now complete. Detailed analysis of the primary and secondary voltages and currents follow.

Peak current calculations: The peak secondary current is approximated by:

$$I_{sec\ pk} = I_o + V_{in}/Z_n = I_o + V_s/(2 \cdot N \cdot Z_n)$$
$$= .072\ V_s$$

The peak current is a function of both input voltage and output current, and is graphically shown in Fig. 16.

The need for high peak current devices in a resonant mode power supply is evident from the values shown below, especially compared with a square wave converter of similar output power.

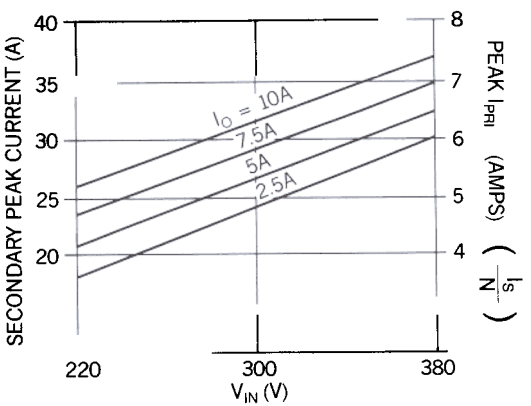

Fig. 16 - Peak Secondary Current vs. V_{in} and I_o

The peak secondary voltage is:

$$V_{s\ pk} = V_{s\ max}/2N = 370/2 \cdot 5 = 37V$$

Rectifiers in the secondary circuit need to block at least twice the peak voltage, and are typically selected with a much higher rating. Schottky diodes can be ruled out in this 15V output application due to their 45 to 90 volt breakdown voltages, so an ultra to hyperfast diode is required. A 150 volt,30 amp (DC) device provides ample safety margin. A low capacitance power package is also desired to minimize parasitics and power losses.

rms current calculations: The primary and secondary RMS currents can be approximated to a high degree of accuracy by a pulsed sinusoidal waveform. The relationships derived in the previous section for peak currents, *on* times and conversion frequencies will be used to calculate the RMS currents incorporating the following equation.

$$I_{rms} = I_{peak}\left[\frac{T_{on}}{2\ T_{per}}\right]^2$$

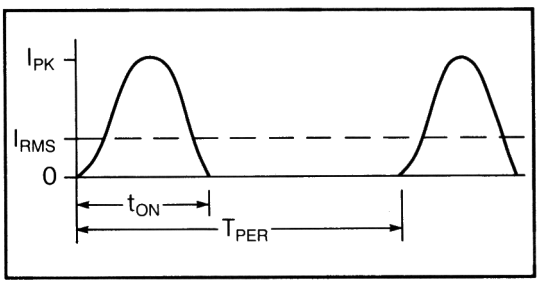

Fig. 17 - rms Current Calculation

The primary current calculations will use the conversion period of $1/f_{conv}$ due to the bidirectional switching of the primary. Secondary currents conduct only once per two conversion periods due to the bridge arrangement of the secondary windings. Both low and high input voltage conditions will be examined at full output load to determine worst case conditions.

The transformer primary wire size will be calculated using the rms current components, in addition to thermal considerations of the transistor switches and rectifiers.

Each of the Mosfet switches, secondary rectifiers and transformer secondary windings conduct current only once per two conversion

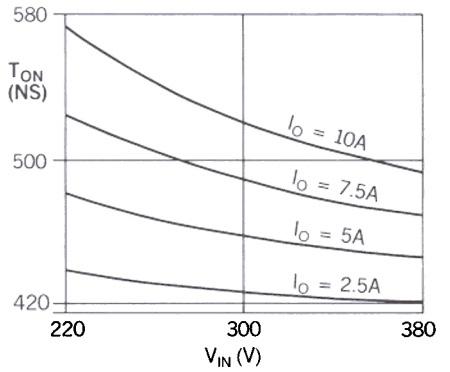

Fig. 18 - On Time vs. V_{in} and I_{out}

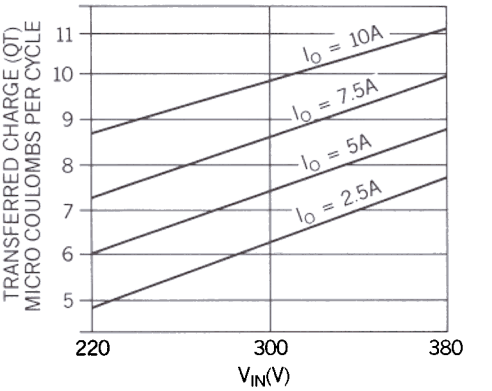

Fig. 19 - Q_t, Transferred Charge vs. V_{in} and I_{out}

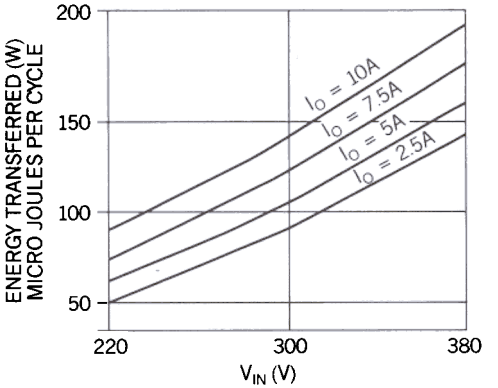

Fig. 20 - Energy Transfer per Cycle vs. V_{in} and I_{out}

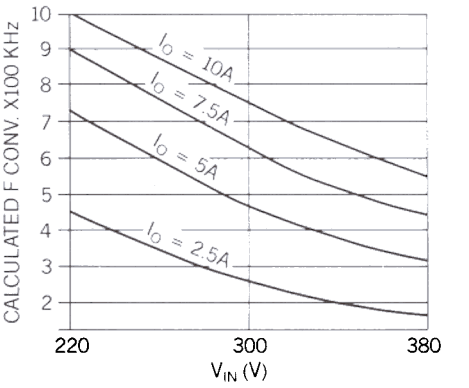

Fig. 21 - Calc. Conversion Freq vs. V_{in} and I_{out}

cycles. This results in a lower rms current through each device.

Low Line	High Line
$I_{sec\ pk}$ = 26 A	$I_{sec\ pk}$ = 37 A
$I_{pri\ pk}$ = 5.2 A	$I_{pri\ pk}$ = 7.4 A
t_{on} = 575 ns	t_{on} = 495 ns
T_{per} = 1.0 µs	T_{per} = 1.82 µs

rms Transformer Primary Current:

$I_{pri\ rms}$ = 2.78 A $I_{pri\ rms}$ = 2.72 A

rms Current - Mosfet Switches and Secondary Rectifiers:

$I_{rect\ rms}$ = 9.86 A $I_{rect\ rms}$ = 9.65 A

$I_{MOS\ rms}$ = 1.97 A $I_{MOS\ rms}$ = 1.93 A

Timing Considerations: The operation of this quasi-resonant circuit has been described as requiring a variable frequency, *fixed on time* control pulse train. Actually, the *on* time must be varied to facilitate zero current switching with changes in input voltage and output current. Using the timing relationships presented earlier, the *on* time is calculated and plotted for the ranges of V_{in} and I_{out} in Fig. 18.

Transferred charge: The charge transferred from the primary to the secondary per cycle is a function of both V_{in} and I_{out}. Using the equations presented in the Appendix, the results are graphically represented in Fig. 19.

For the selected values of voltage and current shown, the average change required in voltage or output current per microCoulomb transferred have been calculated:

Avg dV/µC = 5.935, and Avg dI/µC = 2.086

The energy transferred per cycle is obtained by multiplying the results from the charge calculations by $V_{in}/2$ to convert from charge to energy, with the results shown in Fig. 20.

The conversion period is obtained by dividing the energy transferred per cycle by the out-

put power, accounting for an overall efficiency near 85%. Conversion frequency, its inverse, is graphically depicted for various input voltages and output currents in Fig. 21.

Power Mosfet Switch Considerations

The power Mosfet selection process must take into account the three types of losses incurred by the high voltage switch. First, and probably the most predominant loss contributor is the FET *on* resistance, or $R_{ds(on)}$. Conduction losses are minimized by using a FET with the lowest $R_{ds(on)}$ obtainable.

$$P_{loss\ dc} = I_{pri\ rms}^2\ R_{ds(on)} \quad \text{(Watts)}$$

Generally the low resistance is attained by paralleling numerous FET cells of higher on resistance. The result is a single high current, low resistance device with a large die size, or geometry. This technique is great for lower frequency applications where the transition (turn-on and turn-off) times are a small percentage of the entire duty cycle. At high frequencies and especially with high voltages, this paralleling scheme introduces many difficulties in minimizing the switching transition losses.

Each cell has a finite output capacitance which quickly "adds up" when many are placed in parallel. The FET output capacitance is charged and discharged to the FULL input bulk voltage each cycle, contributing losses. At high frequencies, changing to a larger size FET could increase the total FET losses, despite having a lower *on* resistance. The incremental gains of lower conduction losses are lost to the higher switching losses of the larger capacitance FET. For this reason, it is a worthwhile exercise to examine several different size FETs over the line and load ranges of this design.

$$P_{loss\ ac} = 0.5 C_{oss} V_{in}^2 f_{conv}/2 \quad \text{(Watts)}$$

The gate drive power losses are generally negligible with respect to the total losses, but can be calculated from:

$$P_{loss\ gate} = 0.5 V_{aux} Q_t f_{conv}/2 \quad \text{(Watts)}$$

where Q(t) is the FET total gate charge, accounting for the gate to source charge plus the Miller effect charge.

The greatest primary current occurs at full load, which will be used for the worst case evaluation of power losses. Both high and low input voltage were used to calculate the ac losses, then averaged. The following list is a summary of the total power loss for each Mosfet switch in this application. A 100°C junction temperature at the FET die was assumed, where the actual *on* resistance is double that of the published specification. Various size FETs have been analyzed to compare the ac and dc losses to select one which exhibits the lowest total losses.

Circuit specifics (at the FET switches):

$I_{pri\ rms}$ = 1.97A at V_{in} = 220V, f_{conv} = 1 MHz

$I_{pri\ rms}$ = 1.93A at 375V, 550 KHz

Device @100°C	R_{ds} Ω	C_{oss} pF	Q_g nC	P_{dc} W	P_{ac} W	P_g W	P_{total} W(ea)
IRF720	3.6	64	20	13.7	1.05	0.08	14.87
IRF730	2.0	100	35	7.62	1.57	0.11	9.30
IRF740	1.1	210	63	4.19	3.30	0.19	7.68
IRF820	6.0	54	19	22.8	0.85	0.07	23.78
IRF830	3.0	91	32	11.4	1.43	0.10	12.96
IRF840	1.7	180	63	6.47	2.83	0.19	9.49
IRFP440	1.7	180	63	6.47	2.83	0.19	9.49
IRFP450	0.8	350	130	3.04	5.51	0.39	8.95
IRFP460	0.54	480	190	2.05	7.56	0.57	10.19

The lowest overall losses are obtained with the 740 type devices which will be utilized in this application. This procedure will yield different results for each application, and is a recommended step towards minimizing power losses.

Rectifier Selection

Evident from Figures 16 and 17 is the need for high performance rectifiers to achieve an overall high efficiency power supply. Peak secondary currents approach 40 amps, with an rms component near 14 amps. Due to the high peak reverse voltages of nearly 100 volts, Schottky diodes cannot be used as the secondary rectifiers. Even the "freewheeling" diode must withstand 80 volt peaks at high line.

Reverse recovery times must be minimal to prevent reverse current from flowing in the primary switches in addition to enhancing efficiency. While the circuit currents are quasi-sinusoidal, the rectifier voltage is not. Parasitic inductances and capacitances of the

device and its package must also be accounted for as part of the resonant L-C tank. This implies that the transformer will be designed for a lower leakage inductance than the resonant L and external inductance will be introduced to obtain the precise amount.

The TO-247 package will be utilized for two reasons. First, it has lower parasitics and is better suited to high frequency applications than its TO-3 metal case counterpart. Second, it is simple to heatsink this flat package, which can be mounted in various configurations.

Unitrode UES3015S ultrafast 30 amp, 150 volt rectifiers were selected for the secondary input diodes. Typical performance characteristics are 35 ns reverse recovery times and less than 1 V forward drop at 30 A and 125°C junction temperature. The "freewheeling" diode used is a Unitrode UES1615S ultrafast type, with 16 amp dc capability and a forward drop of less that 0.85 V. It too exhibits a 35 ns reverse recovery time.

Power dissipation and heatsinking requirements for each device can be calculated using the secondary currents obtained previously in this power supply design. Snubbing of each diode will be left to the prototype stage when any parasitic circuit influences can be evaluated.

Main Transformer Design

The transformer design begins with a basic idea of the core geometry most applicable to the particular design. Off-line supplies lend themselves to low, wide winding windows, typical of the ETD geometry. This window shape provides adequate room to accommodate the creepage and clearance distances required for international safety specifications.

Switching of the transformer primary will occur at a maximum of 500 KHz, and standard ferrite materials will be utilized in this example. With numerous choices to consider, the 3C6A material was selected.

To begin this 150 watt design, a fair estimate is to keep the transformer losses around 1% of the total input power, or approximately 2 watts. In addition, the transformer temperature rise is desired to be less than 40°C for combined copper and core losses. A core size can be approximated knowing that its thermal resistance, R_t, needs to be in the neighborhood of 40°C/2W, or less than 20°C/W. This is useful as a first iteration to determine the approximate operating flux density required. The precise size will be calculated using the area product formula for core-loss limited conditions, typical in a high frequency power supply.

$$AP = \left[\frac{P_{in} \cdot 10^4}{120K\ 2f} \right]^{1.58} \cdot (K_h f + K_e f^2)^{0.66} \quad cm^4$$

where:

Pin - Input Power = 180 Watts
K - Winding Factor = 0.163 for half bridge
f - Transformer Frequency = 500 KHz
K_h - Hysteresis Coeff. (3C6A) = $4 \cdot 10^{-5}$
K_e - Eddy Current Coeff. (3C6A) = $4 \cdot 10^{-10}$

For this design,the area-product calculates to 0.543 cm^4, which is slightly less than the smallest standard core size, the ETD-34. Because the core volume is slightly larger than required, the actual core losses (per cm^3) will be lower than first estimated.

The manufacturers core data lists the thermal resistance of the ETD-34 core set as 19°C/W, with a core volume of 7.64 cm^3. Several methods of dividing the power losses between the core and copper can be used. The most common of these suggests an almost equal split between the two, allowing slightly more core than copper loss if possible. An even division of the total losses between the two will be utilized in this design as a first approximation. Later, an evaluation of the minimum number of turns and wire sizes may suggest that the 50/50 ratio be changed to favorably accommodate fewer turns, or less copper. The actual core power density, P_d, is calculated from the following equation, allowing a 20°C temperature rise, T_r, due solely to core losses.

$$\text{Power Density} = \frac{T_r}{R_t \cdot Vol} = \frac{20°C}{19 \cdot 7.64}$$

$$= 138\ mw/cm^3$$

Referencing the manufacturers data sheet for the 3C6A material at a power loss density of approximately 140 mW/cm^3 and a 500 KHz operating frequency, it is determined that an operating flux density of 300 gauss (0.030 T) be

used. The total flux density swing, ΔB, is twice that, or about 0.060 Tesla. The minimum number of primary turns is calculated assuming 5 V primary drops, low line conditions, and a cross-sectional core area, A_e, of 0.971 cm^2.

$$\text{Power Density} = \frac{V_{pri} t_{on} \cdot 10^4}{\Delta B \cdot A_e}$$

$$= \frac{105 \cdot 575 \cdot 10^{-9} \cdot 10^4}{.060 \cdot 0.971} = 10.3 \text{ turns (use 10)}$$

A turns ratio N of 5:1 was previously established for this design. Minimized leakage inductance is obtained by "sandwiching" the secondaries between the two primary halves. In this example, one-half of the primary turns will be wound first, closest to the core center leg. Then, the entire secondary is wound directly above the primary half. The final winding is the remaining primary half, as shown in Fig. 22.

Copper strip or foil will be utilized for each winding to minimize "build-up " which increases the distance between windings, hence increases leakage inductance. If the transformer leakage inductance is greater than the required resonant inductance, then the transformer must be redesigned for lower leakage.

The required primary and secondary copper cross-section areas are calculated using their respective currents divided by 450 amps/cm^2 for a low temperature rise. Other transformer specifics are calculated below.

Primary rms current, $I_{pri\ rms}$ = 2.78 A rms

Secondary rms current, $I_{sec\ rms}$ = 9.86 A rms

Primary copper area, $A_{xp} = I_{pri\ rms}/450$
= .0062 cm^2

Secondary copper area, $A_{xs} = I_{sec\ rms}/450$
= .022 cm^2

Pri. inductance, $L_{pri} = A_L N_p^2$ = 190μH

Sec. (half) inductance, $L_{sec} = A_l N_s^2$ = 7.6μH

The primary conductor area is approximately equal to the area of an AWG # 19 wire, while the secondary area is closest to AWG #14. Eddy current calculations show that the depth of penetration at 500 KHz is .0106 cm, or about the thickness of a number 37 AWG wire. The most practical technique to minimize the AC loss in a transformer winding is to use copper strip or foil, as in this design. Its width is determined by the bobbin width and safety creepage requirements of 8 millimeters as shown.

The required 8 mm primary to secondary spacing between winding ends will be subtracted from the bobbin width of 2.10 cm, leaving 1.30 cm (0.51 inch) for the copper strip width. Allowing for tolerances, standard 0.5 inch width foil will be used in this design. The strip thickness is calculated by dividing the required copper area by the 1.27 cm (0.5 inch) width.

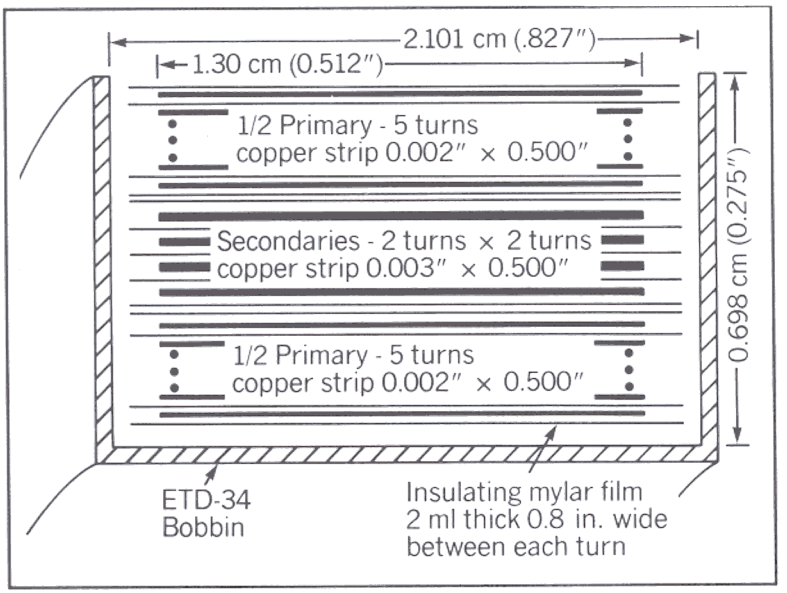

Fig. 22 - Transformer Winding Layout

Pri thickness = A_{xp}/Width = $6.18 \cdot 10^{-3}/1.27$
= .00475 cm, or .00187 in
Sec thickness = A_{xs}/Width = $21.9 \cdot 10^{-3}/1.27$
= .01685 cm, or .00663 in

Standard 2 mil (0.0051 cm) foil will be used for the primary. This is slightly larger than the required thickness of .00475 cm, and is less than 1/2 the .0106 cm penetration depth. Secondary penetration is from both sides because of the interleaved primary, so the calculated secondary thickness should be and is less than twice the penetration depth. Two paralleled 3 mil foils are used as secondary conductors.

The resistance and power loss of each winding is calculated from the following relationships, based on the resistivity of copper at 100°C, $\rho_{cu} = 2.29 \cdot 10^{-6}$ Ω-cm. Total copper and core losses are also highlighted, in addition to the total temperature rise at the maximum conversion frequency.

$$\text{Winding resistance} = \frac{\rho_{cu} \cdot \text{avg length/turn} \cdot N}{A_x}$$

$R_{pri} = 2.29 \cdot 10^{-6} \cdot 5.99 \cdot 10 / 6.18 \cdot 10^{-3} = 22.2\ m\Omega$

$R_{sec} = 2.29 \cdot 10^{-6} \cdot 5.99 \cdot 2 / 21.9 \cdot 10^{-3} = 1.25\ m\Omega$

$P_{loss\ winding} = I_{rms}^2 \cdot R$

$P_{loss\ pri} = 2.78^2 \cdot .0222 = 171\ mW$

$P_{loss\ sec} = 9.86^2 \cdot .00125 = 121.5\ mW$

$P_{loss\ copper} = 2 \cdot 0.171 + 0.1215 = 0.4635\ W$

Total power loss = copper losses + core loss

$P_{total} = 0.464 + 1$ (approx) $\leq 1.5\ W$

Temp. rise = $Rt \cdot P_{total} = 19°C/W \cdot 1.5W$
= 28.5°C

Output Inductor Design

The output inductor will be designed for one amp of ripple current at the minimum conversion frequency of approximately 200 KHz. Due to the variable frequency operation, the ripple current will change inversely with operating frequency, as maximum load occurs, the ripple current is at its lowest. This mode of operation helps lower the overall losses at full load because with lower ripple the peak current that must be switched is less. In addition, it reduces the size of the output choke since the peak (DC+AC) and full load (DC) current are within one percent of each other.

$$L_o = [(V_{out} + V_{diode}) \cdot t_{off\ max}] / \Delta I_{out}$$

$$= 15.8V \quad 5\ us / 1\ A = 80\ \mu H \text{ (approx)}$$

At the maximum conversion frequency and $t_{off\ min}$, the output ripple current reduces to:

$$\Delta I_{out} = [(V_{out} + V_{diode}) \cdot t_{off\ min}] / 80\ \mu H = .08\ A$$

Referring to Section M5 of the Unitrode Seminar Manual, core selection starts by calculating the area product:

$$AP = A_w A_e = \left[\frac{L_o I_{pk} I_{fl} \cdot 10^4}{420 \cdot K \cdot B_{max}}\right]^{1.31}$$

$$= \left[\frac{80 \cdot 10^{-6} \cdot 10.08 \cdot 10 \cdot 10^4}{420 \cdot 0.7 \cdot 0.3}\right]^{1.31} = 0.89\ cm^4$$

A PQ type geometry has been selected for the output choke application. The core set closest in size to the required area product is the PQ 32, which is available in either a 20 or 30 mm height. Of the two, the PQ32/20 size will be used because its height is similar to the ETD34 core set used for the main transformer. Its magnetic area is 1.70 cm^2.

$$N_{min} = \frac{L \cdot I_{pk}\ I_{fl} \cdot 10^4}{B_{max} A_e}$$

$$= \frac{80 \cdot 10^{-6} \cdot 10.08 \cdot 10^4}{0.30 \cdot 1.7} = 15.8 \text{ turns (use 16)}$$

The cores will require gapping to store the required energy without saturating. Gap length is calculated from the inductance formula:

$$\ell_g = (\mu_o \mu_r N^2 A_e \cdot 10^{-2}) / L = .068\ cm$$

using $\mu_o = 4\pi \cdot 10^{-7}$ and $\mu_r = 1$ (air)

Correcting the gap length for the fringing field, a gap of .082 cm (.032") should be used.

Again, copper strip is used to minimize losses. Winding resistance and power loss calculations are similar to those of the main transformer design,and total less than 1.5 W.

Output Capacitor

There are two components of ripple voltage which need to be considered in meeting the design goal of 100 mV. They are both caused by inductor ripple current. The first is simply:

$$\Delta V_{out} = \Delta Q / C_{out}$$

For a given ripple current, this component is minimized by increasing the capacitor value. If this were the only contributor, the minimum capacitance required is:

$$C_{outmin} = \frac{1}{2}\,\frac{\Delta I_{out}}{2}\,\frac{1}{2f}\,\frac{1}{\Delta V_{out}}$$

This component varies with frequency. At $f_{conv\ min}$, 6.25 µF are needed, but at $f_{conv\ max}$ (1MHz) only 0.1 µF is required to maintain the ripple voltage specification.

The second (and usually predominant) ripple voltage component is the voltage drop across the capacitor Equivalent Series Resistance (ESR) caused by the ripple current of ΔI_{out}. The maximum ESR allowable for 100 mV ripple is:

$$ESR_{max} = 100\ mV / 1.0\ A = 100\ m\Omega$$

The two ripple voltage components do not add directly as they are in quadrature. With electrolytic capacitors, the ESR component dominates the capacitor selection. The resulting capacitance value is so much greater than the minimum value required that the $\Delta Q/C_{out}$ term can be ignored. An added benefit of a large output capacitance is the improvement in load transient capability.

In this design, two 100 µF electrolytic units were used in parallel to achieve an ESR value of 3 to 15 milliohms - a broad range necessitated by the difficulty in getting specified high frequency data from capacitor manufacturers.

A final component added to the output filter is a good high frequency capacitor to bypass the inductive components of the electrolytics and shunt any switching spikes which might get to the output. Unitrode "P" type ceramic monolithic capacitors are used for this application. Different capacitor types and values can be paralleled to obtain a low impedance over a broad frequency range, useful in this variable frequency application.

Gate Drive Circuitry

The ideal gate drive circuit must deliver sharp turn-on and turn-off pulses to the high voltage power Mosfets. This is made possible by the UC3860 controller's high speed totem pole drivers. Delivering 3 amp peak currents, the drivers have typical rise and fall times of 25 ns into a 1 nF load.

Half bridge circuits require the use of a gate drive transformer to electrically isolate the "high-side" switching transistor from the control circuit. Driving both transistors from the same transformer 180° out of phase offers nearly identical drive signals to each transistor. This tends to balance the switching losses and maintain a narrower band of the associated transition EMI.

The drive transformer must have low leakage inductance to provide crisp edges during the transitions with little overshoot. This makes zener clamps and snubbing circuits unnecessary at the transformer outputs. A 0.50" O.D. toroid is used, fitted with three identical windings of ten turns each. This helps minimize the transformer magnetizing current and maximizes the peak current delivered to the FET gates.

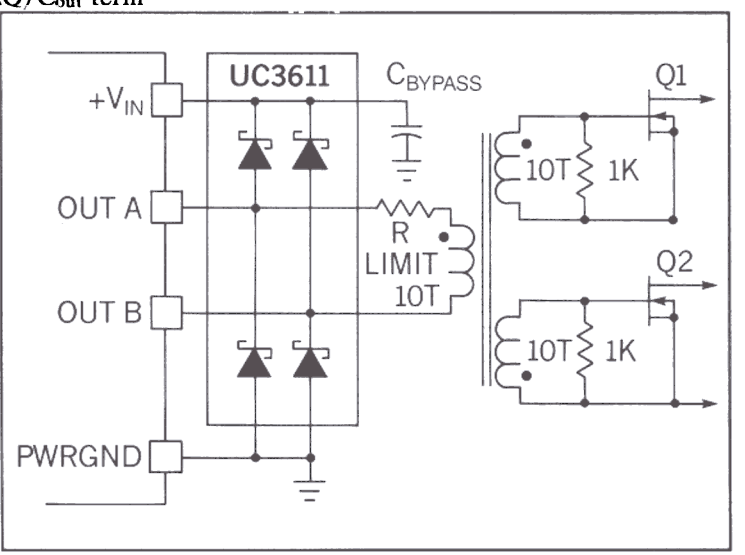

Fig. 23 - Gate Drive Circuit

Resistors from gate to source at each FET provide a fairly low impedance to prevent turn-on during start-up while the IC may still be in undervoltage lockout. During regular operation, these resistors have negligible impedance.

On the controller side, the UC3611 quad Schottky diode prevents the IC outputs from going below ground, avoiding substrate biasing problems. A series resistor limits the peak current to the 3 A rating, and the transformer is reset while both outputs are low, between cycles.

Zero Current Detection and Switching

The primary current is used for two important functions in this design, fault protection and zero current detection. A typical configuration is shown in Fig. 26. The generalized circuit starts with the use of a current transformer in series with the primary of the main transformer to detect primary current. A turns ratio of 1:25 reduces the switch current to a manageable level. It is full wave rectified by 1N4148 diodes (D_6-D_9) and converted to an appropriate unipolar voltage at the current sense resistor, R_{11}. In addition, zero current or zero voltage can be detected by using the UC3860 uncommitted comparator. Its open collector output can interface with the RC *on* timing pin of the one shot, pulling it below the turn off threshold at zero detection. As shown in Fig. 24, this reduces the *on* time of the one shot timer, allowing the Mosfets to switch at zero current for high efficiency.

Implementation requires shifting the noninverting input between two thresholds so that only the falling edge of primary current is an acceptable input for switching to occur. (See Fig. 25.) This is done to prevent a false output from the comparator during the beginning of the cycle, where zero current also occurs. Primary current sensing will be offset by the resistor divider network R_{21} and R_{16} from V_{ref} to ground. This is fed into the inverting

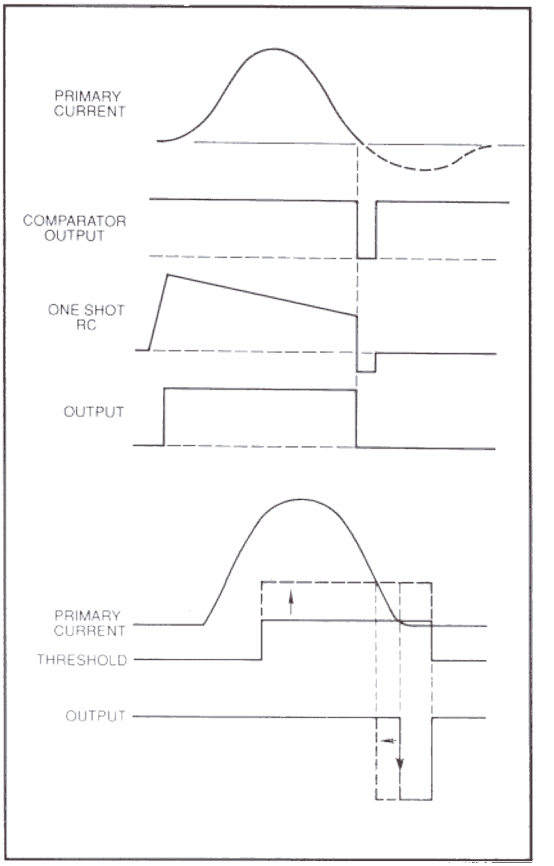

Fig. 24 & 25 - Zero Current Switching

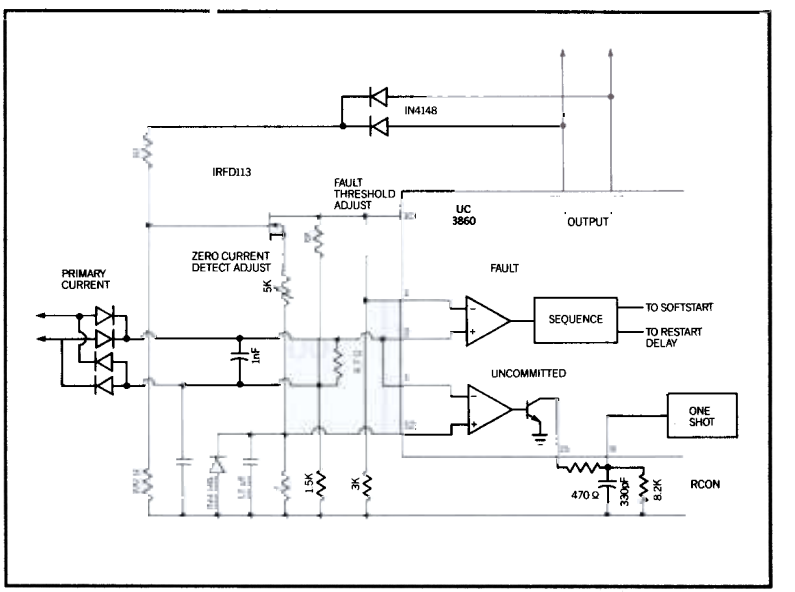

Fig. 26 - Zero Current Switching Circuitry

input of the uncommitted comparator.

In Fig. 26, adjustments can be made to provide a comparator output *just* prior to zero current by resistor R20. Propagation delays throught the IC and drive circuitry, although minimal, can effectively be "nulled-out" along with Mosfet delays by this technique.

The UC3860 Resonant Mode Control IC

The block diagram of the UC3860 in Fig. 27 displays several key building blocks which together provide the functions necessary for precise resonant mode control. To begin, the undervoltage lockout turn-on and turn-off thresholds are pre-programmed for 17 and 10 volts respectively and are used in their standard configuration. This allows ample time for start-up and bootstrapping to occur in an off-line supply while providing adequate Mosfet gate drive voltages. The UVLO can also be reprogrammed for other turn-on and off thresholds. Also, it functions as an alternate shutdown mechanism. While UVLO is invalid, the UC3860 reference voltage output is held low, deactivating the internal circuitry. The 1% accuracy 5.0 V bandgap reference is capable of driving ten milliamps maximum external loads.

The power supply output voltage will be divided down to deliver 3.0 volts at the inverting error amplifier input for the desired V_{out}. With its high gain-bandwidth of 5 MHz, this voltage type op amp also features controlled output voltage excursions. The error amp output swings from 0.0 to 2.0 V above the voltage at the VFO I_{osc} input and tracks this node over temperature. This mechanism facilitates the maximum conversion frequency clamp in addition to the voltage (or current) to frequency conversion gain.

Variable frequency operation commences with the error amplifier providing a variable output voltage. This is transformed to a variable current at the VFO variable current input, I_{vfo}. Internal circuitry mirrors this current to the VFO timing capacitor, C_{vfo} . Maximum fre-

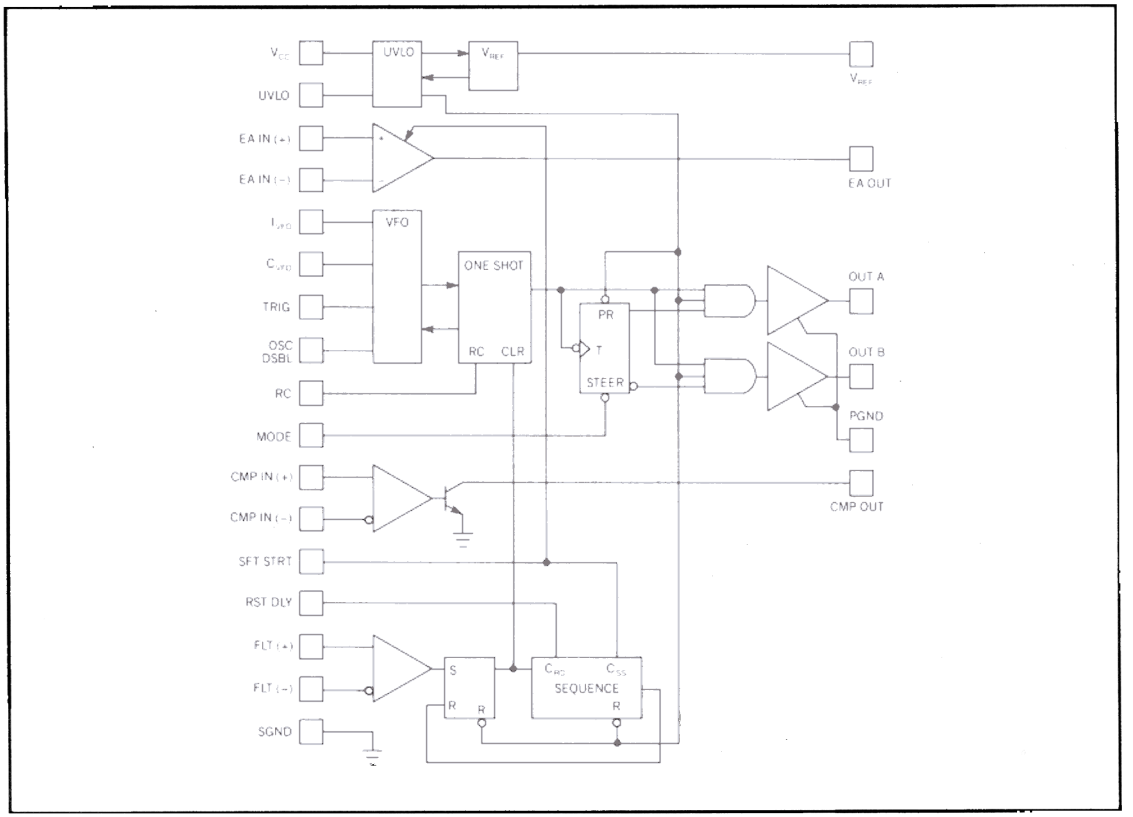

Fig. 27 - UC3860 Block Diagram

quency occurs at $2.0V/R_{vfo} \cdot C_{vfo}$, which coincides with the error amplifier upper clamp. Minimum frequency is also programmable via resistor R_m from V_{ref} to the I_{vfo} input. The frequency to voltage gain of the IC in MHz/V (or GHz/V) is also established by these timing components. Additionally, the VFO can be externally triggered and/or disabled at the respective input pin accommodations.

Fixed on-time pulse widths are generated by the programmable one-shot timing circuit. An RC network is charged by an internal source at the onset of a cycle, then self discharges during the on-time. This occurs between the precise thresholds of the one-shot's comparators. On-time can easily be shortened by an external influence used to discharge the RC components below the comparator's turn-off threshold. This architecture simplifies interfacing with various forms of zero voltage or zero current type switching. The output of the UC3860 uncommitted comparator is an open collector which can interface directly to the one shot (RC) timing pin.

Programming the VFO and One-shot:

Let C_{vfo} = 330 pF, $C_{oneshot}$ = 330 pF
f_{max} = 1.05 MHz, f_{min} = 200 kHz

1. $f_{max} = 2V/R_{vfo}C_{vfo}$;
   $R_{vfo} = 2/(1.05MHz \cdot 330pF) = 5.77\ k\Omega$

2. $f_{min} = 1V/R_mC_{vfo}$;
   $R_m = 1/(0.2MHz \cdot 330pF) = 15.15\ k\Omega$

3. $t_{on} = 0.22 \cdot R_{on} \cdot C_{on}$;
   $R_{on} = 600ns/(0.22 \cdot 330pF) = 8.26\ k\Omega$

The output from the one-shot feeds another programmable module, the toggle flip-flop. Logic selection at the Output Mode pin either alternates the outputs for dual-ended configurations, or unifies outputs A with B for single ended applications. As V_{ref} becomes valid, the toggle flip-flop is always steered towards the A output. While this may be of little concern in some designs, a predictable sequence of events upon power-up is always facilitated.

Each totem-pole output is specified for 3 Amp peak drive pulses, sufficient to insure abrupt transitions at the Mosfet switches. When operating in unison, a 6 A peak current is obtained. Rise and fall times into a 1 nF load are typically 20 nanoseconds. As seen in previous high power IC's, the totem pole power ground is terminated through a separate pin which isolates its power ground noise from that of the IC's signal ground.

Soft start is accomplished by limiting the amplifiers output voltage to that of the soft start pin, typical in most IC controllers. An internal 5 microamp current source from V_{ref} pulls up on the external soft start capacitor, which gradually increases the conversion frequency upon start-up, as opposed to widening the pulse width in conventional PWMs.

Fault protection and management circuits included in the UC3860 are fully user programmable. A fault comparator which has both inverting and non inverting inputs is used to drive a programmable sequence latch. The operation of this latch is controlled at the programmable Restart Delay (RST DLY) pin, and has three unique modes. First, it can be oriented to latch the outputs off until UVLO or V_{cc} are toggled, similar to firing a shutdown SCR. Secondly, it can be used to cease operation until the fault input is removed from the comparator, then recommence operation. The third and most popular mode is often referred to as "hiccup" mode. After receiving a fault, the outputs are turned off for a programmed time interval called the restart delay. Operation is then resumed, provided of course that the fault was removed. Implementation only requires a capacitor from RST DLY to ground.

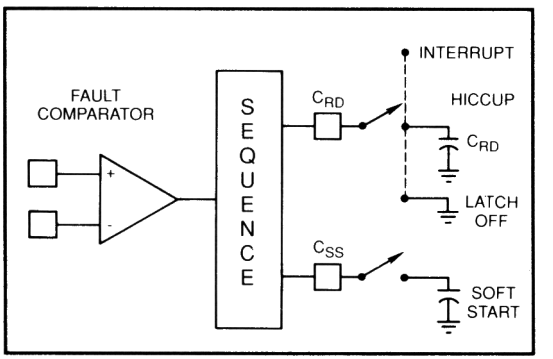

Fig. 28 - Fault Management Programming

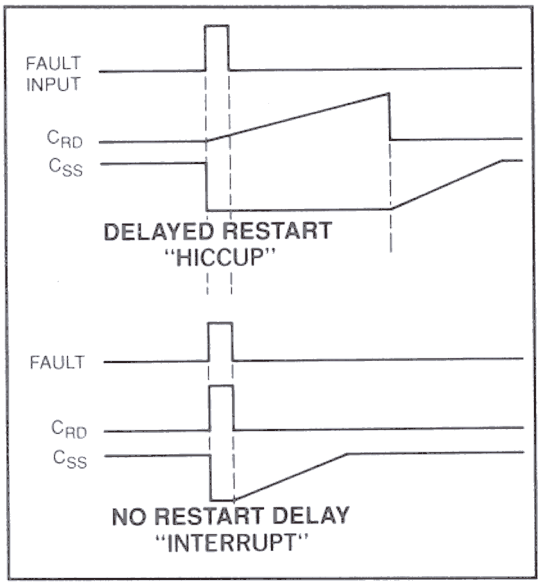

Fig. 29 - Fault Management Waveforms

Closing the Loop

There are several gain stages in the quasi-resonant control loop, and each will be examined to obtain good closed loop circuit response. The block diagram below displays the various gain stages.

Error Amplifier: A reference voltage is applied to the noninverting input of the error amplifier, and the power supply output voltage, through a voltage divider, is applied to inverting input. The error amplifier (E/A) output is commonly referred to as the error voltage V_e, which is an amplified signal corresponding to the deviation of the power supply output voltage from the desired level. The compensation network is designed last, after analyzing the other loop gain contributors. It will provide adequate phase margin at the desired zero dB crossover point to ensure circuit stability.

The varying E/A output voltage V_e is used to generate a variable current to the VFO current input pin, I_{vfo}. As this current is varied, so is the power stage conversion frequency. A higher V_e corresponds to a higher conversion frequency. These values are designed to track each other over temperature, and a linear voltage to current transformation can be assumed. The voltage to current gain into the VFO equals the 2 volt maximum output swing of the error amplifier divided by the VFO input resistor.

Variable frequency oscillator: The variable frequency converter stage accepts an input current at the I_{vfo} input and generates a proportional output frequency. The gain of this stage is programmed by the E/A output voltage with the I_{vfo} input resistor and the VFO timing capacitor, C_{vfo} . The VFO output frequency is approximated by:

$$f_{osc} = I_{vfo}/C_{vfo} \text{ , and } f_{max} = 2V/(R_{vfo} \cdot C_{vfo})$$

The minimum frequency is programmed by a resistor from V_{ref} to the I_{vfo} input, and the transformation of the error amplifier output voltage to frequency is quite linear.

Error amplifier voltage swing = 2 Volts

f_{conv} = 200 kHz min – 1 MHz max

VFO gain:

G_{vfo} = Δ800 kHz / Δ2 V = 0.4 MHz/V

Power stage: The small signal gain of the power stage is approximated by analysis of the charge transferred at various line and load combinations. An assumption is made that the power switch *on* time is constant, and any changes in frequency directly effect the *off* time, or resonant capacitor discharge time. In addition, both V_{IN} and I_{out} are assumed to be constant during the interval of interest.

Based on the relationship that the energy into the resonant circuit, W, equals the output power multiplied by the conversion period:

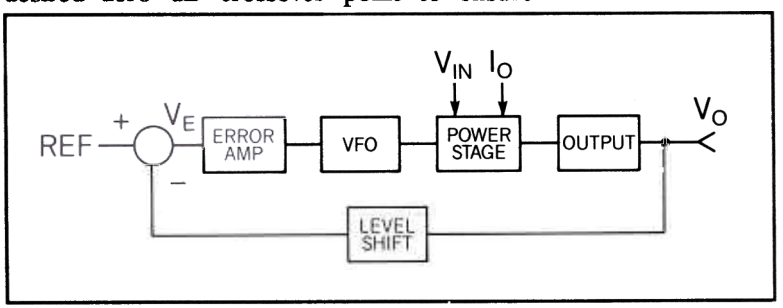

Fig. 30 - Control Loop Block Diagram

$$W = (Q_{in}V_{sec}/2) = \text{Power} \cdot t_{conv}$$
$$= V_{out}I_{out}/f_{conv}$$

therefore:

$$V_{out} = f_{conv}W/I_{out}$$

This term is assumed constant for the interval of interest.

Tabulated below at several points of interest are the values for the power stage gain, from the results of a previous section in this presentation. The gain (in volts per MHz) varies significantly over the input and output ranges, and the highest value will be used to approximate the worst case condition.

V_{IN} sec V	I_{out} A	Win µJ/cyc	f_{conv} kHz	Gain V/MHz	Gain dB
22	2.5	50	450	9.0	19.1
38	2.5	140	180	10.1	20.1
22	5	60	730	8.76	18.9
38	5	160	320	21.4	26.6
22	7.5	78	900	19.3	25.7
38	7.5	185	450	22.6	27.0
22	10	91	1000	19.1	25.6
38	10	205	560	23.6	27.5

The worst case value of 23.6 V/MHz will be used for the power stage. Multiplying this by the VFO gain of 0.4 MHz/V results in a combined gain V_{out}/V_e of 9.44 (19.5 dB).

Output Filter Section: The output filter response is defined by :

L_{out} = 80 µH; C_{out} = 200 µF

R_{out} = 1.5 Ω min to 10 Ω max

ESR = 2 to 10 mΩ

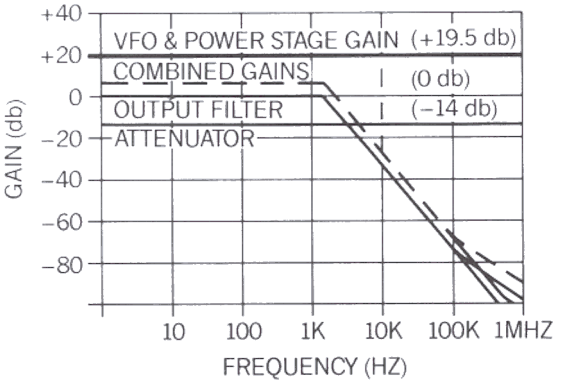

Fig. 31 - Gains vs. Frequency

$$\text{Pole frequency} = \frac{1}{2\pi(L_{out}C_{out})^{0.5}} = 1.25 \text{ kHz}$$

$$\text{ESR Zero} = \frac{1}{2\pi C_{out}\text{ESR}} = 79.6 - 398 \text{ kHz}$$

The output voltage divider shifts the level of the 15 V output to the required 3 V error amplifier input, resulting in a gain of -14 dB.

Compensating the quasi-resonant converter: The generalized approach to this compensation is to place the first pole at a low frequency, typically around one hertz. Two zeros are then introduced at approximately the output filter break frequency to compensate for its two pole rolloff. A second pole is placed at a fairly high frequency to roll off the loop gain in a predictable manner. Unlike their predecessors, the newer control ICs rarely run out of gain-bandwidth and require this high frequency pole.

Most of the previously described elements can be lumped together into one gain vs. frequency Bode plot of everything except the error amplifier, as shown in Fig. 31. The VFO, power stage and level shifting voltage divider have gains that are independent of frequency, and are easily combined. The output filter section response is then multiplied by the combined gain of the previous calculation. One curve now depicts the entire loop response from the error amplifier output around to its input.

The desired characteristic of the overall loop including its zero dB crossover frequency can be shown in a Bode plot, as in Fig. 32. The E/A compensation network will include two zeros near the output filter break frequency to cancel these two poles. Assume for now that the high frequency pole of this circuitry will be

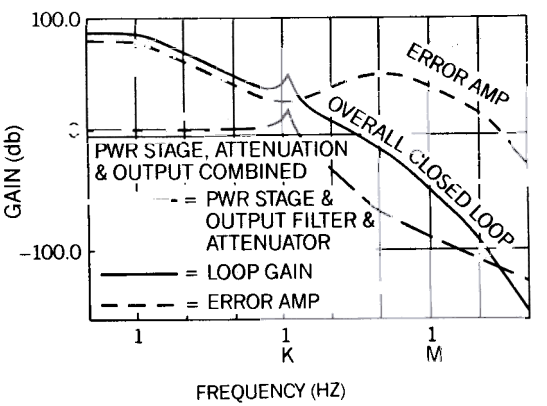

Fig. 32 - Closed Loop Elements

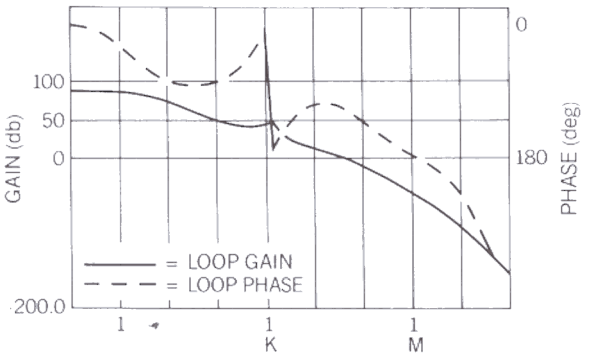

Fig. 33 - Loop Gain and Phase

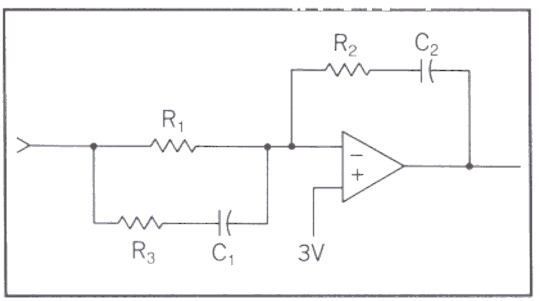

Fig. 34 - E/A Compensation Network

around or above the overall zero dB crossover point. The required error amplifier response can now be approximated graphically from the curve and points plotted.

In this example, two zeros will be introduced in the error amplifier response near the output filter break frequency of 1.25 kHz. A pole is located near the zero dB crossover point at 50 kilohertz. The actual gain and phase obtained in the overall loop is given in Fig. 33.

The error amplifier with its compensation network is shown in Fig. 34. It provides high gain at low frequencies and good transient response.

Zero 1 : $1/(2\pi R_1 C_1)$

Zero 2 : $1/(2\pi R_2 C_2)$

Pole 1 : $1/(2\pi R_3 C_1)$

Max Gain : $R_2/(R_1$ & R_3 in parallel)

Input impedance is the parallel combination of R_1, R_2, and R_3.

The compensation network is designed to produce:

Zero 1 and Zero 2 at 1.25 kHz

Pole 1 at 70 KHz

> 55 dB loop gain at 50 kHz

Using the previous equations and solving:

R_1 = 6.03K R_2 = 78.1K R3 = 100 Ω

C_1 = 22 nF C_2 = 1.7 nF

From the Bode plot of the closed loop response, the supply is compensated to cross 0 dB at approximately 35 kHz, with ample phase margin.

Power Supply Performance

This 150 watt power supply was evaluated while being exercised over various line and load conditions, and exhibited excellent regulation. Response to dynamic loading was well within reasonable limits with little overshoot. Short circuit input current is extremely low, due to the programmed restart delay time constant of 50 milliseconds and soft start of 5 milliseconds.

High efficiency (above 80 %) is achieved over the operating ranges. This is quite respectable for a high frequency, off-line power supply. The power stage was constructed on a double sided printed circuit board used for a previous high frequency example (1.5 MHZ current mode) in 1986.

The control circuit is constructed on the Unitrode UC3860 development PC board. The utilization of a ground plane precedes all circuit layout in megaHertz switch mode power designs, and is incorporated here. Coaxial cable interconnects the gate drive, current sense and output voltage signals between the control and power boards. Observation of the circuit waveforms requires the use of a UHF type scope probe socket, or chassis socket. Any length of ground or hook-up wire will distort the true waveforms.

Summary

Above several hundred kiloHertz, the square wave converter may not be optimal for off line designs. Losses associated with switching high voltages at high currents substantially reduce efficiency, power density and generate much EMI. The need for an alternative solution have resulted in various resonant and quasi-resonant approaches, each with a unique

set of merits, applications and control circuit requirements.

The UC3860 controller has integrated the numerous specific functions and "building blocks" required for resonant and quasi-resonant topologies. Configuration for fixed on-time, variable frequency operation is straightforward, and other adaptations are easily made possible. The uncommitted comparator interfaces well with zero current type switching arrangements. The UC3860's high speed logic, high power outputs and fault protection circuitry combine for an ideal mix of brains, brawn and speed.

REFERENCES

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M5 Power Transformer Design For Switching Power Supplies
M2 Winding Data
C1 Closing The Feedback Loop and Appendices

Other Unitrode Papers:

W. Andreycak, "3 Megahertz Resonant Mode Control IC Regulates 150 Watt Off-Line Supply", *High Frequency Power Conference*, 1988.

R. Mammano, "Resonant Mode Converter Topologies", *Unitrode Power Supply Design Seminar SEM600, Topic 1*", 1988

L. Wofford, "UC1860 - New IC Controls Resonant Mode Power Circuits", *Applied Power Electronics Conference,* 1988

Additional References:

P. Vinciarelli, "Forward Converter Switching At Zero Current", *U.S. Patent # 4,415,959*

Intertec Communications Press, "Recent Developments In Resonant Power Conversion", 1988 (628 pages - various papers and authors)

Resonant Circuits - "Rust Remover" and Appendix

The abrupt transition from conventional square wave conversion to a resonant or quasi-resonant approach can be softened by a review of certain fundamentals. Fig. A1 shows the sine and cosine waveforms along with the timing relationships.

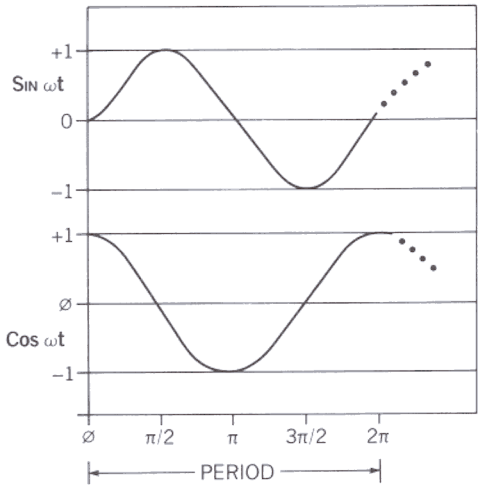

Fig. A1 - Sine, Cosine Relationships

Frequency = $\omega/2\pi$

$T_{period} = 1/f = 2\pi/\omega$

More specific to power conversion, a series resonant LC network driven by a DC voltage source is presented with its corresponding waveforms and equations in Figs. A2 and A3.

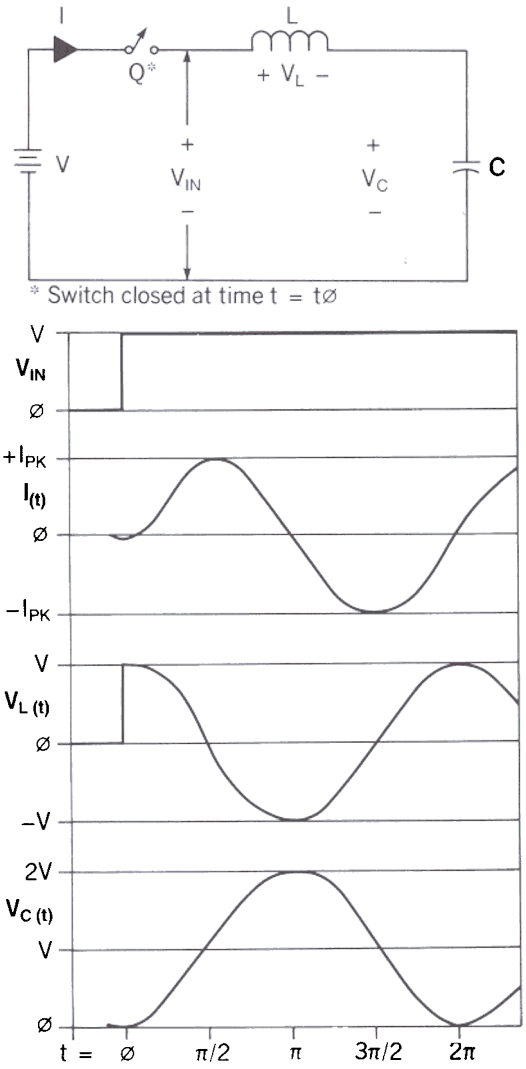

Fig. A2, A3 - Series Resonant Circuit

$\omega = 1/(LC)^{1/2}$, $Z_r = (L/C)^{1/2}$

$i_{pk} = V_{IN}/Z_r$

$i = i_{pk} \sin(\omega t) = V_{IN} \sin(\omega t)/Z_r$

$v_L = V_{IN} \cos(\omega t)$

$v_C = V_{IN} [1-\cos(\omega t)]$

Resonant circuit timing relationships and waveforms: The waveforms of a series resonant, parallel loaded circuit will be analyzed in detail and used to generate the relationships between time, current, charge and energy transfer in a resonant circuit application. Specifically, the buck topology will be used in this example, which can be applied to other topologies and configurations.

The cycle is initiated at time t_0. Switch Q_1 closes, delivering a rectangular voltage waveform to the resonant circuit. The input current rises linearly to I_{out} at a slope equal to V_{IN}/L_r. It reaches the constant output current level I_{out} at time t_1. The time for this to occur is $\Delta t_{10} = (t_1-t_0)$. During this interval, all resonant inductor current is directed to the output and none delivered to the resonant capacitor, C_r.

At t_0:

$$i_{in} = 0,\ i_{Cr} = 0,\ v_{Cr} = 0$$

From t_0 to t_1,

$$i_{in} = V_{IN}t/L_r$$

At t_1, $i_{in} = I_{out}$

$$\Delta t_{10} = L_r I_{out}/V_{IN}$$

At time t_1, the input current equals the fixed current I_{out}. The resonant L_r & C_r tank components begin their resonant cycle at zero current, and the input current rises sinusoidally to its peak of $I_{out} + V_{IN}/Z_r$. It will later intersect the output current I_{out} again at time t_2, corresponding to 1/2 the resonant tank period, π radians.

At t_1:

$$i_{in} = I_{out},\ i_{Cr} = 0,\ v_{Cr} = 0$$

From t_1 to t_2:

$$i_{in} = I_{out} + (V_{IN}/Z_r)\sin\omega(t-t_1)$$

$$\Delta t_{21} = \pi/\omega = 1/(2f) = 1/\pi(L_rC_r)^{1/2}$$

$$i_{Cr} = \frac{V_{IN}}{Z_r}\sin\omega(t-t_1)$$

$$v_{Cr} = V_{IN}(1-\cos\omega(t-t_1))$$

Once the input (inductor) current crosses I_{out} at time t_2 it continues sinusoidally until it reaches zero at time t_3. At this point, switch Q_1 is turned off to facilitate zero current switching. The time required to reach zero current from

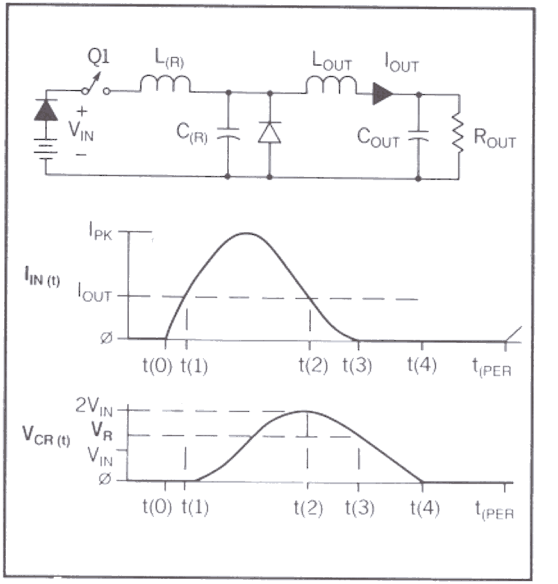

Fig. A4, A5 - Quasi-Resonant Buck Converter

I_{out} is Δt_{32}, and depends upon the amplitude of I_{out} and V_{IN}.

At t_2:

$$i_{in} = I_{out},\ i_r = 0,\ v_{Cr} \approx 2V_{in}$$

From t_2 to t_3:

$$\Delta t_{32} = \frac{1}{\omega}\sin^{-1}\left[\frac{I_{out}Z_r}{V_{in}}\right]$$

$$i_{in} = I_{out} + \frac{V_{IN}}{Z_r}\sin\omega(t-t_1)$$

$$v_{Cr} = V_{IN}(1-\cos\omega(t-t_1))$$

The resonant capacitor voltage v_{Cr} discharges linearly during the interval of Δt_{43}, beginning at time t_3. The capacitor voltage and Δt_{43} are determined from the following equations:

At t_3:

$$i_{in} = 0,\ i_{Cr} = 0$$

From t_3 to t_4:

$$v_{Cr} = v_{Cr(t3)} - I_{out}(t - t_3)/C_r$$

$$\Delta t_{43} = C_r v_{Cr(t3)}/I_{out}$$

Evident from the previous equations is the need to vary the output *on* time to respond to the various line, load and resonant tank circuit influences.

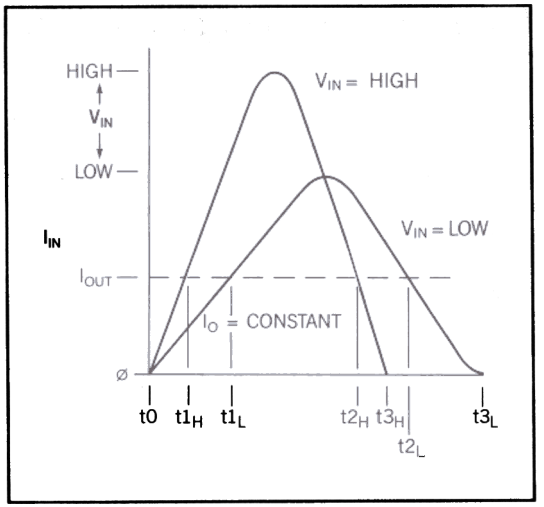

Fig. A6 - i_{in}, t_{on} vs. Line Variation

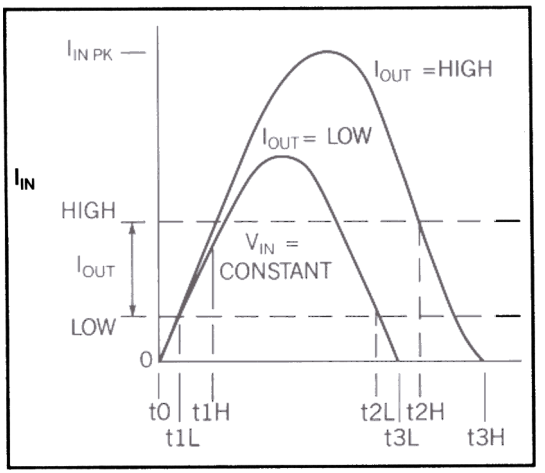

Fig. A7 - i_{in}, t_{on} vs. Load Variation

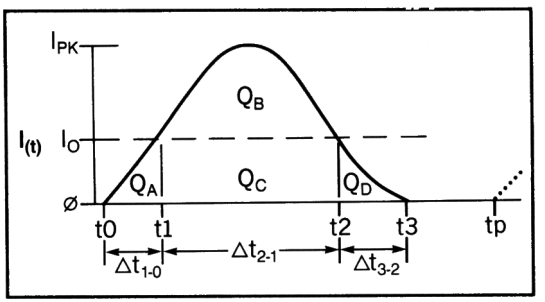

Fig. A8 - Charge Transfer

The conversion frequency or repetition rate at the input switch is approximated following some intermediate calculations for total energy transfer from input to output, as follows:

Charge Transfer in the Resonant Circuit

During each resonant cycle a specific amount of charge (Q) is taken from the input supply and transferred to the output load. The corresponding energy (watt-sec) transferred is simply the charge (Q) multiplied by the input voltage V_{IN}. This relationship will be used to approximate the conversion frequencies required to regulate an output voltage for various ranges of input voltages and output currents.

The input current waveform will be divided into four specific intervals to simplify the calculations. The charge transferred in each interval will be calculated by integrating the current waveform throughout the interval.

Q_a: The charge transferred during the time interval from t_0 to t_1 is calculated from the equation for the area of the triangle formed:

$$\Delta t_{1\text{-}0} = LI_o/V_{IN}$$

$$Q_a = \Delta t_{1\text{-}0} I_o/2 = LI_{out}^2/(2V_{IN})$$

Q_b: During this resonant half-period, the sinusoidal portion of the input current waveform is integrated over the interval t_1 to t_2.

$$i_{in} - I_{out} = (V_{IN}/Z_r)\sin\omega(t-t_1)$$

$$Q_b = \frac{V_{IN}}{Z_r}\int_{t1}^{t2}\sin(\omega(t-t_1))dt$$

$$Q_b = \frac{V_{IN}}{Z_r\omega}\left[-\cos\theta\right]_0^{\pi}$$

$$1/Z_r\omega = C_r$$

$$\therefore\ Q_b = 2V_{IN}C_r$$

Q_c: The rectangular area of charge delivered to the output during interval t_1 to t_2 is:

$$Q_c = I_{out}\Delta t_{21}, \text{ where } \Delta t_{21} = \pi/\omega$$

$$Q_c = \pi I_{out}/\omega$$

Q_d: The sinusoidal current decreases from I_{out} to zero during the t_2 to t_3 interval. The charge transferred is calculated by subtracting the sinusoidal component from the rectangular region formed by I_{out} and t_3.

$$Q_d = I_{out}\Delta t_{32} + I_r\int_{t2}^{t3}\sin(\omega(t-t_1))dt$$

$$Q_d = I_{out}\Delta t_{32} - \frac{V_{IN}}{Z_n\omega}\left[\cos\theta\right]_{\pi}^{\pi+\omega\Delta t_{32}}$$

$$Q_d = I_{out}\Delta t_{32} - V_{IN}C_r[\cos(\pi+\omega\Delta t_{32}) - \cos\pi]$$

$$\Delta t_{32} \approx (1/\omega)\sin^{-1}(I_{out}Z_n/V_{IN})$$

For practical purposes, this area can be represented by a linear approximation without a significant compromise in accuracy. The area formed by $I_{out}\Delta t_{32}/2$ is a reasonable estimate of the area, resulting in approximately 1% error in the total charge transferred.

$$Q_d \approx I_{out}\,\Delta t_{32}/2 = (1/2\omega)I_{out}\sin^{-1}(I_{out}Z_n/V_{IN})$$

Q_t: The total charge transferred from the input to the output per cycle is the summation of charges Q_a through Q_d.

$$Q_t = Q_a + Q_b + Q_c + Q_d$$

$$Q_t = \frac{LI_{out}^2}{2V_{IN}} + 2V_{IN}C_r + \frac{\pi I_{out}}{\omega} + \frac{I_{out}}{2\omega}\sin^{-1}\frac{I_oZ_n}{V_{IN}}$$

The approximation made to simplify the calculation of charge Q_d also allows the substitution of charge Q_a for Q_d, thus reducing the total charge transfer to the following:

$$Q_t = 2Q_a + Q_b + Q_c$$

$$Q_t = \frac{LI_{out}^2}{V_{IN}} + 2V_{IN}C_r + \frac{\pi I_{out}}{\omega}$$

Energy Transfer During the Resonant Cycle

The energy per cycle, W, can be calculated by multiplying the input voltage V_{IN} by the total charge Q_t transferred from the input to the output. Dividing the energy per cycle W by the output power P_{out} unveils the conversion period – the inverse of the switching frequency.

$$T_{conv} = \frac{W/cycle}{P_{out}} = \frac{V_{IN}\,Q_t}{V_{out}I_{out}}$$

$$= \frac{V_{IN}}{V_{out}I_{out}}(Q_a+Q_b+Q_c+Q_d)$$

$$= \frac{V_{IN}}{V_{out}I_{out}}(2Q_a+Q_b+Q_c)$$

$$T_{conv} \approx \frac{V_{IN}}{V_{out}I_{out}}\left[\frac{L_rI_{out}^2}{V_{IN}} + 2V_{IN}C_r + \frac{\pi I_{out}}{\omega}\right]$$

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