Projet 4 - SA828 / Générateur MLI triphasé en U/f à base de ST52E420 d'après P. MISSIRLIU

Projet : IUT2

Info : [DIV359]

Révision : 1, du 29 septembre 2002

Révision : 2, du 13 octobre 2002

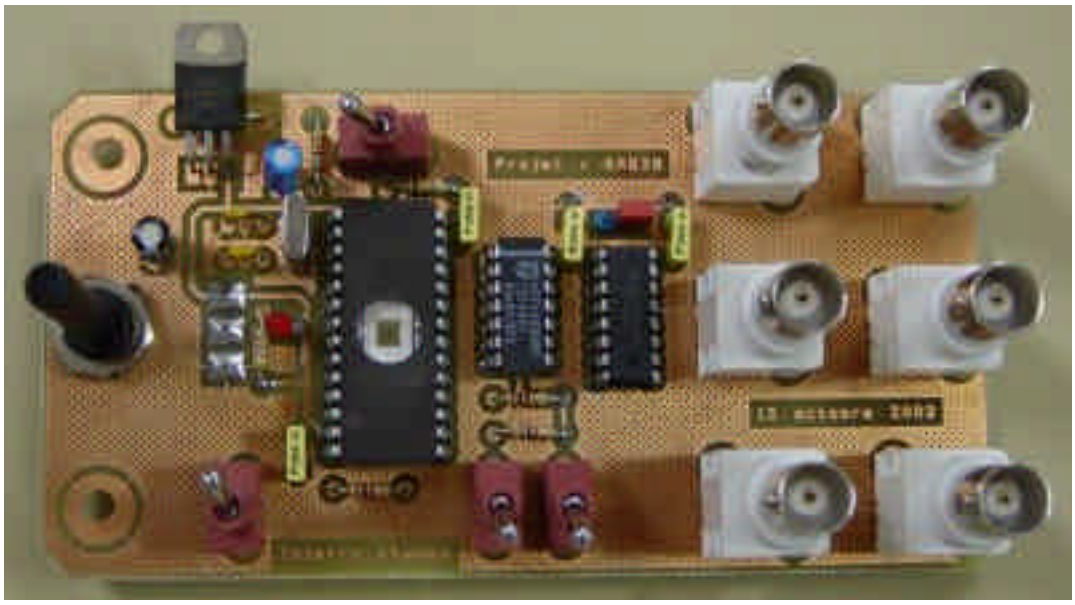


Figure 4.1. Vue du circuit imprimé (images-maquettes\sa828-h2.jpg).

4.1 Liste des documents

- Désignation des composants
- Prix du montage.
- Schéma électronique.
- Circuit imprimé coté cuivre.
- Circuit imprimé coté composants.
- Implantation des composants.
- Documentations.

4.2 Désignation des composants

Tableau 4.1. Liste de composants (projets-iut2.xls / SA828).

N°	Quantité	Référence	Désignation	Empreinte
1	2	C1,C2	10 pF	CK05-3
2	1	C3	1uF	RADIAL06
3	1	C4	10 uF 25V	RADIAL06
4	4	C5,C6,C7,C8	100nF	CK06
5	1	DIV1	20 MHz	HC18UV
6	1	DIV2	+15V	EMBASE
7	1	DIV3	GND	EMBASE
8	1	D1	1N400x	DO41
9	1	D2	3mm	LED3
10	1	JP1	TENSION	03PC1
11	1	JP2	BOT1	BNC-V
12	1	JP3	TOP1	BNC-V
13	1	JP4	BOT2	BNC-V
14	1	JP5	TOP2	BNC-V
15	1	JP6	BOT3	BNC-V
16	1	JP7	TOP3	BNC-V
17	1	P1	1k	POT-SUR-CARTE
18	4	R1,R2,R3,R5	1k	RC04
19	1	R4	100k	RC04
20	1	R6	470	RC04
21	1	SW1	AV/AR	SY230
22	1	SW2	Select1	SY230
23	1	SW3	select2	SY230
24	1	SW4	BP RESET	SY230
25	1	U1	ST52E420	28DIP600L
26	1	U2	4069	14DIP300L
27	1	U3	4504	16DIP300
28	1	U4	7805	TO220

4.3 Implantation mécanique

Figure 4.2. Vue du boîtier (images-maquettes\sa828-d2.jpg).

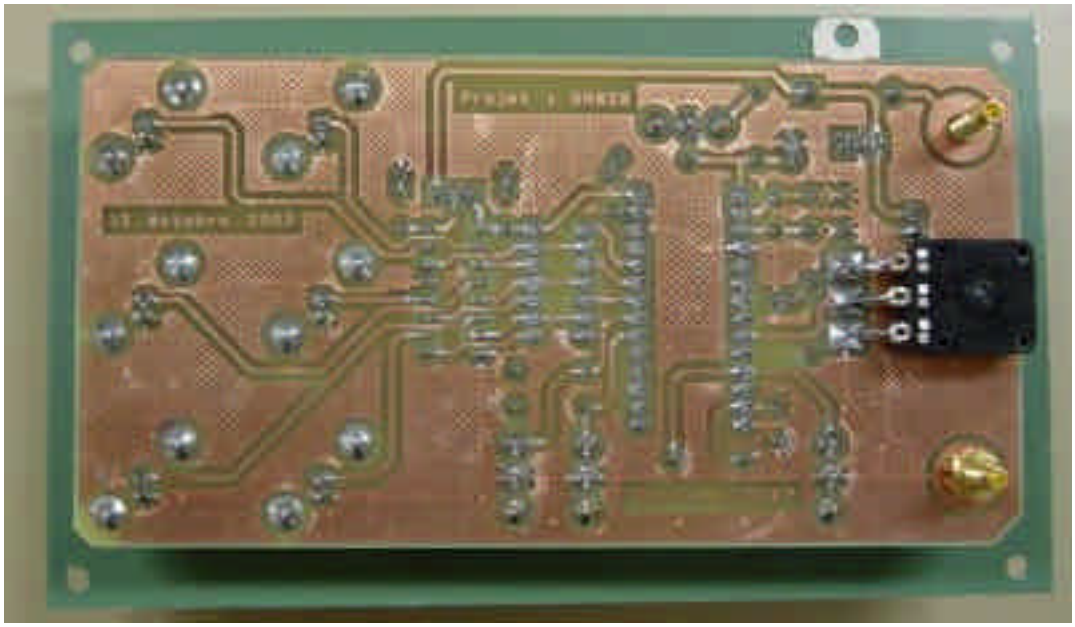


Figure 4.3. Vue du circuit imprimé coté cuivre (images-maquettes\sa828-e2.jpg).

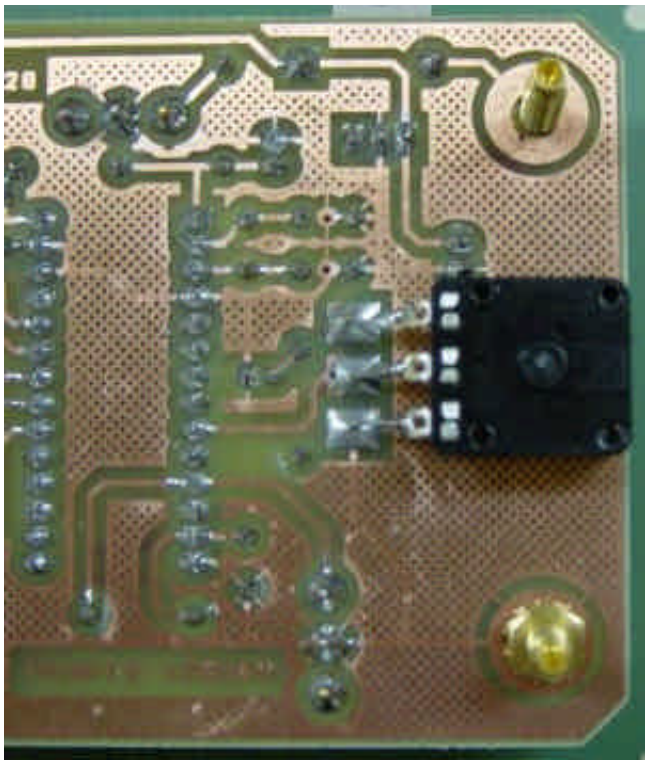


Figure 4.4. Montage du potentiomètre (images-maquettes\sa828-f2.jpg).

4.4 Le courrier de Philippe MISSIRLIU

Vous trouverez ci joint:

- Trois exemplaires de microcontrôleurs STS2E420 programmés en pseudo SA828 ;
- Le schéma de la carte avec laquelle je les ai vérifiés (la partie puissance étant réalisée avec des drivers SKHI22 de SEMIKRON) ;
- Mes notes manuscrites rédigées lors de la conception du programme.

Le brochage du STS2E420 programmé est le suivant :

- PBO : consigne fréquence ;
- PB 1 : réservé pour extension, configuré en entrée analogique ;
- PB2 : sens de rotation ;
- PA4 et PA5, configuration du circuit.

PA4	Référence	PA5	Fréquence de la porteuse
0	Sinus	0	4,9 kHz
1	Sinus + harmonique 3	1	l,2 kHz

Je reste à votre disposition pour toute information complémentaire.

Cordialement.

Philippe MISSIRLIU

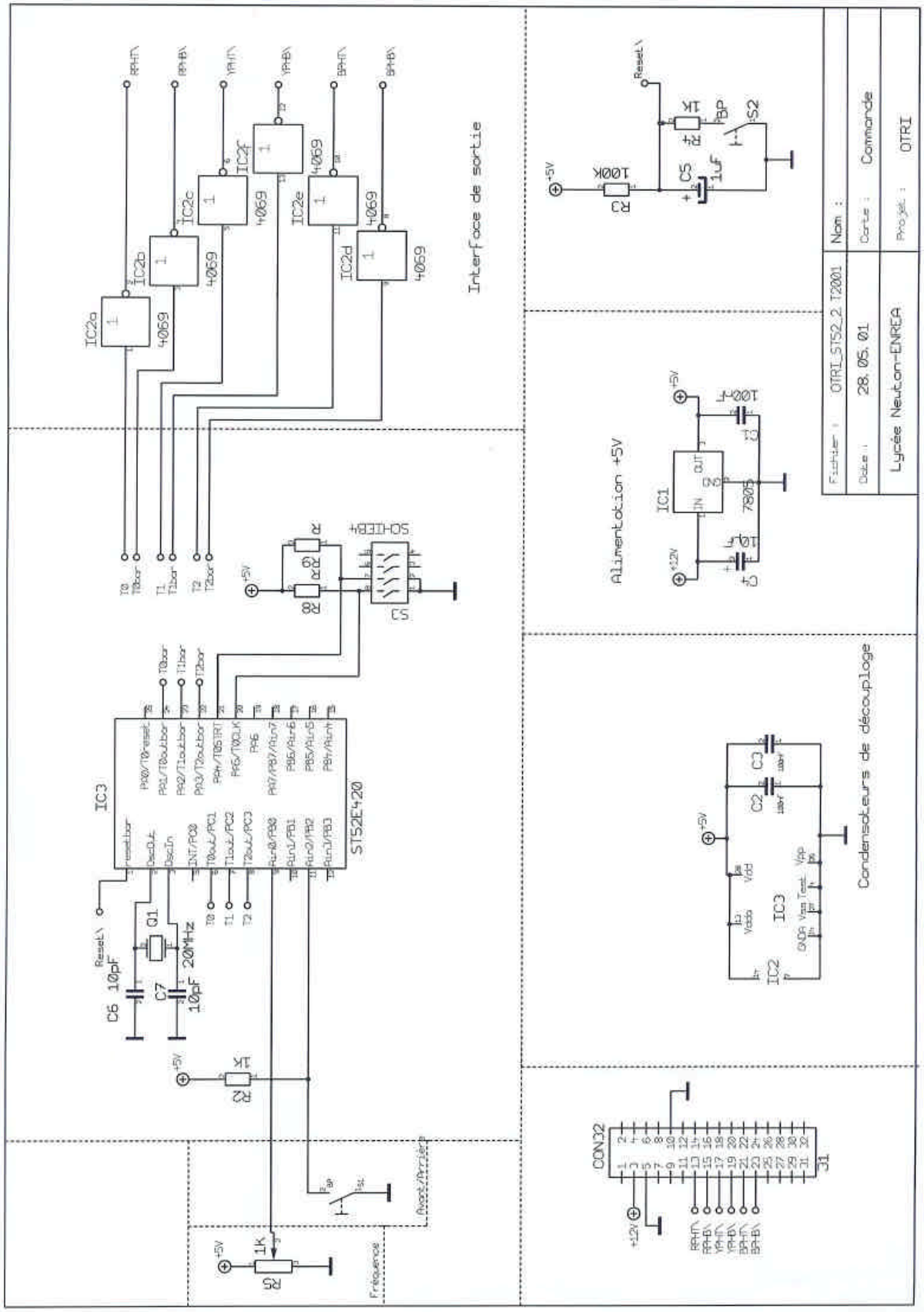


Figure 4.5. Schéma de test (images-maquettes\sa828-11.jpg).

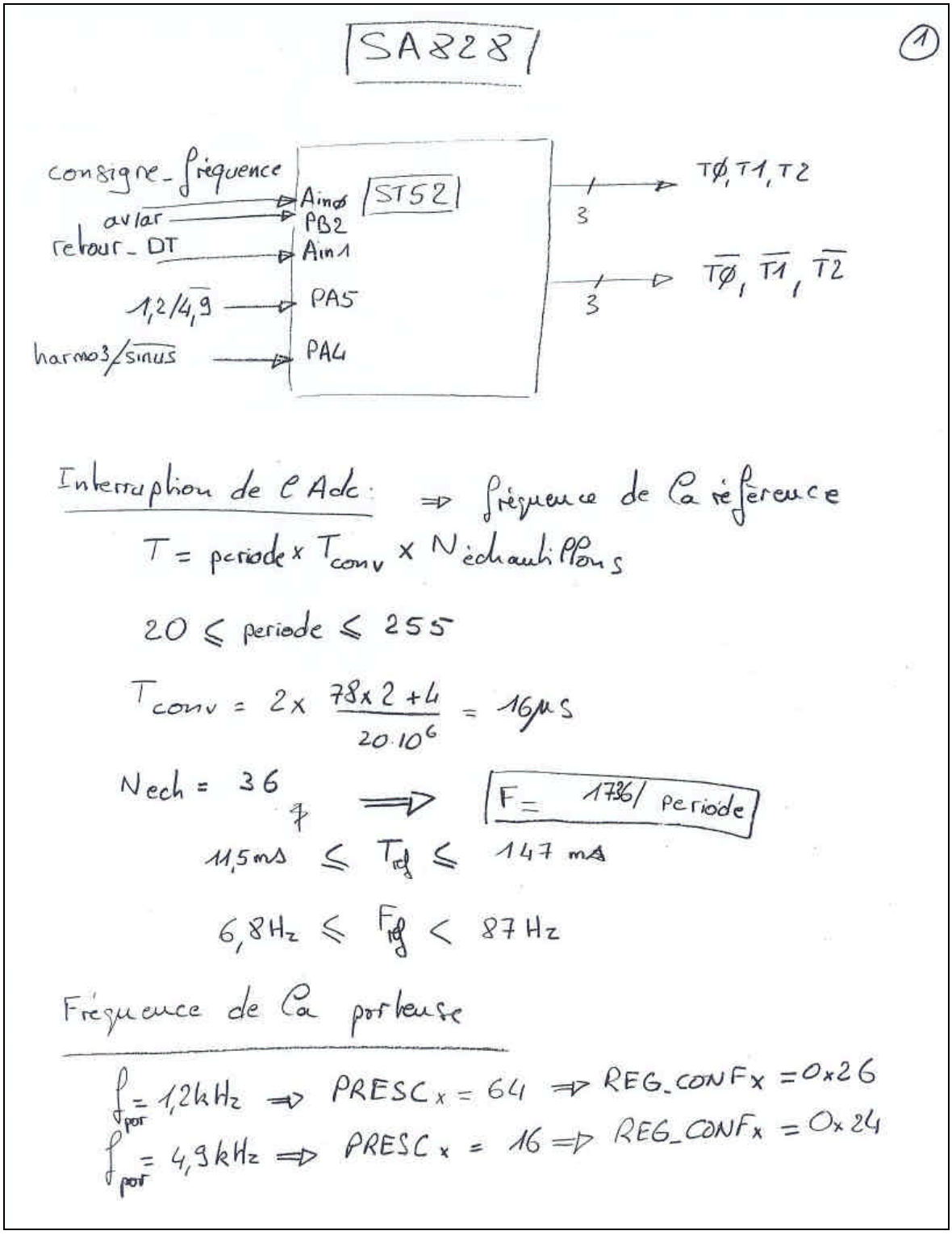


Figure 4.6. Brouillon de programmation N° 1 (images-maquettes\sa828-21.jpg).

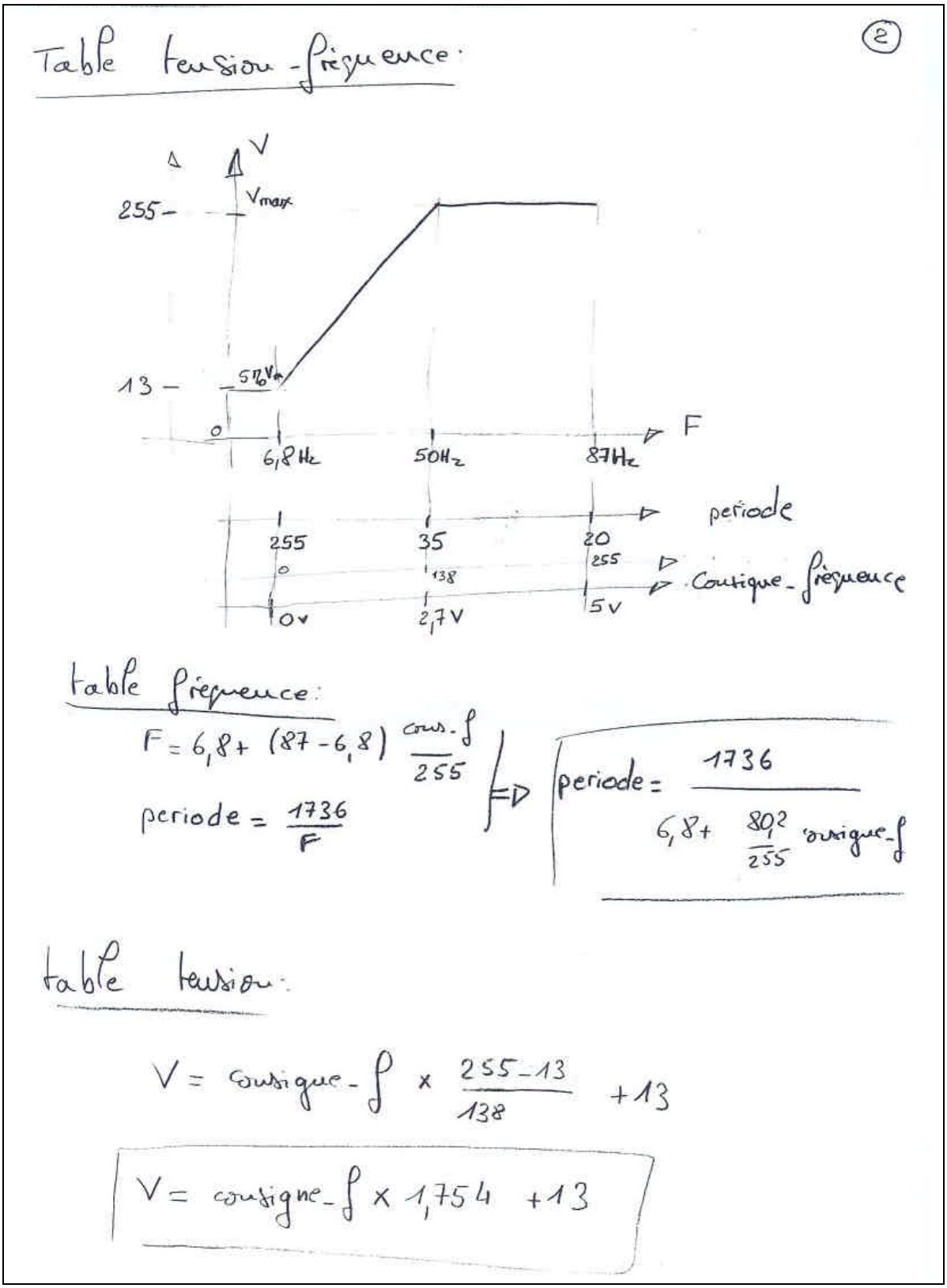


Figure 4.7. Brouillon de programmation N° 2 (images-maquettes\sa828-31.jpg).

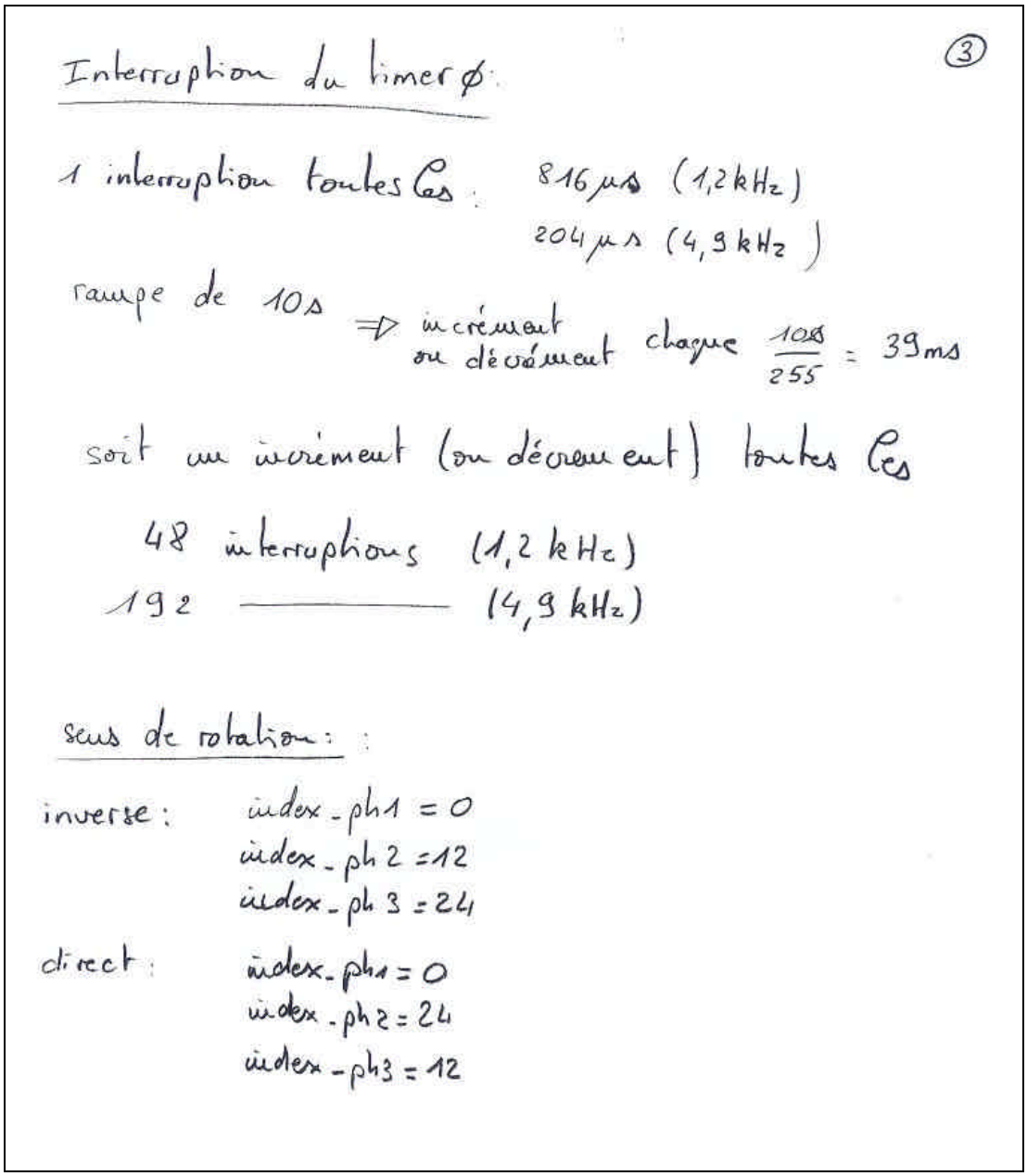


Figure 4.8. Brouillon de programmation N° 3 (images-maquettes\sa828-41.jpg).

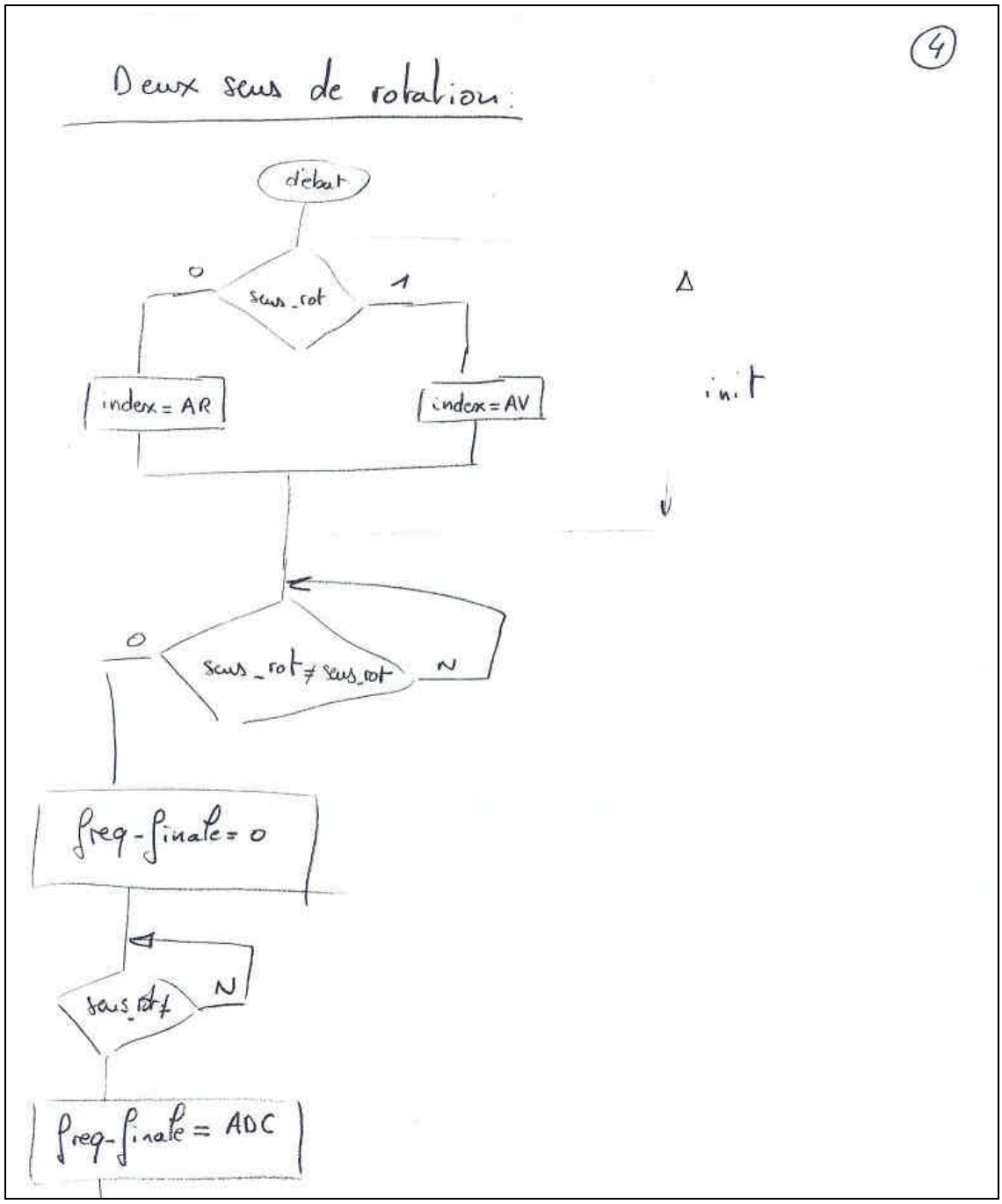


Figure 4.9. Brouillon de programmation N° 4 (images-maquettes\sa828-51.jpg).

Commande MLI triphasé pour moteur asynchrone

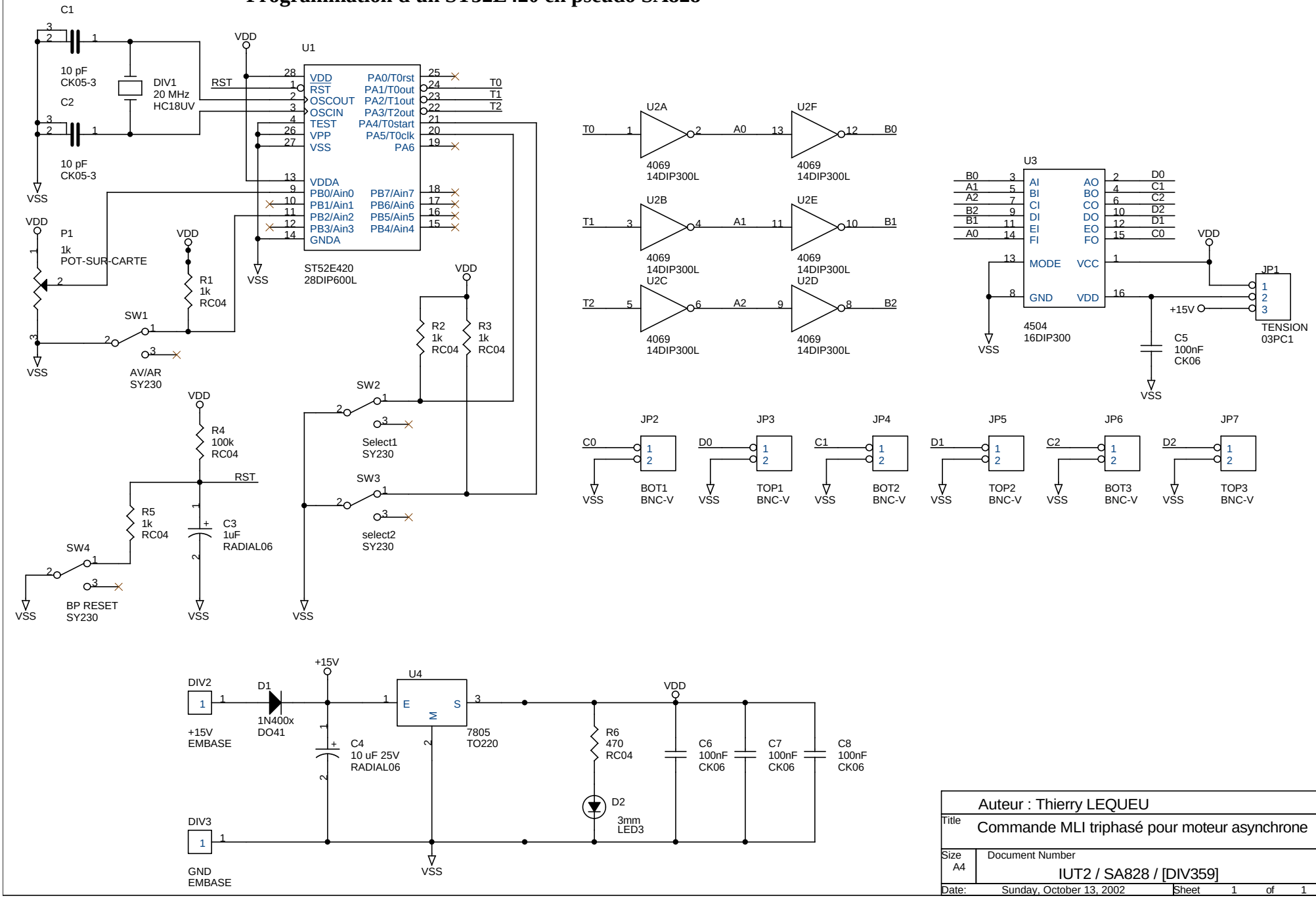
Revised: Sunday, October 13, 2002

IUT2 / SA828 / [DIV359] Revision: 2

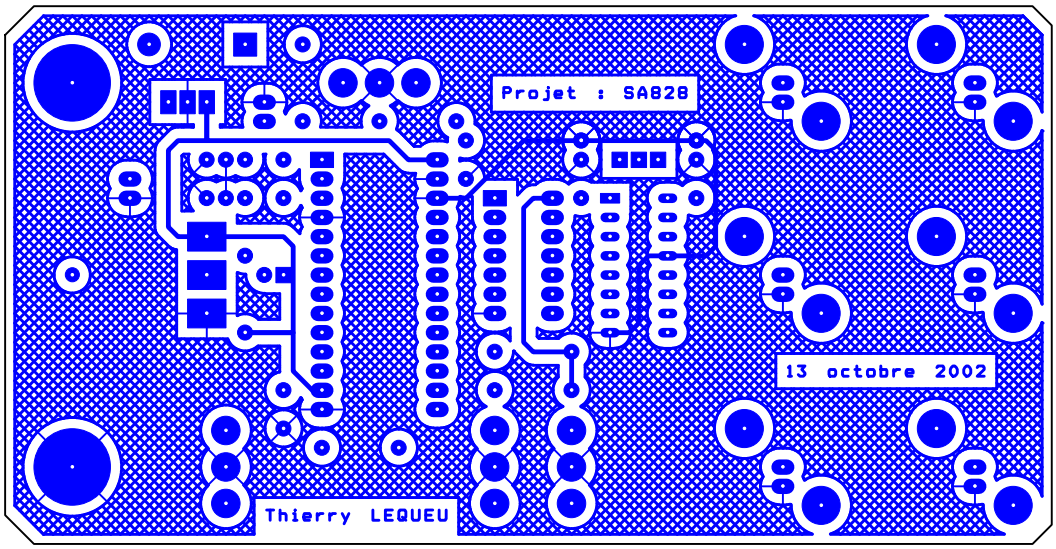
Référence	Qu.	Désignation	Fournisseur	Date	Code Cde.	U.d.V.	Prix U.	Prix T.
DIV2	1	Douille double isolation à visser rouge	Radiospares	20-avr-02	230-6344	1	, €	, €
DIV3	2	Douille double isolation à visser noire	Radiospares	20-avr-02	230-6350	1	, €	, €
C5,C6,C7,C8	4	100nF MKT 63V	Radiospares	20-avr-02	166-8348	10	, €	, €
B1, B3, JP4, JP5, JP6	5	Douille double isolation à visser jaune	Radiospares	20-avr-02	230-6372	1	, €	, €
C1,C2	2	10 pF	Radiospares	20-avr-02	230-6388	1	, €	, €
C3	1	, uF V série M	Radiospare	20-avr-02	228-6868	5	, €	, €
C4	1	uF V série M	Radiospare	20-avr-02	228-6751	5	, €	, €
D1	1	1N4001	Radiospares	20-avr-02	261-148	10	, €	, €
D2	1	LED rouge 3 mm	Radiospare	20-avr-02	171-1234	10	, €	, €
P1	1	Potemtiomêtre KA	Radiospare	20-avr-02	387-414	1	, €	, €
JP2 - JP7	6	BNC vertical	Radiospare	13-oct-02	196-2820	1	, €	, €
R1,R2,R3,R	4	1k	IUT GEII			1	, €	, €
R4	1	100k	IUT GEII			1	, €	, €
R6	1	470	IUT GEII			1	, €	, €
SW1	1	AV/AR	Radiospare	13-oct-02	352-761	1	, €	, €
SW2	1	Select1	Radiospare	13-oct-02	352-761	1	, €	, €
SW3	1	select2	Radiospare	13-oct-02	352-761	1	, €	, €
SW4	1	BP RESET	Radiospare	13-oct-02	352-761	1	, €	, €
U1	1	ST52E420	IUT GEII			1	, €	, €
U2	1	4069	IUT GEII			1	, €	, €
U3	1	4504	IUT GEII			1	, €	, €
U4	1	7805	IUT GEII			1	, €	, €
Divers	1	Support 14 broches tulipe	Radiospare	13-oct-02	100-9941	10	, €	, €
Divers	1	Support 16 broches tulipe	Radiospare	13-oct-02	100-9957	10	, €	, €
Divers	1	Support 28 broches tulipe	Radiospare	13-oct-02	10-9991	10	, €	, €
Divers	171	Circuit imprimé SF x	Radiospare	13-oct-02	159-6091	600	, €	, €
Divers	1	Boitier type P3	IUT GEII	13-oct-02		1	, €	, €
Divers						1		, €

TOTAL H.T. :	, €
dont TVA : 19,60%	, €
TOTAL T.T.C. :	**, €**

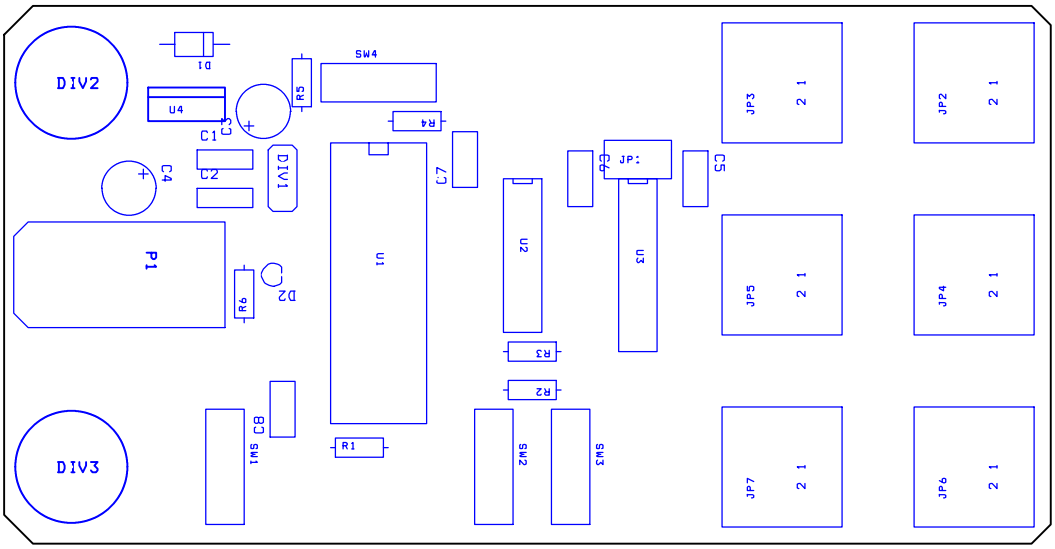
D'aprés Philippe MISSIRLIU
Programmation d'un ST52E420 en pseudo SA828

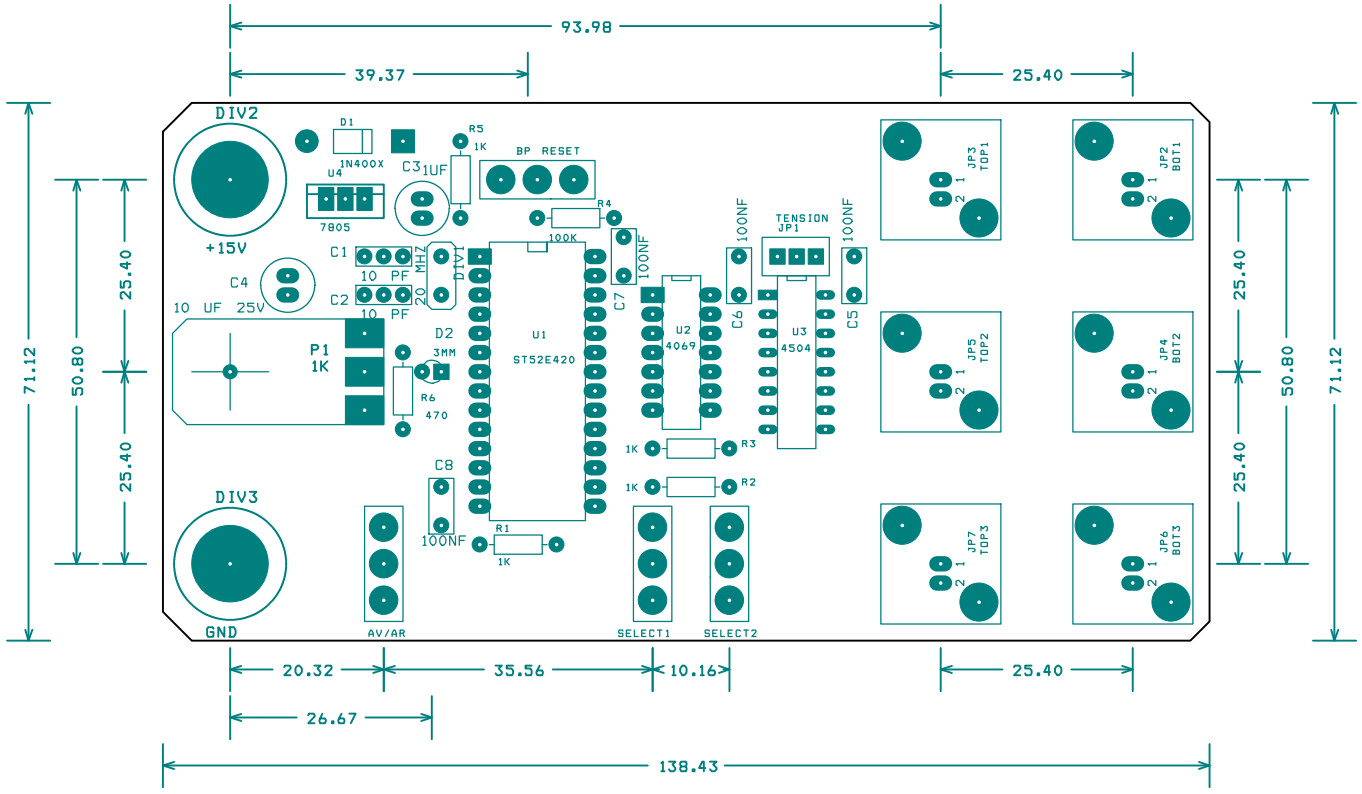


Auteur : Thierry LEQUEU			
Title	Commande MLI triphasé pour moteur asynchrone		
Size A4	Document Number IUT2 / SA828 / [DIV359]		Rev 2
Date: Sunday, October 13, 2002	Sheet 1 of 1		


Projet : SA828
13 octobre 2002
Thierry LEQUEU

Projet : SAB2B
13 octobre 2002
Thierry LEDUEU


DIV2
DIV3
D1
U4
C1
C3
SW4
R5
R4
C2
DIV1
C4
P1
R6
D2
U1
C7
U2
C6
JP:
U3
C5
JP3
JP2
JP5
JP4
JP7
JP6
R3
R2
R1
SW1
C8
SW2
SW3


93.98
39.37
25.40
DIV2
+15V
D1
1N400X
U4
7805
C3
1UF
R5
1K
BP RESET
R4
100K
C1
10 PF
20 MHZ
DIV1
C2
10 PF
C4
10 UF 25V
P1
1K
D2
3MM
R6
470
U1
ST52E420
C8
100NF
R1
1K
C7
100NF
U2
4069
C6
100NF
TENSION
JP1
U3
4504
C5
100NF
R3
1K
R2
1K
JP3
TOP1
JP2
BOT1
JP5
TOP2
JP4
BOT2
JP7
TOP3
JP6
BOT3
DIV3
GND
AV/AR
SELECT1
SELECT2
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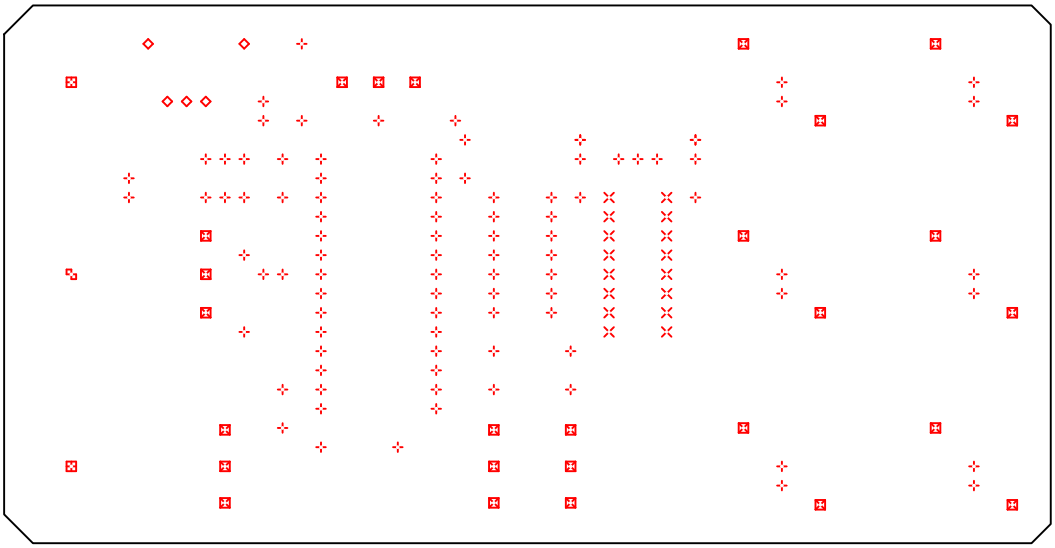
20.32
35.56
10.16
25.40
26.67
138.43



DRILL CHART				
SYM	DIAM	TOL	QTY	NOTE
×	0.610 mm		16	
+	0.787 mm		93	
◇	0.991 mm		5	
⊠	1.499 mm		27	
⊞	4.191 mm		2	
⧉	10.160 mm		1	
TOTAL			144	

ST52T420/E420

8-BIT INTELLIGENT CONTROLLER UNIT (ICU)
Three Timer/PWMs, ADC, WDG

BRIEF DATASHEET

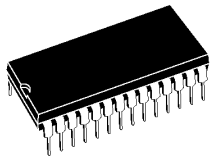
Memories
- Up to 4 Kbytes OTP
- 128 bytes of RAM
- Readout Protection

Core
- Register File Based Architecture
- 55 instructions
- Hardware multiplication and division
- Decision Processor for the implementation of Fuzzy Logic algorithms

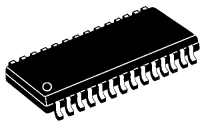
Clock and Power Supply
- Up to 20 MHz clock frequency.
- Power Saving features

Interrupts
- 5 interrupt vectors
- Top Level External Interrupt (INT)

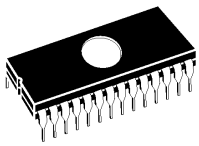
I/O Ports
- 19 I/O PINs configurable in Input and Output mode
- High current sink/source in all pins.



PDIP28



SO28

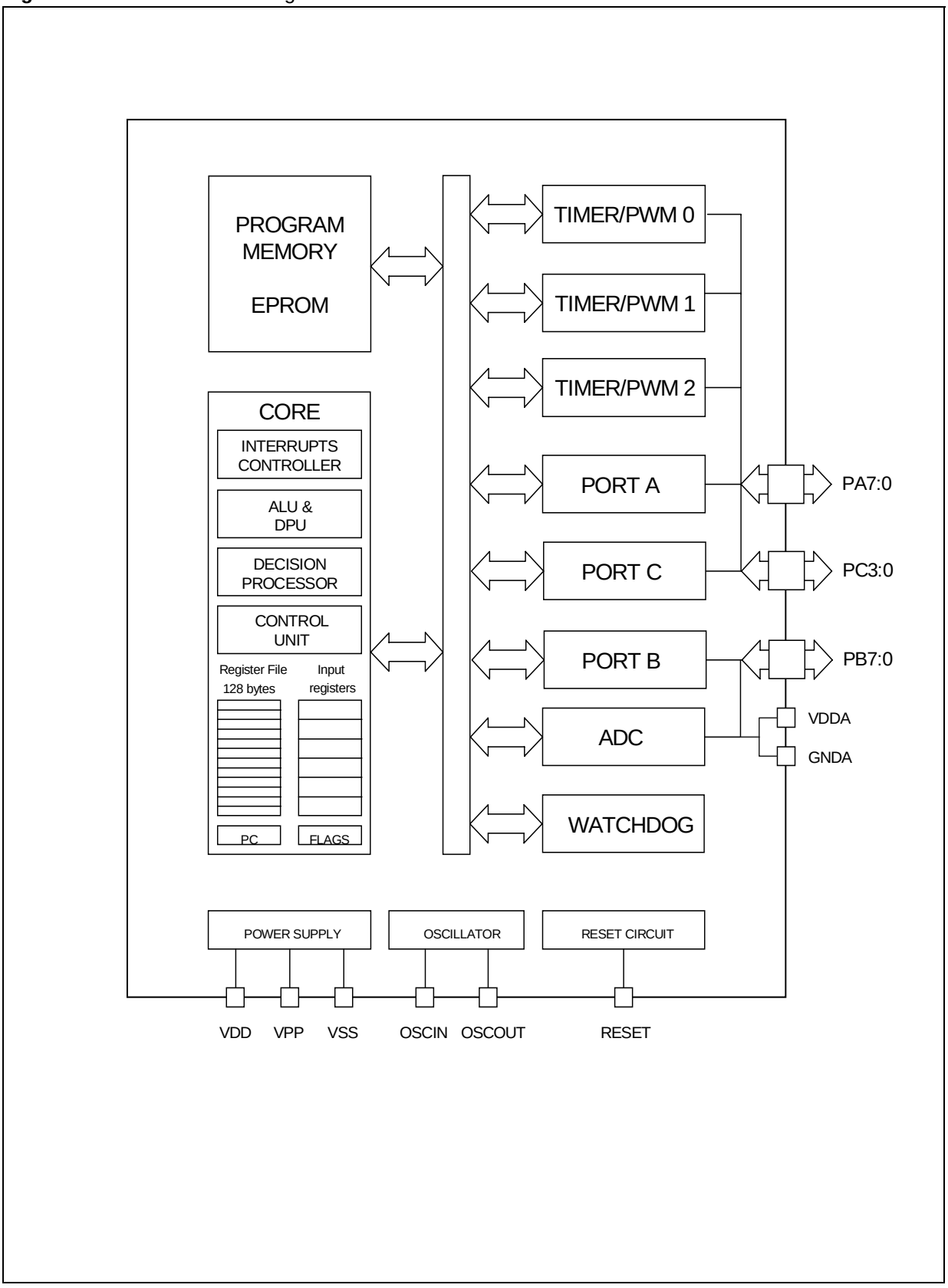


CDIP28W

Peripherals
- 3 Programmable 8-bit Timer/PWMs with internal 16-bit Prescaler featuring:
  - PWM output
  - Input capture
  - Output compare
  - Pulse generator mode
- On-chip 8-bit Sample and Hold A/D Converter with 8-channel analog multiplexer
- Watchdog timer

Development tools
- High level Software tools
- Emulator
- Low cost Programmer
- Gang Programmer

Figure 1. ST52x420 Block Diagram

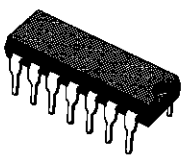


SGS-THOMSON MICROELECTRONICS

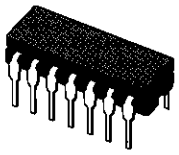
HCC/HCF4069UB

HEX INVERTER

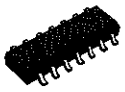
- MEDIUM-SPEED OPERATION
  – t_{PHL}, t_{PLH} = 30ns (typ.) AT 10V
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



EY
(Plastic Package)



F
(Ceramic Frit Seal Package)



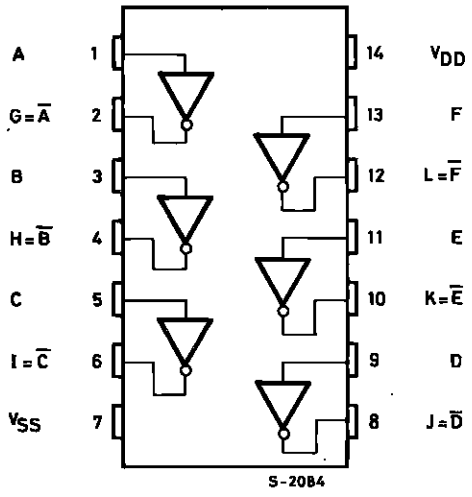
M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

HCC4069UBF	HCF4069UBM1
HCF4069UBEY	HCF4069UBC1

PIN CONNECTIONS



DESCRIPTION

The **HCC4069UB** (extended temperature range) and **HCF4069UB** (intermediate temperature range) are monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package and plastic micro package.

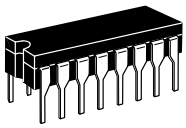
The **HCC/HCF4069UB** consists of six COS/MOS inverter circuits. This device is intended for all general-purpose inverter applications where the medium-power TTL-drive and logic-level-conversion capabilities of circuits such as **HCC/HCF4049B** Hex Inverter/Buffers are not required.

MC14504B

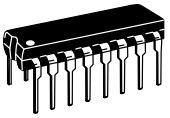
Hex Level Shifter for TTL to CMOS or CMOS to CMOS

The MC14504B is a hex non–inverting level shifter using CMOS technology. The level shifter will shift a TTL signal to CMOS logic levels for any CMOS supply voltage between 5 and 15 volts. A control input also allows interface from CMOS to CMOS at one logic level to another logic level: Either up or down level translating is accomplished by selection of power supply levels V_{DD} and V_{CC}. The V_{CC} level sets the input signal levels while V_{DD} selects the output voltage levels.

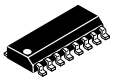
- UP Translates from a Low to a High Voltage or DOWN Translates from a High to a Low Voltage
- Input Threshold Can Be Shifted for TTL Compatibility
- No Sequencing Required on Power Supplies or Inputs for Power Up or Power Down
- 3 to 18 Vdc Operation for V_{DD} and V_{CC}
- Diode Protected Inputs to V_{SS}
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



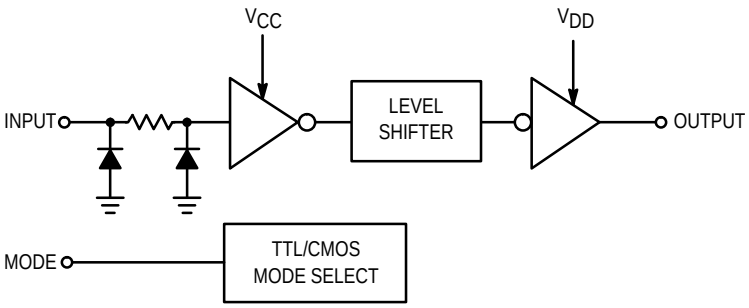
D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

T_A = – 55° to 125°C for all packages.

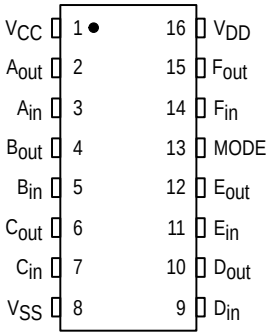
LOGIC DIAGRAM



Mode Select	Input Logic Levels	Output Logic Levels
1 (V_{CC})	TTL	CMOS
0 (V_{SS})	CMOS	CMOS

1/6 of package shown.

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields referenced to the V_{SS} pin, only. Extra precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, the ranges $V_{SS} \le V_{in} \le 18$ V and $V_{SS} \le V_{out} \le V_{DD}$ are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

REV 3
1/94