70A, 30V, 0.010 Ohm, N-Channel Power MOSFETs

These N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA49025.

Features

- 70A, 30V
- \( r_{DS(on)} = 0.010 \Omega \)
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve (Single Pulse)
- 175°C Operating Temperature
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

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<td>RFP70N03</td>
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<tr>
<td>RF1S70N03SM</td>
<td>TO-263AB</td>
<td>F1S70N03</td>
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</table>

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in tape and reel, e.g., RF1S70N03SM9A

Packaging

JEDEC TO-220AB

JEDEC TO-263AB
Absolute Maximum Ratings  \( T_C = 25^\circ C \), Unless Otherwise Specified

<table>
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<tr>
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<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<tbody>
<tr>
<td>Drain to Source Voltage (Note 1)</td>
<td>( V_{DSS} )</td>
<td>( \text{Continuous (Figure 2)} ), ( \text{Pulsed Drain Current (Note 1)} ), ( \text{Power Dissipation} )</td>
<td>30</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Drain to Gate Voltage (( R_{GS} = 20, \Omega )) (Note 1)</td>
<td>( V_{DGR} )</td>
<td>-</td>
<td>30</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Gate to Source Voltage</td>
<td>( V_{GS} )</td>
<td>-</td>
<td>±20</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Drain Current</td>
<td>( I_D )</td>
<td>-</td>
<td>70</td>
<td>-</td>
<td>-</td>
<td>A</td>
</tr>
<tr>
<td>Pulsed Drain Current (Note 1)</td>
<td>( I_{DM} )</td>
<td>-</td>
<td>200</td>
<td>-</td>
<td>-</td>
<td>A</td>
</tr>
<tr>
<td>Pulsed Avalanche Rating</td>
<td>( E_{AS} )</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Figures 5, 13, 14</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>( P_D )</td>
<td>-</td>
<td>150</td>
<td>-</td>
<td>-</td>
<td>W</td>
</tr>
<tr>
<td>Derate Above 25(^{\circ}C)</td>
<td>( 1.0 )</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>W(^{\circ}C)</td>
</tr>
<tr>
<td>Operating and Storage Temperature</td>
<td>( T_J, T_{STG} )</td>
<td>-55 to 175</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>(^{\circ}C)</td>
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<tr>
<td>Maximum Temperature for Soldering</td>
<td>( T_L )</td>
<td>300</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>(^{\circ}C)</td>
</tr>
<tr>
<td>Package Body for 10s, see Techbrief 334</td>
<td>( T_{pkg} )</td>
<td>260</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>(^{\circ}C)</td>
</tr>
</tbody>
</table>

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
1. \( T_J = 25^\circ C \) to 150\(^{\circ}C\).

Electrical Specifications  \( T_C = 25^\circ C \), Unless Otherwise Specified

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<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain to Source Breakdown Voltage</td>
<td>( B_{V_{DSS}} )</td>
<td>( I_D = 250\mu A, V_{GS} = 0V ) (Figure 10)</td>
<td>30</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Gate to Source Threshold Voltage</td>
<td>( V_{GS(TH)} )</td>
<td>( V_{GS} = V_{DS}, I_D = 250\mu A ) (Figure 9)</td>
<td>2</td>
<td>-</td>
<td>4</td>
<td>V</td>
</tr>
<tr>
<td>Zero Gate Voltage Drain Current</td>
<td>( I_{DSS} )</td>
<td>( V_{DS} = 30V, V_{GS} = 0V )</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{DS} = 30V, V_{GS} = 0V, T_C = 150^\circ C )</td>
<td>-</td>
<td>-</td>
<td>50</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Gate to Source Leakage Current</td>
<td>( I_{GSS} )</td>
<td>( V_{GS} = \pm 20V )</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>Drain to Source On Resistance</td>
<td>( r_{DS(ON)} )</td>
<td>( I_D = 70A, V_{GS} = 10V ) (Figure 8)</td>
<td>-</td>
<td>-</td>
<td>0.010</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>Turn-On Time</td>
<td>( t_{ON} )</td>
<td>( V_{DD} = 15V, I_D = 70A, R_L = 0.214\Omega, V_{GS} = 10V, R_{GS} = 2.5\Omega )</td>
<td>-</td>
<td>-</td>
<td>80</td>
<td>ns</td>
</tr>
<tr>
<td>Turn-On Delay Time</td>
<td>( t_{d(ON)} )</td>
<td>-</td>
<td>20</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Rise Time</td>
<td>( t_r )</td>
<td>-</td>
<td>20</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Turn-Off Delay Time</td>
<td>( t_{d(OFF)} )</td>
<td>-</td>
<td>40</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Fall Time</td>
<td>( t_f )</td>
<td>-</td>
<td>25</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Turn-Off Time</td>
<td>( t_{OFF} )</td>
<td>-</td>
<td>125</td>
<td>-</td>
<td>-</td>
<td>ns</td>
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<tr>
<td>Total Gate Charge</td>
<td>( Q_{g(TOT)} )</td>
<td>( V_{GS} = 0V ) to 20V ( V_{DD} = 24V, I_D = 70A, R_L = 0.343\Omega, I_{g(REF)} = 1.0mA ) (Figure 12)</td>
<td>-</td>
<td>215</td>
<td>260</td>
<td>nC</td>
</tr>
<tr>
<td>Gate Charge at 10V</td>
<td>( Q_{g(10)} )</td>
<td>( V_{GS} = 0V ) to 10V ( V_{DD} = 24V, I_D = 70A, R_L = 0.343\Omega, I_{g(REF)} = 1.0mA ) (Figure 12)</td>
<td>-</td>
<td>120</td>
<td>145</td>
<td>nC</td>
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<tr>
<td>Threshold Gate Charge</td>
<td>( Q_{g(TH)} )</td>
<td>( V_{GS} = 0V ) to 2V ( V_{DD} = 24V, I_D = 70A, R_L = 0.343\Omega, I_{g(REF)} = 1.0mA ) (Figure 12)</td>
<td>-</td>
<td>6.5</td>
<td>8.0</td>
<td>nC</td>
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<tr>
<td>Input Capacitance</td>
<td>( C_{ISS} )</td>
<td>( V_{DS} = 25V, V_{GS} = 0V, f = 1MHz ) (Figure 11)</td>
<td>-</td>
<td>3300</td>
<td>-</td>
<td>pF</td>
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<tr>
<td>Output Capacitance</td>
<td>( C_{OSS} )</td>
<td>-</td>
<td>1750</td>
<td>-</td>
<td>-</td>
<td>pF</td>
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<tr>
<td>Reverse Transfer Capacitance</td>
<td>( C_{RSS} )</td>
<td>-</td>
<td>750</td>
<td>-</td>
<td>-</td>
<td>pF</td>
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<tr>
<td>Thermal Resistance Junction to Case</td>
<td>( R_{JUC} ) (Figure 3)</td>
<td>-</td>
<td>1.0</td>
<td>-</td>
<td>-</td>
<td>(^{\circ}C/W)</td>
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<tr>
<td>Thermal Resistance Junction to Ambient</td>
<td>( R_{JUA} ) TO-220, TO-263</td>
<td>-</td>
<td>62</td>
<td>-</td>
<td>-</td>
<td>(^{\circ}C/W)</td>
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Source to Drain Diode Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
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<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source to Drain Diode Voltage</td>
<td>( V_{SD} )</td>
<td>( I_{SD} = 70A )</td>
<td>-</td>
<td>-</td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td>Reverse Recovery Time</td>
<td>( t_{rr} )</td>
<td>( I_{SD} = 70A, di_{SD}/dt = 100A/\mu s )</td>
<td>-</td>
<td>-</td>
<td>125</td>
<td>ns</td>
</tr>
</tbody>
</table>
**Typical Performance Curves**

**FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE**

**FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE**

**FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE**

**FIGURE 4. FORWARD BIAS SAFE OPERATING AREA**

**FIGURE 5. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY**

- **NOTE:** Refer to Intersil Application Notes AN9321 and AN9322.
Typical Performance Curves (Continued)

FIGURE 6. SATURATION CHARACTERISTICS

FIGURE 7. TRANSFER CHARACTERISTICS

FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

FIGURE 9. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE
**Typical Performance Curves** (Continued)

![Typical Performance Curves Graph](image)

**NOTE:** Refer to Intersil Application Notes AN7254 and AN7260.

**FIGURE 12. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT**

---

**Test Circuits and Waveforms**

![Test Circuits and Waveforms Diagram](image)

**FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT**

**FIGURE 14. UNCLAMPED ENERGY WAVEFORMS**

**FIGURE 15. SWITCHING TIME TEST CIRCUIT**

**FIGURE 16. SWITCHING WAVEFORMS**

---

**FIGURE 12. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT**
Test Circuits and Waveforms (Continued)

**FIGURE 17. GATE CHARGE TEST CIRCUIT**

**FIGURE 18. GATE CHARGE WAVEFORM**
PSPICE Electrical Model

.SUBCKT RFP70N03 2 1 3 ;
* NOM TEMP = 25°C

CA 12 8 6.09e-9
CB 15 14 6.05e-9
CIN 6 8 3.40e-9

DBODY 7 5 DBDMOD
DBBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 35.4
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 3.10e-9
LSOURCE 3 7 1.82e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RDKMOD 1
RDRAIN 5 16 RDSMOD 30.7e-6
RGATE 9 20 0.890
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 3.92e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBA 7 8 19 DC 1
VTO 21 6 0.605

.MODEL DBDMOD D (IS=7.91e-12 RS=3.87e-3 TRS1=2.71e-3 TRS2=2.50e-7 CJO=4.84e-9 TT=4.51e-8)
.MODEL DBKMOD D (RS=3.9e-2 TRS1=1.05e-4 TRS2=3.11e-5)
.MODEL DPLCAPMOD D (CJO=4.8e-9 IS=1e-30 N=10)
.MODEL MOSMOD NMOS (VTO=3.46 KP=47 IS=1e-30 N=10)
.MODEL MOSMOD PMOS (VTO=3.46 KP=47 IS=1e-30 N=10)
.MODEL RVTOMOD RES (TC1=-3.29e-3 TC2=3.49e-7)
.MODEL RDSMOD RES (TC1=2.23e-3 TC2=6.56e-6)

.ENDS

NOTE: For further discussion of the PSPICE model consult A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options; written by William J. Hepp and C. Frank Wheatley.
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Intersil (Taiwan) Ltd.
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Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029
70A, 30V, 0.010 Ohm, N-Channel Power MOSFETs

These N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA49025.

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- 70A, 30V
- $r_{DS(ON)} = 0.010\, \Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve (Single Pulse)
- 175°C Operating Temperature
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

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<td>TO-263AB</td>
<td>F1S70N03</td>
</tr>
</tbody>
</table>

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in tape and reel, e.g., RF1S70N03SM9A

Symbol

Packaging
Absolute Maximum Ratings  \( T_C = 25^\circ\text{C}, \text{Unless Otherwise Specified} \)

<table>
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<tr>
<th>Parameter</th>
<th>Symbol</th>
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<th>Typ</th>
<th>Max</th>
<th>Units</th>
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<tr>
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<td>( V_{DSS} )</td>
<td>( I_D = 250\mu\text{A}, V_{GS} = 0\text{V} ) (Figure 10)</td>
<td>30</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Drain to Gate Voltage ((R_{GS} = 20k\Omega)) (Note 1)</td>
<td>( V_{DGR} )</td>
<td>( I_{DM} )</td>
<td>200</td>
<td>-</td>
<td>-</td>
<td>A</td>
</tr>
<tr>
<td>Gate to Source Voltage</td>
<td>( V_{GS} )</td>
<td>( \pm 20\text{V} )</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Drain Current</td>
<td>( I_D )</td>
<td>( I_D )</td>
<td>70</td>
<td>-</td>
<td>-</td>
<td>A</td>
</tr>
<tr>
<td>Pulsed Drain Current</td>
<td>( I_{DM} )</td>
<td>( I_{DM} )</td>
<td>200</td>
<td>-</td>
<td>-</td>
<td>A</td>
</tr>
<tr>
<td>Pulsed Avalanche Rating</td>
<td>( E_{AS} )</td>
<td>Figures 5, 13, 14</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>W</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>( P_D )</td>
<td>( 150\text{W} )</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>W</td>
</tr>
<tr>
<td>Derate Above 25°C</td>
<td>( \theta_{JC} )</td>
<td>( 1.0\text{W/}^\circ\text{C} )</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>W/\text{C}</td>
</tr>
<tr>
<td>Operating and Storage Temperature</td>
<td>( T_J, T_{STG} )</td>
<td>( -55 \text{ to } 175^\circ\text{C} )</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>\text{C}</td>
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</tbody>
</table>

Maximum Temperature for Soldering

- Leads at 0.063in (1.6mm) from case for 10s: \( T_L \) 300 \( ^\circ\text{C} \)
- Package Body for 10s, see Techbrief 334: \( T_{pkg} \) 260 \( ^\circ\text{C} \)

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
1. \( T_J = 25^\circ\text{C} \) to 150°C.

Electrical Specifications  \( T_C = 25^\circ\text{C}, \text{Unless Otherwise Specified} \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
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<th>Typ</th>
<th>Max</th>
<th>Units</th>
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<td>( I_D = 250\mu\text{A}, V_{GS} = 0\text{V} ) (Figure 10)</td>
<td>30</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Gate to Source Threshold Voltage</td>
<td>( V_{GS(TH)} )</td>
<td>( V_{GS} = V_{DS}, I_D = 250\mu\text{A} ) (Figure 9)</td>
<td>2</td>
<td>-</td>
<td>4</td>
<td>V</td>
</tr>
<tr>
<td>Zero Gate Voltage Drain Current</td>
<td>( I_{DSS} )</td>
<td>( V_{DS} = 30\text{V}, V_{GS} = 0\text{V} )</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>\mu\text{A}</td>
</tr>
<tr>
<td>Gate to Source Leakage Current</td>
<td>( I_{GSS} )</td>
<td>( V_{GS} = \pm 20\text{V} )</td>
<td>-</td>
<td>-</td>
<td>50</td>
<td>\mu\text{A}</td>
</tr>
<tr>
<td>Drain to Source On Resistance</td>
<td>( r_{DS(ON)} )</td>
<td>( I_D = 70\text{A}, V_{GS} = 10\text{V} ) (Figure 8)</td>
<td>-</td>
<td>-</td>
<td>0.010</td>
<td>\Omega</td>
</tr>
<tr>
<td>Turn-On Time</td>
<td>( t_{ON} )</td>
<td>( V_{DD} = 15\text{V}, I_{D} = 70\text{A}, R_L = 0.214\Omega )</td>
<td>-</td>
<td>-</td>
<td>80</td>
<td>ns</td>
</tr>
<tr>
<td>Turn-On Delay Time</td>
<td>( t_{d(ON)} )</td>
<td>( I_D = 70\text{A}, R_L = 0.214\Omega )</td>
<td>-</td>
<td>-</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>Rise Time</td>
<td>( t_{r} )</td>
<td>-</td>
<td>20</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Turn-Off Delay Time</td>
<td>( t_{d(OFF)} )</td>
<td>-</td>
<td>-</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Fall Time</td>
<td>( t_{f} )</td>
<td>-</td>
<td>-</td>
<td>25</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Turn-Off Time</td>
<td>( t_{OFF} )</td>
<td>-</td>
<td>-</td>
<td>10</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Total Gate Charge</td>
<td>( Q_{g(TOT)} )</td>
<td>( V_{GS} = 0\text{V to 20V} )</td>
<td>-</td>
<td>215</td>
<td>260</td>
<td>nC</td>
</tr>
<tr>
<td>Gate Charge at 10V</td>
<td>( Q_{g(10)} )</td>
<td>( V_{DD} = 24\text{V}, I_{D} = 70\text{A}, R_L = 0.343\Omega )</td>
<td>-</td>
<td>120</td>
<td>145</td>
<td>nC</td>
</tr>
<tr>
<td>Threshold Gate Charge</td>
<td>( Q_{g(TH)} )</td>
<td>( V_{GS} = 0\text{V to 2V} )</td>
<td>-</td>
<td>6.5</td>
<td>8.0</td>
<td>nC</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>( C_{ISS} )</td>
<td>( V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz} ) (Figure 11)</td>
<td>-</td>
<td>3300</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>Output Capacitance</td>
<td>( C_{OSS} )</td>
<td>-</td>
<td>1750</td>
<td>-</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Reverse Transfer Capacitance</td>
<td>( C_{RSS} )</td>
<td>-</td>
<td>750</td>
<td>-</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance Junction to Case</td>
<td>( R_{JUC} )</td>
<td>(Figure 3)</td>
<td>-</td>
<td>1.0</td>
<td>-</td>
<td>\text{C/W}</td>
</tr>
<tr>
<td>Thermal Resistance Junction to Ambient</td>
<td>( R_{JUA} )</td>
<td>TO-220, TO-263</td>
<td>-</td>
<td>-</td>
<td>62</td>
<td>\text{C/W}</td>
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Source to Drain Diode Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source to Drain Diode Voltage</td>
<td>( V_{SD} )</td>
<td>( I_{SD} = 70\text{A} )</td>
<td>-</td>
<td>-</td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td>Reverse Recovery Time</td>
<td>( t_{rr} )</td>
<td>( I_{SD} = 70\text{A}, dl_{SD}/dt = 100\text{A/\mu s} )</td>
<td>-</td>
<td>-</td>
<td>125</td>
<td>ns</td>
</tr>
</tbody>
</table>
Typical Performance Curves

**FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE**

**FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE**

**FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE**

**FIGURE 4. FORWARD BIAS SAFE OPERATING AREA**

**FIGURE 5. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY**

**NOTES:** Refer to Intersil Application Notes AN9321 and AN9322.
Typical Performance Curves (Continued)

**Figure 6. Saturation Characteristics**

- $V_{GS} = 10V$
- $V_{GS} = 8V$
- $V_{GS} = 7V$
- $V_{GS} = 6V$
- $V_{GS} = 5V$
- $V_{GS} = 4V$

$V_{DS}$, Drain to Source Voltage (V)

**Figure 7. Transfer Characteristics**

- $V_{GS} = V_{DS}, I_D = 250\mu A$

Pulse Duration = 80\mu s
Duty Cycle = 0.5% MAX
$V_{DD} = 15V$

$T_J$, Junction Temperature (°C)

**Figure 8. Normalized Drain to Source on Resistance vs Junction Temperature**

- $V_{GS} = 10V, I_D = 70A$

**Figure 9. Normalized Gate Threshold Voltage vs Junction Temperature**

- $V_{GS} = 0V, f = 1MHz$
- $C_{ISS} = C_{GS} + C_{GD}$
- $C_{RSS} = C_{GD}$
- $C_{OSS} = C_{DS} + C_{GD}$

**Figure 10. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**

- $I_D = 250\mu A$

**Figure 11. Capacitance vs Drain to Source Voltage**

- $C_{ISS}$
- $C_{OSS}$
- $C_{RSS}$

$V_{DS}$, Drain to Source Voltage (V)
Typical Performance Curves (Continued)

![Graph showing typical performance curves for different drain-source voltages.](image)

NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 12. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

![Figure 13. Unclamped energy test circuit](image)

VARY \( \tau_p \) TO OBTAIN REQUIRED PEAK \( I_{\text{AS}} \)

![Figure 14. Unclamped energy waveforms](image)

![Figure 15. Switching time test circuit](image)

![Figure 16. Switching waveforms](image)
Test Circuits and Waveforms (Continued)

FIGURE 17. GATE CHARGE TEST CIRCUIT

FIGURE 18. GATE CHARGE WAVEFORM
PSPICE Electrical Model

.SUBCKT RFP70N03 2 1 3 ;
"NOM TEMP = 25°C"

CA 12 8 6.09e-9
CB 15 14 6.05e-9
CIN 6 8 3.40e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 35.4
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 3.10e-9
LSOURCE 3 7 1.82e-9

MOS1 16 6 8 MOSMOD M=0.99
MOS2 16 21 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDSMOD 5 16 30.7e-6
RGATE 9 20 0.890
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 3.92e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBA T 8 19 DC 1
VTO 21 6 0.665

.MODEL DBDMOD D (IS=7.91e-12 RS=3.87e-3 TRS1=2.71e-3 TRS2=2.50e-7 CJO=4.84e-9 TT=4.51e-8)
.MODEL DBKMOD D (RS=3.9e-2 TRS1=1.05e-4 TRS2=3.11e-5)
.MODEL DPLCAPMOD D (CJO=4.8e-9 IS=1e-30 N=10)
.MODEL MOSMOD NMOS (VTO=3.46 KP=47 IS=1e-30 N=10)
.MODEL RDSMOD RES (TC1=2.23e-3 TC2=6.56e-6)
.MODEL RVTOMOD RES (TC1=-3.29e-3 TC2=3.49e-7)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-8.35 VOFF=-6.35)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-6.35 VOFF=-8.35)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.0 VOFF=3.0)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=3.0 VOFF=2.0)

.ENDS

NOTE: For further discussion of the PSPICE model consult A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options; written by William J. Hepp and C. Frank Wheatley.
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<th>ASIA</th>
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<td>7F-6, No. 101 Fu Hsing North Road</td>
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<td>TEL: (886) 2 2716 9310 FAX: (886) 2 2715 3029</td>
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