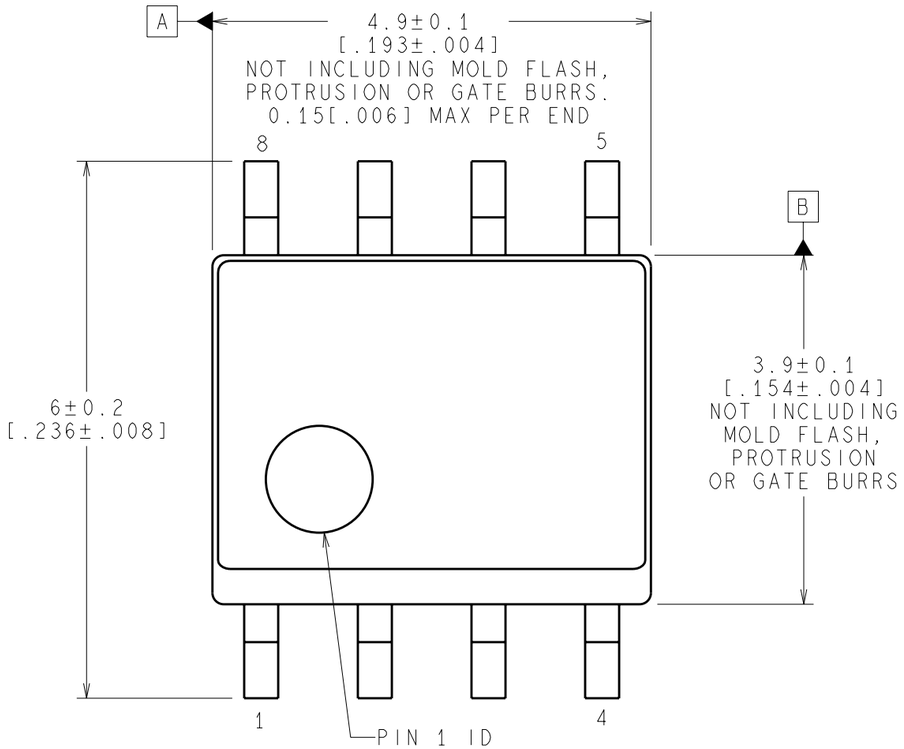
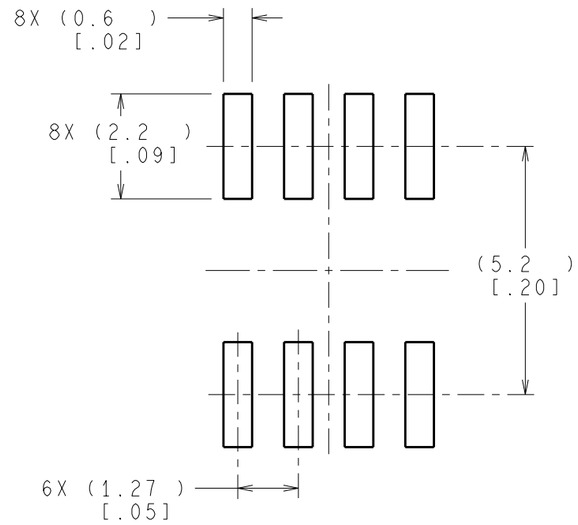
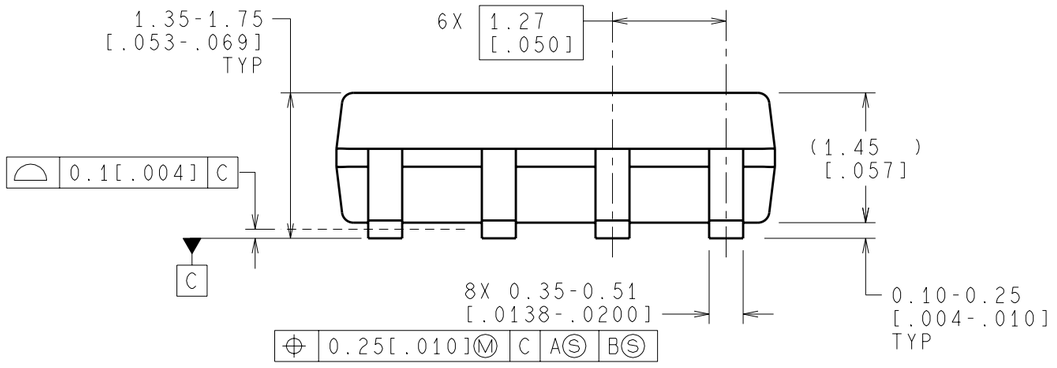
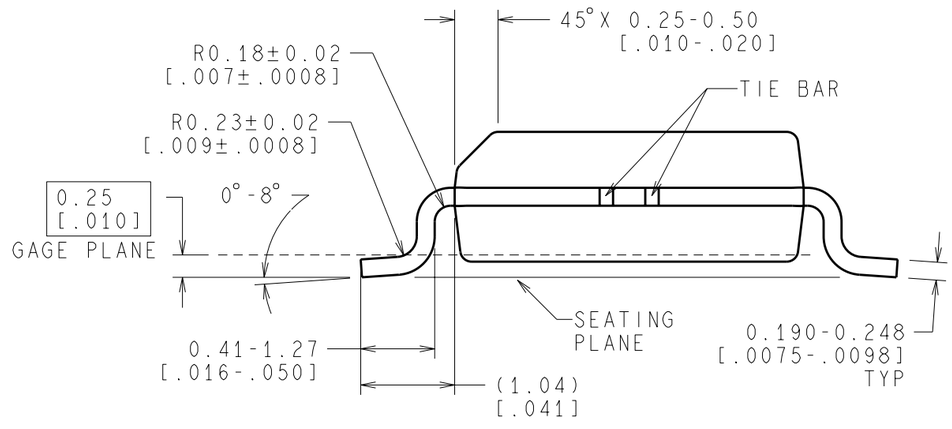




RECOMMENDED LAND PATTERN





NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR LEAD FINISH THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR) WEB PAGE (www.national.com).
2. REFERENCE JEDEC REGISTRATION MS-012, VARIATION AA.

CONTROLLING DIMENSION IS MILLIMETER
VALUES IN [ ] ARE INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

REVISIONS

REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
J	CHGE LD SHAPE FROM TAPER TO SQUARE; REVISE PER CURRENT STD; REDRAW)	11246	01/19/1996	MS/CS
K	DIM 1.35-1.75[.053-.069] WAS .069 [1.75] MAX; DIM 45°x 0.25-.050[.010-.020] WAS 45°X .017; REVISE DWG PER JEDEC STD; CONVERT CONTROLLING DIM TO MILLIMETER; DELETE DET A & TRANSFER ITS DIM'S TO SIDE VIEW; ADD RECOMMENDED LAND PATTERN DETAIL; REVISE NOTES; REVISE DWG TITLE; CHANGE DWG FORMAT TO B SIZE.	1727	02/14/2005	AS-MS/ TL/SN
L	REVISE DWG TITLE.	2187	09/15/2006	MS/MS
M	ADD TIE BAR AT SIDE OF PACKAGE; ADD "PROTRUSION OR GATE BURRS" TO DIM. 4.9 & DIM. 3.9	2820	05/29/2009	TKY/EL

APPROVALS	DATE
DRAWN MARTA SUCHY	01/19/1996
DFTG. CHK. T LEQUANG & E LEE	05/29/2009
ENGR. CHK. TK YII	05/29/2009

PROJECTION MM (INCH)

National Semiconductor
2900 Semiconductor Dr., Santa Clara, CA 95052-8090

SOIC NARROW,
4.9x3.9x1.45mm,
8 LD, 1.27mm PITCH

SCALE	SIZE	DRAWING NUMBER	REV
NTS	B	(SC)MKT-M08A	M

FORMERLY: N/A

SHEET 1 of 1