AND8147/D

An Innovative Approach to Achieving Single Stage PFC and Step-Down Conversion for Distributive Systems

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APPLICATION NOTE

INTRODUCTION

In most modern PFC circuits, to lower the input current harmonics and improve the input power factor, designers have historically used a boost topology. The boost topology can operate in the Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM), or Critical Conduction Mode.

Most PFC applications using the boost topology are designed to operate over the universal input AC voltage range (85−265 Vac), at 50 or 60 Hz, and provide a regulated DC bus (typically 400 Vdc). In most applications, the load can not operate from the high voltage DC bus, so a DC−DC converter is used to provide isolation between the AC source and load, and provide a low voltage output. The advantages to this system configuration are low Total Harmonic Distortion (THD), a power factor close to unity, excellent voltage regulation, and fast transient response on the isolated DC output. The major disadvantage of the boost topology is that two power stages are required which lowers the systems efficiency, increases component count, cost, and increases the size of the power supply.

ON Semiconductor's NCP1651 (www.onsemi.com) offers a unique alternative for Power Factor Correction designs, where the NCP1651 has been designed to control a PFC circuit operating in a flyback topology. There are several major advantages to using the flyback topology. First, the user can create a low voltage isolated secondary output, with a single power stage, and still achieve a low input current distortion, and a power factor close to unity. A second advantage, compared to the boost topology with a DC−DC converter, is a lower component count which reduces the size and the cost of the power supply.

Traditionally, the flyback approach has been ignored for PFC applications because of the perceived limitations such as high peak currents and high switch voltage ratings. This paper will demonstrate the novel control approach incorporated in the NCP1651 design, coupled with advances in discrete semiconductor technology that have made the flyback approach very feasible for a range of applications.

Controller Analysis

The NCP1651 can operate in either the Continuous or Discontinuous mode of operation. The following analysis will help to highlight the advantages of Continuous versus Discontinuous mode of operation.

The table below defines a set of conditions from which the comparison will be made between the two modes of operation.

Table 1.

Po = 90 W
Vin = 85−265 Vrms (analyzed at 85 Vrms input)
Efficiency = 80%
Pin = 108 W
Vo = 48 Vdc
Freq = 100 kHz
Transformer turns ratio n = 4

Continuous Mode (CCM)

To force the inductor current to be continuous over the majority of the input voltage range (85−265 Vac) the primary inductance, Lp needs to be at least 1.0 mH. Figure 1 shows the typical current through the primary winding of the flyback transformer. During the switch on period, this current flows in the primary and during the switch off−time, it flows in the secondary.

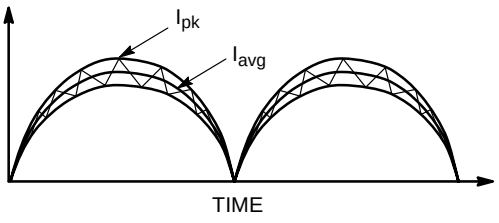

Figure 1.

Therefore, the peak current can be calculated as follows:

$$I_{pk} = I_{avg} + \frac{(1.414 \cdot V_{in} \sin \theta \cdot t_{on} \cdot 2)}{L_p} \quad \text{(eq. 1)}$$

where:

$$I_{avg} = \frac{1.414 \cdot P_{in}}{V_{in} \sin \theta} \quad \text{(eq. 2)}$$

$$T_{on} = T/(((\frac{N_S}{N_P}) \cdot (\frac{1.414 \cdot V_{in} \sin \theta}{V_O})) + 1) \quad \text{(eq. 3)}$$

For the selected operating condition:

$$T_{on} = 6.15\ \mu s \quad \text{(eq. 4)}$$

$$I_{pk} = \frac{1.414 \cdot 113}{85 \sin \theta} + \frac{1.414 \cdot 85 \cdot 6.15 \cdot 2}{1} = 3.35\ A \quad \text{(eq. 5)}$$

The analysis of the converter shows that the peak current operating in the CCM is 3.35 A.

Discontinuous Mode (DCM)

In the discontinuous mode of operation, the inductor current falls to zero prior to the end of the switching period as shown in Figure 2.

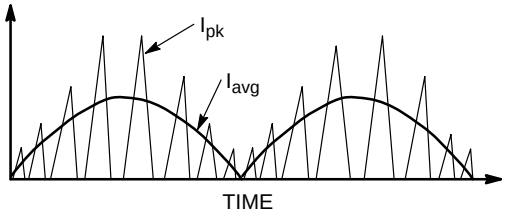

Figure 2.

To ensure DCM, Lp needs to be reduced to approximately 100 μH.

$$I_{pk} = \frac{V_{in} \sin \theta \cdot 1.414 \cdot t_{on}}{L_p} \quad \text{(eq. 6)}$$

$$I_{pk} = \frac{1.414 \cdot 85 \sin 90 \cdot 5.18}{100} = 6.23\ A$$

The results show that the peak current for a flyback converter operating in the Continuous Conduction Mode is about one half the peak current of a flyback converter operating in the Discontinuous Conduction Mode.

The lower peak current as a result of operating in the CCM lowers the conduction losses in the flyback MOSFET.

Current Harmonics Analysis

A second result of running in DCM can be higher input current distortion, Electromagnetic Interference (EMI), and a lower Power Factor, in comparison to CCM. While the higher peak current can be filtered to produce the same performance result, it will require a larger input filter.

A simple Fast Fourier Transform (FFT) was run in (ORCAD) Spice to provide a comparison between the harmonic current levels for CCM and DCM. The harmonic current levels will affect the size of the input EMI filter which in some applications are required to meet the levels of IEC1000−3−2. In the SPICE FFT model, no front end filtering was added so the result of the analysis could be compared directly.

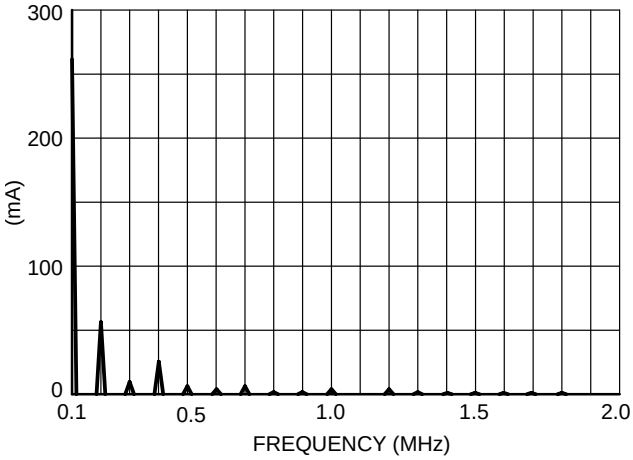

Figure 3. Continuous Conduction Mode FFT

Referring to Figure 3**,** at the 100 kHz switching frequency, the FFT is 260 mA, and the 2nd harmonic (200 kHz) is 55 mA.

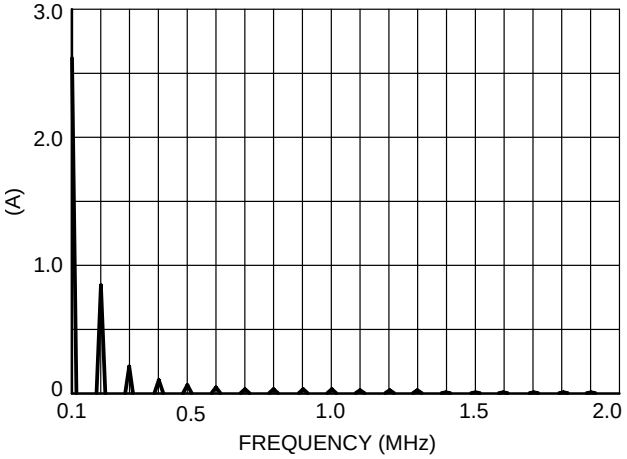

Figure 4. Discontinuous Conduction Mode FFT

Refer to Figure 4, at 100 kHz the FFT is 2.8 A, and the second harmonic (200 kHz) is 700 mA.

Results

From the result of our analysis it is apparent that a flyback PFC converter operating in CCM has half the peak current, and one tenth the fundamental (100 kHz) harmonic current compared to a flyback PFC converter operating in DCM. The results are lower conduction losses in the MOSFET and secondary rectifying diode, and a smaller input EMI filter. On the negative side to CCM operation, the flyback transformer will be larger because of the required higher primary inductance, and the leakage inductance will be higher affecting efficiency because of the leakage inductance energy that must be absorbed during the controller off time.

Some of the advantages to operating in DCM include lower switching losses because the current falls to zero prior to the next switching cycle, a smaller transformer, and in general the smaller transformer should result in a lower leakage inductance and less energy to be absorbed in the snubber.

Transformer Turn Ratio

The flyback transformer turns ratio affects several operating parameters, the secondary side peak current and the MOSFET drain to source voltage (VDS) during the controller off time, refer to Figure 8 for the application schematic.

The peak secondary current is:

Ipk prim • n

Where n is the transformer turns ratio, in our application n = 4.

Using the analysis for CCM versus DCM, the peak secondary current is:

CCM = 3.34 • 4 = 13.4 Apk

DCM = 6.23 • 4 = 24.9 Apk

It's clear from the analysis that the higher the turns ratio, there is a higher corresponding secondary side peak current resulting in higher conduction losses in the output rectifier.

A second effect of the turns ratio is the MOSFET VDS. The MOSFET VDS during the off time is:

$V_{pk} = V_{in}$ max • 1.414 + $(V_o + V_f)$ n + V_{spike}

where:

V_{in} max = 265 Vrms

V_o = the output voltage

V_f = the forward voltage drop across the output diode

V_{spike} = The voltage spike due to the transformer leakage inductance

The turns ratio in this equation determines the output voltage reflected back to the primary, $(V_o + V_f)n$.

A second effect of the turns ratio is the transformer leakage inductance, which effects Vspike. The leakage inductance is related to the coupling between the primary and the secondary of the transformer. As the turns ratio increase, there are more turns on the transformer, and unless the designer is careful in their core geometry selection and winding technique, the result will be a higher leakage inductance.

To minimize leakage inductance, a core with a wide winding window should be used; this will reduce the number of primary and secondary layers. In addition, interleaving the primary and secondary winding will increase the coupling. An example will help to illustrate the point. In our application the transformer required 74 primary turns (two layers) and 19 secondary turns (a single layer). The manufacturer of the transformer wound 45 primary turns, then the 19 turn secondary, and then the remaining 29 primary turns. The result was a measured leakage inductance of 9.0 μH.

A second transformer was wound with the entire 74 primary turns (two layers), then the 19 turn secondary, the measured leakage inductance increased to 37 μH. The reason for the increased leakage inductance was poor coupling between the primary and secondary.

Once the leakage inductance is reduced, verify that the voltage spike at turn off (Vspike) will not exceed your MOSFET VDS.

The MOSFET in our application has a VDS rating of 800 V, to provide a safety margin of at least 100 V VDS under worst case conditions:

Vspike:

$V_{spike} = VDS - V_{margin} - V_{in}$ max • 1.414 − $(V_o + V_f)$

800 − 100 − 265 • 1.414 − (48 + 0.7) 4 = 130 V

In our application the snubber circuit was designed to limit the VDS of the MOSFET to 130 Vpk. Refer to Figure 5 for the VDS waveform. The energy stored in the transformer leakage inductance is:

E = _ le I_{pk}_

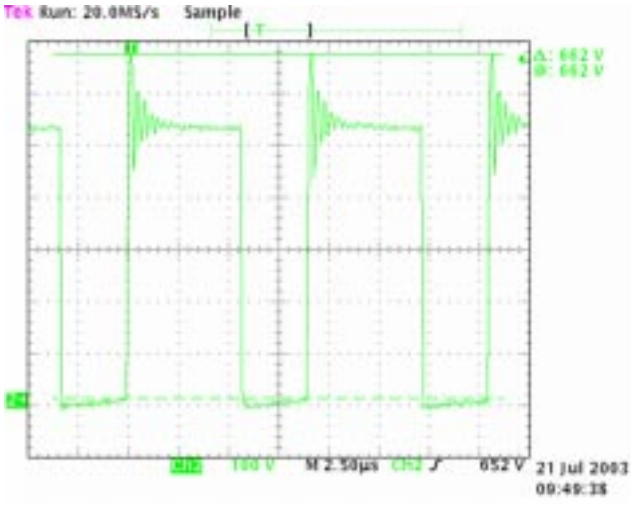

Figure 5.

The above analysis and examples illustrate the effects of the transformer turns ratio on the secondary side peak currents in the PFC and the MOSFET VDS at turn off. Careful attention should be taken when trading off turns ratio, primary inductance and duty cycle.

Output Voltage Ripple

A second consideration when using a flyback topology for PFC is that the output voltage ripple contains (on the secondary of the transformer) two components, the traditional high frequency ripple associated with a flyback converter, and the rectified line frequency ripple (100 or 120 Hz).

The high frequency ripple can be calculated by:

$$\Delta V = \sqrt{\Delta V_{cap}^2 + V_{esr}^2} \quad \text{(eq. 7)}$$

$$\Delta V_{cap} = \frac{Io_{avg} \cdot d_t}{C_o} \qquad Io_{avg} = \frac{I_p + I_{ped}}{2} \quad \text{(eq. 8)}$$

$$\Delta V_{esr} = I_{pk} \cdot esr \qquad \Delta V_{esr} = 13.38 \cdot 0.015 = 0.20\ V \quad \text{(eq. 9)}$$

where:

n = transformer turns ratio

I_{pk} = peak current (secondary) (13.38 Apk)

I_{ped} = pedestal of the secondary current (10.5 Apk)

C_o = output capacitance (3000 μ total)

esr = output capacitor equivalent series resistance (0.015_)

$d_t = T_{off}$ (3.92 μ)

$$\Delta V = \frac{\frac{13.38 + 10.5}{2}}{3000} \cdot 3.92 \qquad \text{(eq. 10)}$$

$$\_V = 0.0156\ V$$

Solving eq. 7 the high frequency ripple component on the output is:

$$\Delta V = \sqrt{0.0156^2 + 0.20^2} = 0.20\ V \quad \text{(eq. 11)}$$

The low frequency portion of the ripple:

$$\Delta V = \frac{I_{pk} \cdot d_t}{C_o} \qquad I_{avg} = \frac{P_o}{V_o} \qquad I_{pk} = \frac{I_{avg}}{0.637} \quad \text{(eq. 12)}$$

$$I_{pk} = \frac{90}{48 \cdot 0.637} = 2.95\ A$$

If the output voltage ripple is divided into 10° increments over one cycle (180°) the sinusoidal ripple voltage with respect to phase angle is:

$$\Delta V = \frac{P_o}{\frac{0.637 \cdot V_o \sin\ \theta}{C_o \cdot 18 \cdot fline}} \quad \text{(eq. 13)}$$

To calculate the total output voltage ripple:

Vripple total = eq. 7 + eq. 13.

$$\Delta V_{ripple\ total} = \sqrt{\Delta V_{cap}^2 + \Delta V_{esr}^2} + \frac{P_o}{\frac{0.637 \cdot V_o \sin\ \theta}{C_o \cdot 18 \cdot fline}} \quad \text{(eq. 14)}$$

In Figure 6, the output voltage ripple as a function of phase angle is plotted. The results show that as long as a capacitor(s) with low esr are used, that the output voltage ripple will be dominated by the low frequency ripple (100 Hz or 120 Hz).

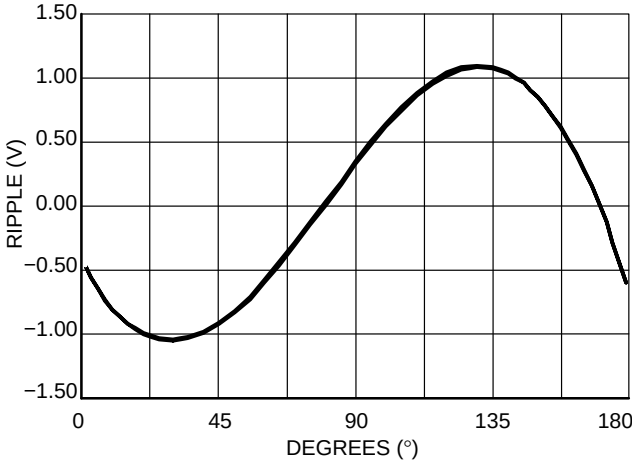

Figure 6. Output Ripple Envelope

Hold−Up Time

If the secondary output voltage is used for a distributed bus, the designer may elect to size the output capacitor for hold−up times, versus ripple. If so the output capacitors can be calculated by:

$$C_o = \frac{2 \cdot P_o \cdot th}{V_{nom}^2 + V_{min}^2} \quad \text{(eq. 15)}$$

where:

P_{out} = the maximum output power

th = the required hold−up time (we selected one cycle of the line 60 Hz, 16.67 ms)

V_{nom} = the nominal 48 Vdc output

V_{min} = 36 Vdc

$$C_o = \frac{2 \cdot 90 \cdot 16.67}{48^2 - 36^2} = 3000\ \mu F \quad \text{(eq. 16)}$$

In the above calculations for output voltage ripple and hold−up time, it is a coincidence that the same value of output capacitance was selected in both cases.

NCP1651 Features

The NCP1651 internally provides all of the necessary features that are typically seen in a PFC controller, plus some features not normally found. For example the NCP1651 has a high voltage start−up circuit, which allows the designer to connect pin 16 of the NCP1651 directly to the high voltage DC bus, eliminating bulky and expensive start−up circuitry.

After power is applied to the circuit, a high voltage FET is biased as a current source to provide current for start−up power. The high voltage start−up circuit is enabled and current is drawn from the rectified AC line to charge the V_{CC} cap. When the voltage on the V_{CC} cap reaches the turn on point for the UVLO circuit (10.8 V nominally), the start−up circuit is disabled, and the PWM circuit is enabled. With the NCP1651 enabled the bias current increases from its

standby level to the operational level. A divide−by−eight counter is preset to the count of 7, so that on start−up the chip will not be operational on the first cycle. The second V_{CC} cycle the counter is advanced to 8, and the chip will be allowed to start at this time. Refer to Figure 7.

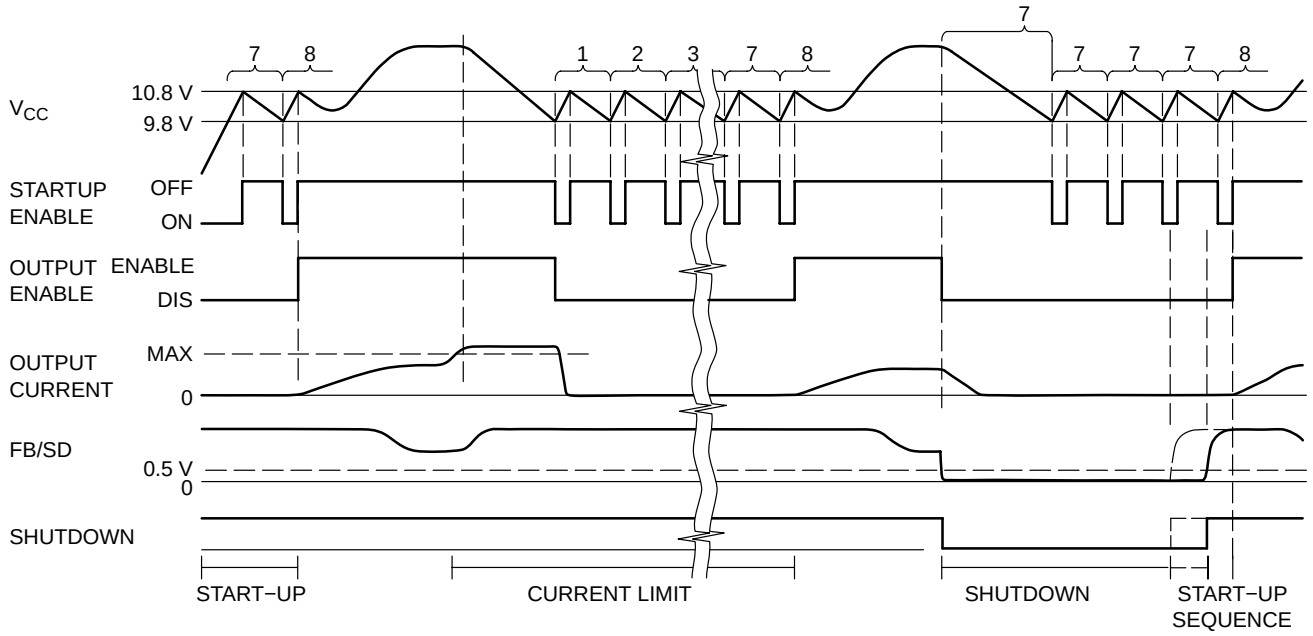

Figure 7.

In addition to providing the initial charge on the V_{CC} capacitor, the start circuit also serves as a timer for the start−up, overcurrent, and shutdown modes of operation. Due to the nature of this circuit, this chip must be biased using the start−up circuit and an auxiliary winding on the power transformer. Attempting to operate this chip off of a fixed voltage supply will not allow the chip to start.

In the shutdown mode, the V_{CC} cycle is held in the 7 count state until the shutdown signal is removed. This allows for a repeatable, fast restart. See Figure 6 for the timing diagram**.**

The unit will remain operational as long as the V_{CC} voltage remains above the UVLO under voltage trip point. If the V_{CC} voltage is reduced to the under voltage trip point, operation of the unit will be disabled, the start−up circuit will again be enabled, and will charge the V_{CC} capacitor up to the turn on voltage level. At this point the start−up circuit will turn off and the unit will remain in the shutdown mode. This will continue for the next seven cycles. On the eighth cycle, the NPC1651 will again become operational. If the V_{CC} voltage remains above the undervoltage trip point the unit will continue to operate, if not the unit will begin another divide−by−eight cycle.

The purpose of the divide−by−eight counter is to reduce the power dissipation of the chip under overload conditions and allow it to recycle indefinitely without overheating the chip.

It is critical that the output voltage reaches a level that allows the auxiliary voltage to remain above the UVLO turn−off level before the V_{CC} cap has discharged to 9.8 V level. If the bias voltage generated by the inductor winding fails to exceed the shutdown voltage before the capacitor reduces to the UVLO under voltage turn−off level, the unit will shut down and go into a divide−by−eight cycle, and will never start. If this occurs, the V_{CC} capacitor value should be increased.

CONCLUSION

It will ultimately be up to the designer to perform a trade−off study to determine which topology, Boost versus flyback, Continuous versus Discontinuous Mode of operation will meet all the system performance requirements. But the recent introduction of the NCP1651 allows the system designer an additional option yielding a less expensive, smaller solution.

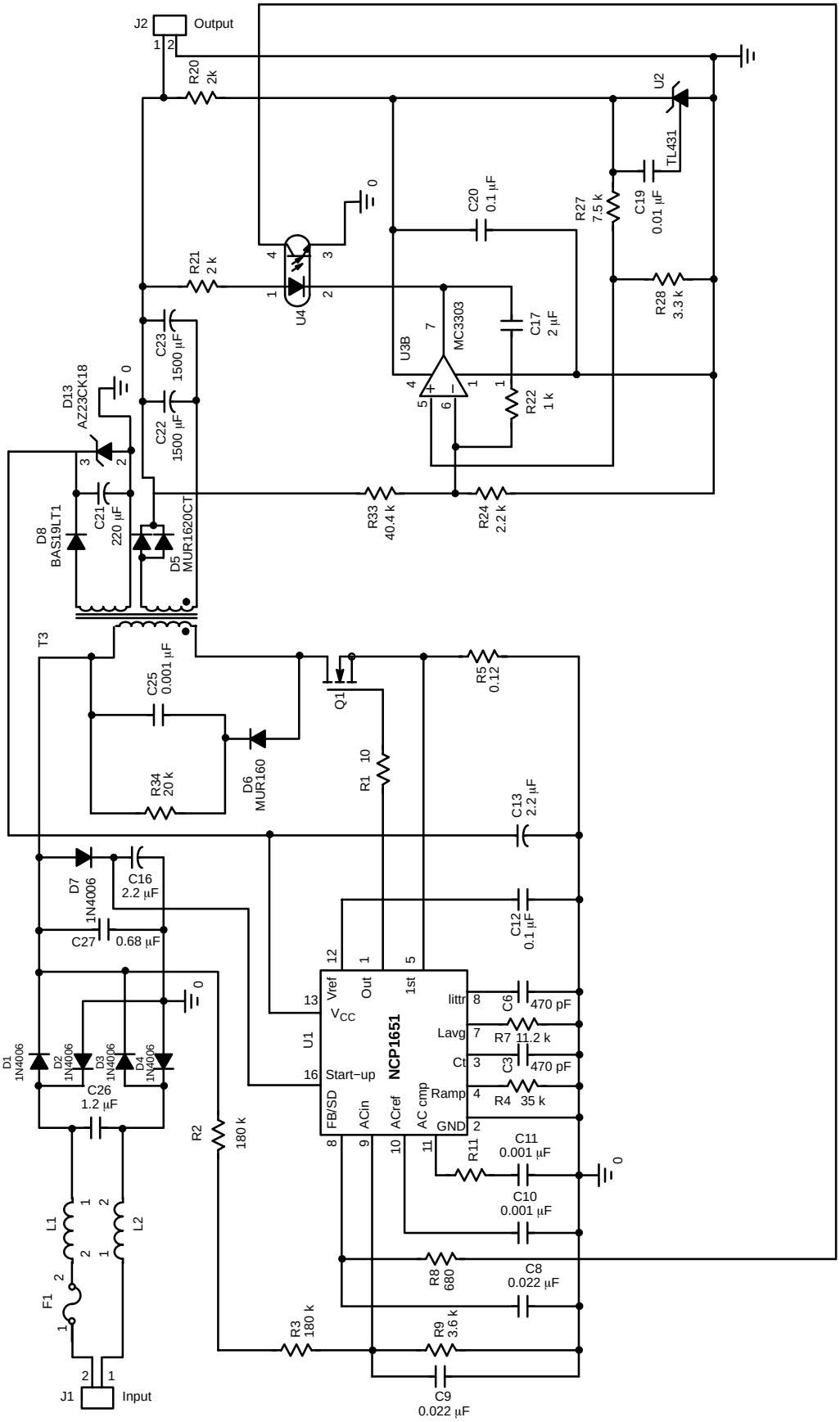

Figure 8. CCM Application Schematic

Notes

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