8-/4-Channel ADCs with Simultaneous T/Hs and Reference

**General Description**

The MAX155/MAX156 are high-speed, 8-bit, multi-channel analog-to-digital converters (ADCs) with simultaneous track/hold (T/Hs) to eliminate timing differences between input channel samples. The MAX155 has 8 analog input channels, and the MAX156 has 4 analog input channels. Each channel has its own T/H, and all T/Hs sample at the same instant. The ADC converts a channel in 3.6µs and stores the result in an internal 8x8 RAM. The MAX155/MAX156 also feature a 2.5V internal reference and power-down capability, providing a complete, sampling data-acquisition system.

When operating from a single +5V supply, the MAX155/MAX156 perform either unipolar or bipolar, single-ended or differential conversions. For applications requiring wider dynamic range or bipolar conversions around ground, the VSS supply pin may be connected to -5V.

Conversions are initiated with a pulse to the WR pin, and data is accessed from the ADC's RAM with a pulse to the RD pin. A bidirectional interface updates the channel configuration and provides output data. The ADC may also be wired for output-only operation. The MAX155 comes in 28-pin DIP and wide SO packages, and the MAX156 comes in 24-pin narrow plastic DIP and 28-pin wide SO packages.

**Applications**

- Phase-Sensitive Data Acquisition
- Vibration and Waveform Analysis
- DSP Analog Input
- AC Power Meters
- Portable Data Loggers

**Features**

- 8 Simultaneously Sampling Track/Hold Inputs
- 3.6µs Conversion Time per Channel
- Unipolar or Bipolar Input Range
- Single-Ended or Differential Inputs
- Mixed Input Configurations Possible
- +2.5V Internal Reference
- Single +5V or Dual ±5V Supply Operation

**Ordering Information**

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP. RANGE</th>
<th>PIN-PACKAGE</th>
<th>ERROR (LSBs)</th>
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<tbody>
<tr>
<td>MAX155ACP</td>
<td>0°C to +70°C</td>
<td>28 Plastic DIP</td>
<td>±1/2</td>
</tr>
<tr>
<td>MAX155BCP</td>
<td>0°C to +70°C</td>
<td>28 Plastic DIP</td>
<td>±1</td>
</tr>
<tr>
<td>MAX155ACW</td>
<td>0°C to +70°C</td>
<td>28 Wide SO</td>
<td>±1/2</td>
</tr>
<tr>
<td>MAX155BCW</td>
<td>0°C to +70°C</td>
<td>28 Wide SO</td>
<td>±1</td>
</tr>
<tr>
<td>MAX155BCD</td>
<td>0°C to +70°C</td>
<td>Dice*</td>
<td>±1</td>
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</table>

Ordering information continued on last page.

* Contact factory for dice specifications.

**Pin Configurations**

The MAX156 is on the last page.

Maxim Integrated Products 1
8-/4-Channel ADCs with Simultaneous T/Hs and Reference

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
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<tbody>
<tr>
<td>VDD to AGND</td>
<td>VDD to DGN</td>
<td>0.3V, +6V</td>
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<tr>
<td>AGND to DGN</td>
<td>0.3V, -6V</td>
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<tr>
<td>VSS to AGND</td>
<td>0.3V, VDD</td>
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<tr>
<td>CS, WR, RD, ClK, MODE to DGN</td>
<td>0.3V, VDD</td>
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<tr>
<td>BUSY, DON to DGN</td>
<td>0.3V, VDD</td>
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<tr>
<td>REFIN to AGND</td>
<td>0.3V, VDD</td>
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<tr>
<td>Ain to AGND</td>
<td>-0.3V, VDD</td>
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<td>Output Current (REFOUT)</td>
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Continuous Power Dissipation (Tamb = +70°C)
- 24-Pin Plastic DIP (derate 6.7mW/°C above +70°C): 696mW
- 24-Pin CERDIP (derate 12.5mW/°C above +70°C): 1000mW
- 28-Pin Plastic DIP (derate 9.09mW/°C above +70°C): 727mW
- 28-Pin Wide SO (derate 12.5mW/°C above +70°C): 1000mW
- 28-Pin CERDIP (derate 16.67mW/°C above +70°C): 1333mW

Operating Temperature Ranges:
- MAX155/MAX156_C,- = -40°C to +85°C
- MAX155/MAX156_E,- = 0°C to +70°C
- MAX155/MAX156_MU = -55°C to +125°C

Storage Temperature Range: -65°C to +160°C

Lead Temperature (soldering, 10 sec): +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VDD) = +5V, REFIN = ±2.5V, External Reference, AGND = DGN = 0V, VSS = 0V or -5V, ClK = 5MHz External, Unipolar Range.

Single Ended Mode; Tamb = TMIN to TMAX, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
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<td>Integral Linearity Error</td>
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<td>MAX15_A</td>
<td>±1/2</td>
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<td>LSB</td>
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<tr>
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<td></td>
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<td>MAX15_B</td>
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<tr>
<td>No Missing Codes Resolution</td>
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<td>Offset Error (Unipolar)</td>
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<td></td>
<td></td>
<td>MAX15_B</td>
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<td>Offset Error (Bipolar)</td>
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<td>LSB</td>
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<td>MAX15_B</td>
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<td>LSB</td>
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<td>Channel-to-Channel Matching</td>
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<td>LSB</td>
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<td></td>
<td></td>
<td>MAX15_B</td>
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DYNAMIC PERFORMANCE (VIN = 50kHz, 2.5 Vpp sine wave sampled at 220ksamples/sec)

<table>
<thead>
<tr>
<th>Parameter</th>
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<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
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<td>MAX15_B</td>
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<td>Total Harmonic Distortion</td>
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<td>4 ns</td>
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</table>

Note 1: The accuracy is specified at 0°C to +70°C.

Note 2: The aperture delay matching is specified at ±VDD ±0.3V to ±VDD ±0.3V.

Note 3: The signal-to-noise and distortion ratio is specified at 0.1% THD.
### ELECTRICAL CHARACTERISTICS (continued)

(VDD = +5V, REFIN = +2.5V, External Reference, AGND = DGND = 0V, VSS = 0V or -5V, fCLK = 5MHz External, Unipolar Range, Single-Ended Mode, TA = TMIN to TMAX, unless otherwise noted.)

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<tr>
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<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<tr>
<td>Unipolar, Single-Ended</td>
<td>AIN(+) to AGND</td>
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<td>VREF</td>
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<td>V</td>
</tr>
<tr>
<td>Bipolar, Single-Ended</td>
<td>AIN(+) to AIN(-)</td>
<td>0</td>
<td>VREF</td>
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<td></td>
<td>V</td>
</tr>
<tr>
<td>Bipolar, Differential</td>
<td>AIN(+) to AIN(-)</td>
<td>-VREF</td>
<td>VREF</td>
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<td>V</td>
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<td>Common-Mode Range</td>
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<td>μA</td>
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<td>REFIN Range (for specified performance) (Note 2)</td>
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<td>2.500</td>
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<td>V</td>
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<td>IREF</td>
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<td>2.5V</td>
<td>1</td>
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<td>V</td>
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<tr>
<td>Load Regulation</td>
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<td>Power-Supply Sensitivity</td>
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<td>V</td>
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<td>CS, RD, WR, CLK, DO-07 (when inputs)</td>
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<td>V</td>
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<tr>
<td>Input Low Voltage</td>
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<td>pF</td>
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<td>μA</td>
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<td>μA</td>
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<td>μA</td>
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<td>BUSY, DO-07 Output Low Voltage</td>
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<td>V</td>
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<td>Output High Voltage</td>
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<td>μA</td>
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<td>Floating State Leakage</td>
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<td>μs</td>
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### 8-/4-Channel ADCs with Simultaneous T/Hs and Reference

#### ELECTRICAL CHARACTERISTICS (continued)

(VDD = +5V, REFIN = +2.5V, External Reference, AGND = DGND = 0V, VSS = 0V or -5V, fCPU = 5MHz External, Unipolar Range, Single-Ended Mode, TA = TMIN to TMAX unless otherwise noted.)

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<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<td>V</td>
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<td>mA</td>
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<td>MAX155</td>
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<td>CLK, CS, WR</td>
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<td>RD = 0 or VDD,</td>
<td>DO, DOUT = 0V or VDD</td>
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<td>-5</td>
<td>V</td>
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<td>±0.1</td>
<td>LSB</td>
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#### TIMING CHARACTERISTICS (Note 3, Figures 1-7)

(VDD = +5V, REFIN = +2.5V, External Reference, AGND = DGND = 0V, VSS = 0V or -5V, TA = TMIN to TMAX unless otherwise noted.)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<td>ns</td>
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<tr>
<td>CS to RD Setup Time</td>
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<td>280</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MAX155M</td>
<td></td>
<td>300</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>WR to BUSY (Low Delay)</td>
<td>tWBD</td>
<td>MAX15, C/E</td>
<td>0</td>
<td>220</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MAX155M</td>
<td></td>
<td>240</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>BUSY High to WR Delay (to update configuration register) (Notes 2, 3)</td>
<td>tWPD</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>CLK to WR Delay (acquisition time) (Note 2)</td>
<td>tACD</td>
<td>800</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>BUSY High to RD Delay (Notes 2, 3)</td>
<td>tBPD</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>
TIMING CHARACTERISTICS (continued) (Note 3, Figures 1-7)

(Vcc = +5V, REFIN = +2.5V, External Reference, AGND = DGND = 0V, VSS = 0V or 5V, TA = Tmin to Tmax, unless otherwise noted.)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>RD to Data Valid (Note 4)</td>
<td>tDv</td>
<td>MAX15_C/E</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MAX155M</td>
<td>120</td>
<td></td>
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<td>ns</td>
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<tr>
<td>RD to Data Three-State Output (Note 5)</td>
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<td>MAX15_C/E</td>
<td>80</td>
<td></td>
<td></td>
<td>ns</td>
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<tr>
<td></td>
<td></td>
<td>MAX155M</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CLK to BUSY Delay (Note 2)</td>
<td>tCBS</td>
<td>MAX15_C/E</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MAX155M</td>
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<tr>
<td>CLK Frequency</td>
<td></td>
<td>MAX15_C/E</td>
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<td></td>
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</tr>
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<td>MAX155M</td>
<td>5.0</td>
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<td></td>
<td>MHz</td>
</tr>
</tbody>
</table>

Note 1: Vcc = +5V, REFIN = +2.5V, VSS = 0V. Performance at ±5% power-supply tolerance is guaranteed by Power-Supply Rejection test.
Note 2: Guaranteed by design, not production tested.
Note 3: All input control signals are specified with t = t = 20ns (10% to 90% of 14V) and timed from a +1.6V voltage level. Output signals are timed from Vcc and VSS.
Note 4: tpd is the time required for an output to cross +0.8V or -2.4V measured with load circuit of Figure 1.
Note 5: tcn is the time required for the data lines to change 0.5V, measured with load circuits of Figure 2.

Figure 1. Load Circuits for Data Access Timing
Figure 2. Load Circuits for Three-State Output Timing
Figure 3. Write and Read Timing
## 8-/4-Channel ADCs with Simultaneous T/Hs and Reference

### Pin Description

<table>
<thead>
<tr>
<th>MAX155</th>
<th>MAX156</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIP:SO</td>
<td>DIP:SO</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>23</td>
<td>26</td>
<td>AIN3</td>
</tr>
<tr>
<td>2</td>
<td>24</td>
<td>28</td>
<td>AIN2</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>2</td>
<td>AIN1</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>4</td>
<td>AIN0</td>
</tr>
<tr>
<td>5</td>
<td>3</td>
<td>5</td>
<td>MODE</td>
</tr>
<tr>
<td>6</td>
<td>4</td>
<td>6</td>
<td>VSS</td>
</tr>
<tr>
<td>7</td>
<td>5</td>
<td>7</td>
<td>CS</td>
</tr>
<tr>
<td>8</td>
<td>6</td>
<td>8</td>
<td>RD</td>
</tr>
<tr>
<td>9</td>
<td>7</td>
<td>9</td>
<td>WR</td>
</tr>
<tr>
<td>10</td>
<td>8</td>
<td>10</td>
<td>BUSY</td>
</tr>
<tr>
<td>11</td>
<td>9</td>
<td>11</td>
<td>CLK</td>
</tr>
<tr>
<td>12</td>
<td>10</td>
<td>12</td>
<td>D7/ALL</td>
</tr>
<tr>
<td>13</td>
<td>11</td>
<td>13</td>
<td>D6/DIFF</td>
</tr>
<tr>
<td>14</td>
<td>12</td>
<td>14</td>
<td>DGND</td>
</tr>
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<td>15</td>
<td>13</td>
<td>15</td>
<td>D5/BIP</td>
</tr>
<tr>
<td>16</td>
<td>14</td>
<td>16</td>
<td>D4/INH</td>
</tr>
<tr>
<td>17</td>
<td>15</td>
<td>17</td>
<td>D3/PD</td>
</tr>
<tr>
<td>18</td>
<td>16</td>
<td>18</td>
<td>D2/A2</td>
</tr>
<tr>
<td>19</td>
<td>17</td>
<td>19</td>
<td>D1/A1</td>
</tr>
<tr>
<td>20</td>
<td>18</td>
<td>20</td>
<td>D0/A0</td>
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<td>21</td>
<td>19</td>
<td>21</td>
<td>REFOUT</td>
</tr>
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<td>22</td>
<td>20</td>
<td>22</td>
<td>REF/N</td>
</tr>
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<td>23</td>
<td>21</td>
<td>23</td>
<td>AGND</td>
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<td>24</td>
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<td>24</td>
<td>VDD</td>
</tr>
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<td>25-28</td>
<td></td>
<td></td>
<td>AIN7-4</td>
</tr>
<tr>
<td></td>
<td>1, 3</td>
<td>25, 27</td>
<td>N.C.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **AIN3**: Sampling Analog input, channel 3
- **AIN2**: Sampling Analog input, channel 2
- **AIN1**: Sampling Analog input, channel 1
- **AIN0**: Sampling Analog input, channel 0
- **MODE**: Mode configures multiplexer and converter. See Table 4.
- **VSS**: Negative Supply. Power VSS with -5V for extended input range.
- **CS**: Chip Select. Input must be low for the ADC to recognize RD, or WR.
- **RD**: READ Input reads data sequentially from RAM.
- **WR**: WRITE Input's rising edge initiates conversion and updates channel configuration register. Falling edge samples inputs.
- **BUSY**: BUSY Output is low when conversion is in progress.
- **CLK**: External Clock Input.
- **D7/ALL**: Three-State Data Output Bit 7 (MSB) / Sequential or Specific Conversion
- **D6/DIFF**: Three-State Data Output Bit 6 / Single-Ended/Differential Select
- **DGND**: Digital Ground
- **D5/BIP**: Three-State Data Output Bit 5 / Unipolar/Bipolar Conversion
- **D4/INH**: Three-State Data Output Bit 4 / Inhibit Conversion Input
- **D3/PD**: Three-State Data Output Bit 3 / Power-Down Input
- **D2/A2**: Three-State Data Output Bit 2 / RAM Address Bit A2 (MAX155 only)
- **D1/A1**: Three-State Data Output Bit 1 / RAM Address Bit A1
- **D0/A0**: Three-State Data Output Bit 0 / RAM Address Bit A0
- **REFOUT**: Reference Output, +2.5V
- **REF/N**: Reference Input, +2.5V normally
- **AGND**: Analog Ground
- **VDD**: Power-Supply Voltage, +5V normally
- **AIN7-4**: Sampling Analog Input, channels 7-4
- **N.C.**: No Internal Connection - floating pin.
Detailed Description
A/D Converter Operation

The MAX155/MAX156 contain a 3.6µs successive approximation ADC and 8/4 track-and-hold (T/H) inputs. When a conversion is started, all AIN inputs are simultaneously sampled. All channels sample whether or not they are selected for the conversion. Either a single-channel or multi-channel conversion may be requested and channel configurations may be mixed. ADC results are then stored in an internal RAM.

In hard-wired mode (see Multiplexer and A/D Configurations section) multi-channel conversions are initiated with one write operation. In input/output (I/O) mode, multi-channel configurations are set up prior to the conversion by loading channel selections into the configuration register. This register also selects single-ended/differential, unipolar/bipolar (Figure 9), power-down and other functions. Each channel selection requires a separate write operation (i.e. 8 writes for 8 channels), but only after power-up. Once the desired channel arrangement is loaded, each subsequent write converts all selected channels without reconfiguring the multiplexer (mux). I/O mode requires more write operations, but provides more flexibility than hard-wired mode.

To access conversion results, successive RD pulses automatically sequence through RAM, beginning with channel 0. Each RD pulse increments the RAM address counter, which resets to 0 when WR goes low in multi-channel conversions. An arbitrary RAM location may also be read by writing a 1 to INH while loading the RAM address (A0-A2), and then performing a read operation.

### Table 1. Multiplexer Configurations

<table>
<thead>
<tr>
<th>PIN*</th>
<th>INPUT</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>D2/A2</td>
<td>1 or 0</td>
<td>AD-A2 select a multiplexer channel for the configurations described below, or select a RAM address for reading with a subsequent RD.</td>
</tr>
<tr>
<td>D1/A1</td>
<td>0</td>
<td>Normal ADC operation</td>
</tr>
<tr>
<td>D3/PD</td>
<td>1</td>
<td>Power-Down reduces the power-supply current. Configuration data may be loaded and is maintained during power-down.</td>
</tr>
<tr>
<td>D4/NH</td>
<td>0</td>
<td>A conversion starts when WR goes high.</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Inhibits the conversion when WR goes high. Allows mux configuration to be loaded and RAM locations to be accessed without starting a conversion.</td>
</tr>
<tr>
<td>D5/BIP**</td>
<td>0</td>
<td>Unipolar conversion (Figure 9a) for the channel specified by A0-A2. Input range = 0V to VREF.</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Bipolar conversion (Figure 9b) for the channel specified by A0-A2. Input range = ±VREF.</td>
</tr>
<tr>
<td>D6/DIFF**</td>
<td>0</td>
<td>Single-ended configuration for the channel specified by A0-A2 as described in Table 2.</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Differential configuration for the channel specified by A0-A2 as described in Table 2.</td>
</tr>
<tr>
<td>D7/ALL</td>
<td>0</td>
<td>All previously configured channels are converted. Data is read with consecutive RD pulses, beginning with the lowest configured channel.</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Only the channel specified by A2-A0 is converted. A single RD pulse reads the result of that conversion.</td>
</tr>
</tbody>
</table>

* Configuration inputs are shared with data outputs D0-D7. The functions of D0-D7 are not described in this table.
** DIFF and BIP are not implemented on the current conversion, but go into effect on the following conversion.
8-/4-Channel ADCs with Simultaneous T/Hs and Reference

Multiplexer and A/D Configuration

A conversion is started with a WR pulse. All channel's sample on WR's falling edge. Mux configuration data is loaded on WR's rising edge. In I/O mode (MODE = Open Circuit), selections for channel number, single- or multi-channel conversion, unipolar or bipolar input, and single-ended or differential input are made with A0-A2, ALL, BIP, and DIFF (Table 1). These input pins are also shared with the RAM data outputs D0-D7. An alternate, simpler interface is provided by the hard-wired mode, which selects some general mux configurations without requiring ADC programming. Hard-wired connections of MODE and VSS select from 4 mux configurations as listed in Table 4 (see Hard-Wired Mode section).

On the rising edge of WR, the mux configuration register is updated; falling edge initiates sampling of all inputs. A channel selection can be implemented on the current conversion but changes from unipolar to bipolar (with BIP) or from single-ended to differential operation (with DIFF) do not go into effect until the following WR. This can be overcome by writing to the configuration register while inhibiting the conversion (INH = 1), or by changing DIFF and BIP one conversion early, i.e., on the previous write.

Table 2. Single-Ended Channel Selection (MODE = Open Circuit)

<table>
<thead>
<tr>
<th>MUX ADDRESS</th>
<th>SINGLE-ENDED CHANNEL SELECTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0 A1 A2 DIFF</td>
<td>0 1 2 3 4 5 6 7 AGN(x)</td>
</tr>
<tr>
<td>0 0 0 0</td>
<td>+</td>
</tr>
<tr>
<td>1 0 0 0</td>
<td>+</td>
</tr>
<tr>
<td>0 1 0 0</td>
<td>+</td>
</tr>
<tr>
<td>1 1 0 0</td>
<td>+</td>
</tr>
<tr>
<td>0 0 1 0</td>
<td>+</td>
</tr>
<tr>
<td>0 1 1 0</td>
<td>+</td>
</tr>
<tr>
<td>1 1 1 0</td>
<td>+</td>
</tr>
</tbody>
</table>

Note: Shaded areas represent MAX156 operation

Table 3. Differential Channel Selection (MODE = Open Circuit)

<table>
<thead>
<tr>
<th>MUX ADDRESS</th>
<th>DIFFERENTIAL CHANNEL SELECTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0 A1 A2 DIFF</td>
<td>0 1 2 3 4 5 6 7</td>
</tr>
<tr>
<td>0 0 0 1</td>
<td>+</td>
</tr>
<tr>
<td>0 1 0 1</td>
<td>+</td>
</tr>
<tr>
<td>0 0 1 1</td>
<td>-</td>
</tr>
<tr>
<td>0 1 1 1</td>
<td>-</td>
</tr>
<tr>
<td>1 0 0 1</td>
<td>-</td>
</tr>
<tr>
<td>1 1 0 1</td>
<td>-</td>
</tr>
<tr>
<td>1 0 1 1</td>
<td>-</td>
</tr>
<tr>
<td>1 1 1 1</td>
<td>-</td>
</tr>
</tbody>
</table>

Note: Shaded areas represent MAX156 operation.
8-/4-Channel ADCs with Simultaneous T/Hs and Reference

**Interface Timing**

**Input/Output Mode, Multi-Channel Conversion Timing**

I/O mode is selected when the MODE input is open circuit. In I/O mode, the mux configuration register determines the conversion type. The register is updated on the rising edge of WR.

Table 1 lists all conversion options. For example, at D6/DIFF, a logic 0 or 1 selects a single-ended or differential conversion. Data is loaded into addressed locations in the configuration register with a series of WR pulses. If INH is high while writing, no conversion takes place. A conversion is started by writing INH = 0 to the configuration register. When a change is made to the contents of the configuration register, a “dummy” conversion may be necessary. This is due to a built-in latency of one full conversion for unipolar/bipolar and single-ended/differential selections.

It is not necessary to update the configuration register before every conversion. A particular mux configuration must be loaded only once after power-up (but the configuration may require several writes to be loaded). A mux configuration is retained for successive conversions and during power-down (PD = 1) so that reconfiguring is unnecessary when the ADC returns to normal operation (PD = 0). Configuration and RAM data is lost only when power is removed from the ADC at Vpp.

When updating the configuration register, INH should be high for all except the last WR so the conversion is not started until the mux is set. On WR’s falling edge, all input channels sample simultaneously. BUSY goes low at the beginning of the conversion, and channels are converted sequentially starting with the lowest selected channel. When BUSY goes high, conversion results are stored in RAM. At conversion end, a microprocessor (μP) can access the RAM contents with consecutive RD pulses. The first accessed data is the lowest channel’s result. Subsequent RD pulses access conversion results for the remaining channels.

The configuration data determines which RAM locations are sequentially read by consecutive RD pulses, so new data should be placed in the configuration register only after a full RD operation. It is not necessary to update the configuration register for every conversion. A new conversion is initiated with a WR pulse (when INH = 0), regardless of the number of channels that have been read.

Figure 4a shows the MAX155 timing for an 8-channel unipolar configuration. 8 channels are configured and 8 consecutive RD pulses access data. Figure 4b illustrates 4-channel differential conversion timing involving 4 sampled channels and 4 RD pulses. In cases where conflicting differential configurations are loaded, the last channel selected with DIFF = 1 will be the positive input of the differential channel.

**Input/Output Mode, Single-Channel Conversion Timing**

Figure 5a shows timing for a single-channel (ALL = 1), single-ended conversion. Figure 5b shows a differential conversion. With MODE floating, the configuration register is updated on the rising edge of WR. BUSY goes low at the beginning of the conversion and returns high when the channel designated by the configuration register has been converted. All channels are sampled on the falling edge of WR even if only a single channel has been requested. At conversion end, the μP can read the result for the selected channel with a single RD pulse. Subsequent RD pulses will access old conversion results remaining in other RAM locations. The next conversion is initiated with a WR pulse, regardless of the number of channels that have been read.

INH and A0-A2, in the configuration register, access locations in RAM. INH = 1 allows the RAM address pointer to be updated without starting a conversion. A READ pulse then reads the contents of the addressed location.
8-/4-Channel ADCs with Simultaneous T/Hs and Reference

NOTE: After power-up, and prior to the above timing sequence, all single-ended channels must be set up by writing the following data into the configuration register. 8 WRS (see Figure 3) are needed for 8 channels:

<table>
<thead>
<tr>
<th>A0</th>
<th>A1</th>
<th>A2</th>
<th>PD</th>
<th>INH</th>
<th>BIP</th>
<th>DIFF</th>
<th>ALL</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>S</td>
<td>0</td>
<td>0</td>
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<tr>
<td>1</td>
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<td>S</td>
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<td>0</td>
<td>1</td>
<td>S</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>S</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>S</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

S = May be selected

Once the above data is loaded, all channels are converted with a single WR to any address (this is where the above timing diagram begins). With INH = 0, and ALL = 0:

<table>
<thead>
<tr>
<th>A0</th>
<th>A1</th>
<th>A2</th>
<th>PD</th>
<th>INH</th>
<th>BIP</th>
<th>DIFF</th>
<th>ALL</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>S</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Figure 4a. Input/Output Mode Timing - Eight Single-Ended Conversions
8-/4-Channel ADCs with Simultaneous T/Hs and Reference

NOTE: After power-up, and prior to the above timing sequence, all differential channels must be set up by writing to the configuration register (AIN0, 2, 4, 6 are +, and AIN1, 3, 5, 7 are - for this example). 4 WRs (see Figure 3) are needed for 4 channels.

<table>
<thead>
<tr>
<th>A0</th>
<th>A1</th>
<th>A2</th>
<th>PD</th>
<th>INH</th>
<th>BIP</th>
<th>DIFF</th>
<th>ALL</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>S</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<td>0</td>
<td>1</td>
<td>S</td>
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<td>9</td>
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<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>S</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>S</td>
<td>1</td>
<td>9</td>
</tr>
</tbody>
</table>

S = May be selected

Once the above data is loaded, all channels are converted with a single WR to any address (this is where the above timing diagram begins). With INH = 0, and ALL = 0:

<table>
<thead>
<tr>
<th>A0</th>
<th>A1</th>
<th>A2</th>
<th>PD</th>
<th>INH</th>
<th>BIP</th>
<th>DIFF</th>
<th>ALL</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>S</td>
<td>1</td>
</tr>
</tbody>
</table>

Figure 4b: Input/Output Mode Timing - Four Differential Conversions
8-/4-Channel ADCs with Simultaneous T/Hs and Reference

**Figure 5a.** Input/Output Mode Timing - Single-Channel, Single-Ended Conversion

**Figure 5b.** Input/Output Mode Timing - Single-Channel, Differential Conversion
8-/4-Channel ADCs with Simultaneous T/Hs and Reference

**Figure 6: Input/Output Mode Timing - Reading Arbitrary RAM Locations**

### Hard-Wired Mode

For simpler applications, the MODE and VSS pins can be hard-wired to specify the type of conversion as outlined in Table 4. In this mode, the configuration register is not used, so input data on D0-D7 is ignored. For example, if MODE is tied low, an 8-channel, single-ended conversion begins with WR. With MODE tied high, a 4-channel, differential conversion is initiated with WR. Again, the configuration register is not affected by the data present on D0-D7. These conversions are otherwise identical to those shown in Figure 4.

### Analog Considerations

#### Internal Reference

The internal 2.5V reference (REFOUT) must be bypassed to AGND (Figure 8a) with a 4.7µF electrolytic and a 0.1µF ceramic capacitor to ensure stability.

#### External Reference

If an external voltage reference is used at REFIN, REFOUT must either be bypassed (Figure 8b) or disabled to prevent its output from oscillating and generating unwanted conversion noise elsewhere in the ADC. If component count is critical when using an external reference, REFOUT may be disabled by connecting it to VSS. In this case, the unused internal reference does not need a bypass capacitor. A disadvantage of using REFOUT to VSS is that power-down current will be increased by about 250µA above the specification limits.

### Table 4. Hard-Wired Mode - Multiplexer Selections

<table>
<thead>
<tr>
<th>MODE</th>
<th>VSS</th>
<th>CONVERSION TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPEN-CIRCUIT</td>
<td>X</td>
<td>Multiplexer configuration register determines conversion type. Not hard-wired.</td>
</tr>
<tr>
<td>0</td>
<td>AGND</td>
<td>8-Channel, Single-Ended, Unipolar Conversion</td>
</tr>
<tr>
<td>1</td>
<td>AGND</td>
<td>4-Channel, Differential, Unipolar Conversion</td>
</tr>
<tr>
<td>0</td>
<td>-5V</td>
<td>8-Channel, Single-Ended, Bipolar Conversion</td>
</tr>
<tr>
<td>1</td>
<td>-5V</td>
<td>4-Channel, Differential, Bipolar Conversion</td>
</tr>
</tbody>
</table>
8-/4-Channel ADCs with Simultaneous T/Hs and Reference

Figure 7a. Hard-Wired Mode Timing - Eight Single-Ended Conversions

Figure 7b. Hard-Wired Mode Timing - Four Differential Conversions
8-14-Channel ADCs with Simultaneous T/Hs and Reference

**Power-Down Mode**

The MAX155/MAX156 may be placed in a powered-down state by writing a 1 to the PD location in the configuration register (Table 1). The register may be updated while in this state (to change mux configurations or exit power-down mode) and all register contents are retained; however, no data can be read from RAM and no conversions can be started. The power-down command is implemented on WR’s rising edge.

To minimize current drain, the MAX155/MAX156 internal reference is turned off during power-down. When returning to normal operation (PD = 0), up to 5ms may be needed to allow the reference to recharge its 4.7μF bypass capacitor before a conversion is performed. If an external reference is used, and remains on during power-down, a conversion can be started within 50μs after loading PD with a 0.

**Bypassing**

A 47μF electrolytic and a 0.1μF ceramic capacitor should bypass VDD to AGND. If input signals below ground are expected, a negative supply is necessary. In that case, VSS should be bypassed to AGND with a 4.7μF and 0.1μF combination.

The internal reference requires a 4.7μF and 0.1μF combination. If an external voltage reference is used, bypass REFIN to AGND with a 4.7μF capacitor close to the chip. When an external reference is used, REFOUT must still be either bypassed or connected to VDD.

**Track/Hold Amplifiers**

The MAX155/MAX156 T/H amplifiers’ high input impedance usually requires no input buffering. All T/Hs sample simultaneously. For best results, the analog inputs should not exceed the power-supply rails (VDD, VSS) by more than 50mV.

The time required for the T/H to acquire an input signal for one channel is a function of how quickly the channel input capacitance is charged. If the source impedance of the input signal is high, acquisition takes longer, and more time must be allowed between conversions. Acquisition time is calculated by:

$$ t_{ACQ} = 8(R_S + R_N) \times 40°F \text{ (but never less than } 800μs) $$

where $$ R_N = 15kΩ $$ and $$ R_S = \text{source impedance of the ADC’s input signal} $$

**Conversion Time**

Conversion time is calculated by:

$$ t_{CONV} = \frac{9 \times N \times 2}{f_{CLK}} $$

where N is the number of channels converted. This includes one clock cycle of uncertainty. For a single channel and 5MHz clock, the conversion time is $$(9 \times 1 \times 2)/5MHz = 3.6μs.$$ For the MAX155, the maximum conversion time for 8 channels is $$(9 \times 8 \times 2)/5MHz = 28.8μs.$$ In the application example (Figure 10), six conversions are configured, and the conversion time is $$(9 \times 6 \times 2)/5MHz = 21.6μs.$$
**8-/4-Channel ADCs with Simultaneous T/Hs and Reference**

**Application Information**

**9-Bit A/D Conversion**

In I/O Mode, a 9th bit of resolution can be created by performing two unipolar differential conversions with opposite input polarities (i.e., first with AIN0[+] and AIN1[-], then with AIN0[-] and AIN1[+]). Only the A0 bit must be changed to reverse input channel polarity (Table 3). The sign reversal also occurs on the current write without any conversion delay. For a differential input signal, one of the two conversions will read 0 while the other will contain an 8-bit result. The input polarity that provides the 8-bit result indicates the 9th (sign) bit. 4 channels can be measured this way. A major drawback of this technique is that many of the sampling features of the MAX155/MAX156 are defeated since two separate samples are needed.

If only two 9-bit channels are needed, then two separate differential channels with reversed input polarities can be connected so that both input pairs sample at the same time. This way the simultaneous sampling advantages of the MAX155/MAX156 are retained.

**Typical I/O Mode Application**

MAX155/MAX156 address and configuration inputs for this example were determined by selecting the desired channel configurations in Tables 2 and 3. Figure 10 illustrates the configuration outlined in Table 5.

**Table 5. Typical Multiplexer Configuration**

<table>
<thead>
<tr>
<th>A2</th>
<th>A1</th>
<th>A0</th>
<th>DIFF</th>
<th>BIP</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Channel (1, 0), Differential, Bipolar</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Channel 2, Single-Ended, Unipolar</td>
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<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Channel 3, Single-Ended, Bipolar</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Channel 4, Single-Ended, Bipolar</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Channel 5, Single-Ended, Unipolar</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Channel (6, 7), Differential, Unipolar</td>
</tr>
</tbody>
</table>
8-/4-Channel ADCs with Simultaneous T/Hs and Reference

An A/D conversion in I/O Mode involves the following three steps:

1. Configure the mux by loading data into the configuration register based on selections from Table 2 and/or 3 (with INH = 1 and MODE = open circuit). For this example, 6 write operations (with each address and data setting in Table 5 above) load the mux after power-up.

2. Sample all selected channels with a WR pulse (and INH = 0), and update or rewrite any one location of the configuration register.

This write operation may be skipped by loading INH with a 0 on the last WR of the above step. The conversion then starts on the 6th WR. DIFF and BIP cannot be changed on the 6th WR if the conversion is started at that time.

When the conversion starts, BUSY goes low while all selected channels are sequentially converted. Conversion results are stored in RAM and are ready to read when BUSY returns high.

3. Data is read from RAM with INH = L and consecutive RD strobes. Note that in the 6 channel configurations described in this example (Figure 10), 6 RD pulses access all available data, starting with the differential channel (1,0). Additional RD pulses loop around, accessing the lowest channel data again.

4. To start a new conversion cycle with the same mux configuration, repeat steps 2 and 3.

![Typical Operating Circuit](image-url)
### Ordering Information (continued)

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP. RANGE</th>
<th>PIN-PACKAGE</th>
<th>ERROR (LSBs)</th>
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</thead>
<tbody>
<tr>
<td>MAX155AEPI</td>
<td>-40°C to +85°C</td>
<td>28 Plastic DIP</td>
<td>±1/2</td>
</tr>
<tr>
<td>MAX155BEPI</td>
<td>-40°C to +85°C</td>
<td>28 Plastic DIP</td>
<td>±1</td>
</tr>
<tr>
<td>MAX155AEWI</td>
<td>-40°C to +85°C</td>
<td>28 Wide SO</td>
<td>±1/2</td>
</tr>
<tr>
<td>MAX155BEWI</td>
<td>-40°C to +85°C</td>
<td>28 Wide SO</td>
<td>±1</td>
</tr>
<tr>
<td>MAX155AMJI</td>
<td>-55°C to +125°C</td>
<td>28 CERDIP**</td>
<td>±1/2</td>
</tr>
<tr>
<td>MAX155BMJI</td>
<td>-55°C to +125°C</td>
<td>28 CERDIP**</td>
<td>±1</td>
</tr>
<tr>
<td>MAX156ACNG</td>
<td>0°C to +70°C</td>
<td>24 Plastic DIP†</td>
<td>±1/2</td>
</tr>
<tr>
<td>MAX156BCNG</td>
<td>0°C to +70°C</td>
<td>24 Plastic DIP†</td>
<td>±1</td>
</tr>
<tr>
<td>MAX156ACWI</td>
<td>0°C to +70°C</td>
<td>28 Wide SO</td>
<td>±1/2</td>
</tr>
<tr>
<td>MAX156BCWI</td>
<td>0°C to +70°C</td>
<td>28 Wide SO</td>
<td>±1</td>
</tr>
<tr>
<td>MAX156BC/D</td>
<td>0°C to +70°C</td>
<td>Dice*</td>
<td>±1</td>
</tr>
<tr>
<td>MAX156AENG</td>
<td>-40°C to +85°C</td>
<td>24 Plastic DIP†</td>
<td>±1/2</td>
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<tr>
<td>MAX156BENG</td>
<td>-40°C to +85°C</td>
<td>24 Plastic DIP†</td>
<td>±1</td>
</tr>
<tr>
<td>MAX156AEWI</td>
<td>-40°C to +85°C</td>
<td>28 Wide SO</td>
<td>±1/2</td>
</tr>
<tr>
<td>MAX156BEWI</td>
<td>-40°C to +85°C</td>
<td>28 Wide SO</td>
<td>±1</td>
</tr>
</tbody>
</table>

* Contact factory for dice specifications.
** Contact factory for availability and processing to MIL-STD-883.
† Narrow

### Pin Configurations (continued)

**TOP VIEW**

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<tr>
<th>PIN</th>
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<td>AIN1</td>
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<td>AIN3</td>
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<td>CLK</td>
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<td>D7/ALL</td>
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<td>12</td>
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</table>

**WIDE SO**

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<tr>
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<td>Ain3</td>
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<td>mode</td>
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<td>Vss</td>
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<td>CS</td>
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</tr>
<tr>
<td>28</td>
<td>N.C.</td>
</tr>
</tbody>
</table>
8-/4-Channel ADCs with Simultaneous T/Hs and Reference

Chip Topography

NOTE: LABELS IN ( ) ARE FOR MAX156.
8-/4-Channel ADCs with Simultaneous T/Hs and Reference

Package Information

28 Lead Plastic DIP (P1)
\[ \theta_{JA} = 110°C/W \]
\[ \theta_{JC} = 50°C/W \]

28 Lead Small Outline, Wide (W1)
\[ \theta_{JA} = 80°C/W \]
\[ \theta_{JC} = 45°C/W \]