# Active Cell Balancer Extends Run Time and Lifetime of Large Series-Connected Battery Stacks

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Large stacks of series-connected battery cells are increasingly used to power electric vehicles or store energy in wind and solar power systems. It is not uncommon to have 100 cells connected in series in an electric vehicle, and even more in energy storage units for alternative energy systems. Typically, the stack is treated by the charge-discharge system as a single battery—cells are charged and discharged as a series stack and the state of charge (SoC) of each cell depends on its ability to store and maintain charge. Treating the cell stack as a single battery composed of capacity-matched cells can work well in the short term, but becomes increasingly inefficient in the long run.

When a battery stack is first constructed, the capacities of its component cells can be well matched, but over time, individual cells lose capacity at different rates due to temperature variations and other factors. In a straightforward stack charge-discharge implementation, the cell with the least capacity—the weakest cell—effectively limits the run time of the stack. When the stack is charged, the weakest cell reaches its full charge voltage before stronger cells, so stronger cells are not charged to capacity. Likewise, when the stack is discharged, the weakest cell reaches its cutoff voltage sooner, limiting run time.
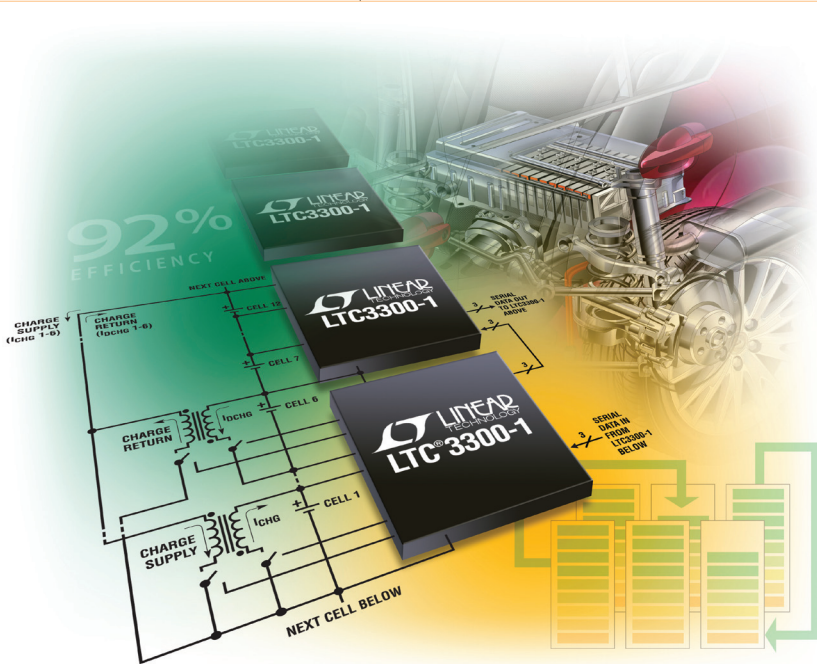
The LTC®3300-1 balances the states of charge of individual cells in large battery stacks, increasing capacity, extending run time and prolonging lifetime of the stack

LINEAR TECHNOLOGY

The LTC3300-1 is a fault-protected controller IC for transformer-based bidirectional active balancing of multicell battery stacks. Active bidirectional balancing can transfer charge from the stack to low SoC cells, or transfer charge from high SoC cells to the stack. In this way, the overall capacity of the stack is improved.

The capacity of the stack and its run time can be improved by balancing the state of charge between cells within the stack. Figure 1 shows a simplified schematic of a 12-cell balancer using two LTC3300-1 cell balancing controllers.

LTC3300-1 IMPROVES BATTERY STACK RUN TIMES AND LIFETIMES

The LTC3300-1 is a fault-protected controller IC for transformer-based bidirectional active balancing of multicell battery stacks. Active bidirectional balancing can transfer charge from the stack to low SoC cells, or transfer charge from high SoC cells to the stack. In this way, the overall capacity of the stack is improved.

A single LTC3300-1 can balance up to six series connected cells with a common mode voltage range of up to 36v. Multiple LTC3300-1 devices can be connected in series, allowing balancing of long strings of series connected cells. A unique level shifting SPI-compatible serial interface allows multiple LTC3300-1 devices to be connected in series without opto-couplers or isolators.

As the stack is charged, weaker cells operate in discharge mode and stronger cells operate in the charge mode until all cells reach their full SoC. Likewise, during discharge, weaker cells are operated in charge mode while stronger cells are operated in discharge mode until all cells reach their cutoff voltage. This extends the run time of the stack, which reduces the number of charge/discharge cycles and thus extends the life of the batteries within the stack.

With the LTC3300-1, all individual cell balancers can operate simultaneously in any combination of discharge or charge modes, even when multiple LTC3300-1 devices are used. For instance, for a stack of 12 cells, with two LTC3300-1 devices connected in series, charge can be transferred from cell 12 to cell 1 in a single time step by discharging cell 12 and charging cell 1. When compared to other methods of transferring charge between cells, this single time step method is the fastest and most efficient. A single time step can include multiple balancers in discharge or charge modes resulting in optimum balance time.

The LTC3300-1 includes fault protection, including read-back capability, cyclic redundancy check (CRC) communication error detection, maximum on-time volt-second clamps and cell or transformer secondary overvoltage shutdown.

The LTC3300-1 is available in a 48-lead 7mm × 7mm QFN or LQFP package.

HOW TO APPLY THE LTC3300-1

The cell balancer incorporates a boundary mode synchronous flyback transformer power stage that is controlled by the LTC3300-1. There are six sets of control signals within the LTC3300-1 that control the gates of the primary side and secondary side NMOS switches and current sense inputs for each pair of NMOS switches.

The naming convention used for the LTC3300-1 is that the transformer primary is connected across the battery cell and the secondary of the transformer is across the ground reference of the IC to a point six or more cells up the stack. The primary side gate signals are referenced to the next lower cell while the secondary side gates are referenced to the ground reference of the IC, the v⁻ exposed pad.
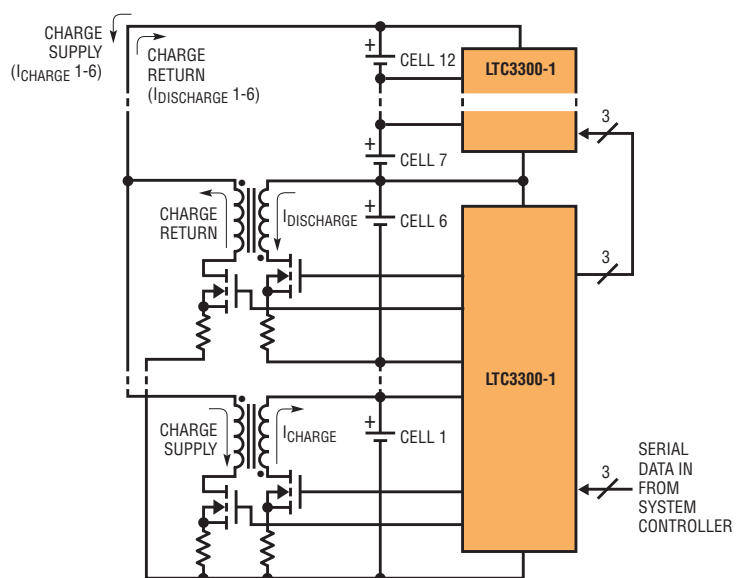

Figure 1. Simplified schematic of how the LTC3300-1 actively balances individual cells in a 12-cell battery stack

With the LTC3300-1, all individual cell balancers can operate simultaneously, in any combination of discharge or charge modes, even when multiple LTC3300-1 devices are used. For instance for a stack of 12 cells, with two LTC3300-1 devices connected in series, charge can be transferred from cell 12 to cell 1 in a single time step by discharging cell 12 and charging cell 1.

During discharge mode (Figure 2) the primary side NMOS is turned on first and remains on until the current signal ramps up to 50mV or the primary max on-time setting is reached. The flux built up in the primary side of the flyback transformer is then transferred to the secondary. The secondary gate signal turns on the second-ary side NMOS, and it remains on until the secondary current sense signal ramps down to 0mV or the secondary side max on-time is reached. The cycle repeats until the LTC3300-1 is given a command to stop the discharge mode or encounters a fault such as a watchdog timer timeout, a cell undervoltage (2.0V), a cell overvolt-age (5.0V) or a transformer secondary overvoltage caused by a lost connection.

During charge mode (Figure 3) the secondary is turned on first and remains

on until the secondary current signal ramps up to 50mV or the secondary max on-time setting is reached. The flux built up in the secondary side of the flyback transformer is then transferred to the primary. The primary gate signal turns on the primary side NMOS and it remains on until the current sense signal ramps down to 0mV or the primary side max on-time is reached. The cycle repeats until the LTC3300-1 is given a command to stop the charge mode or encounters a fault such as a watchdog timer timeout, a cell undervoltage (2.0V), a cell overvolt-age (5.0V), or a transformer secondary overvoltage caused by a lost connection.

The average balancing currents are deter-mined by the value of the current sensing resistors ($R_{SENSE(PRI)}$ and $R_{SENSE(SEC)}$), the turns ratio (1:T) from primary to secondary

of the flyback transformer, the number of cells within the secondary stack (s) and the transfer efficiency (η) of the power stage.

$$R_{SENSE(PRI)} = \frac{50mV}{2 \cdot I_{DISCHARGE}} \cdot \frac{S}{S+T}$$

$$R_{SENSE(PRI)} = \frac{50mV}{2 \cdot I_{CHARGE}} \cdot \frac{S \cdot T}{S+T} \eta_{CHARGE}$$

The turns ratio of the flyback trans-former is selected based on the number of cells across the secondary winding and the maximum reflected voltage on the primary side and secondary side NMOS switches. For a 12-cell secondary, a 1:2 turns ratio from primary to secondary provides a good balance between transfer efficiency and voltage stress on the two NMOS switches. For a larger number of cells across the secondary, a higher turns ratio can be selected and still provide
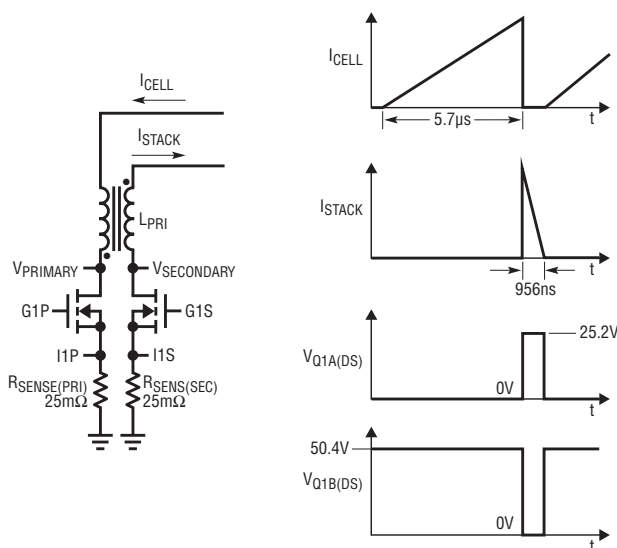

Figure 2. Discharge mode of a single cell in the stack
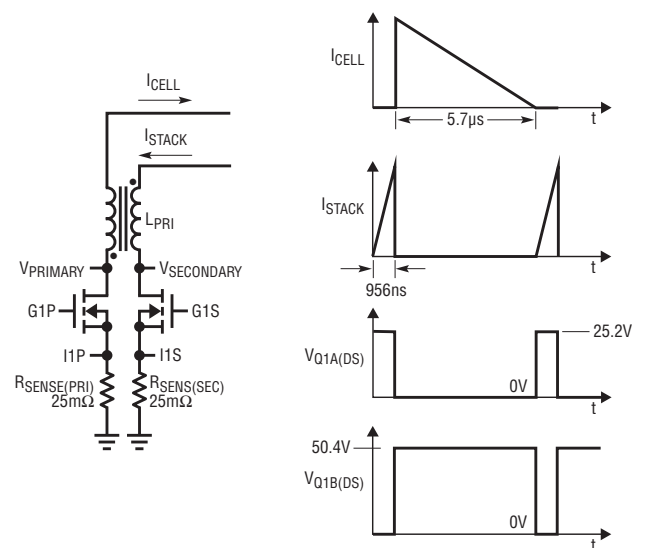

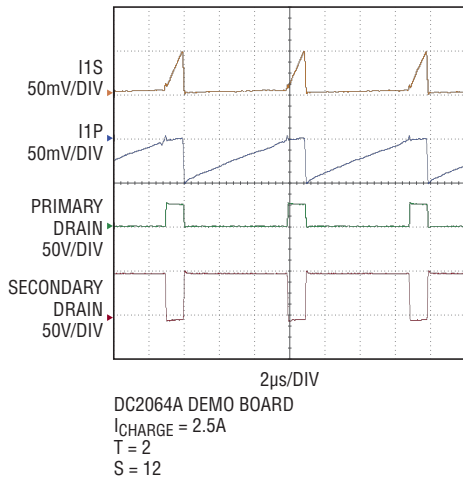Figure 3. Charge mode of a single cell in the stack

Figure 4. Demonstration circuit DC2064A typical charge mode waveforms for a 2.5A balance current
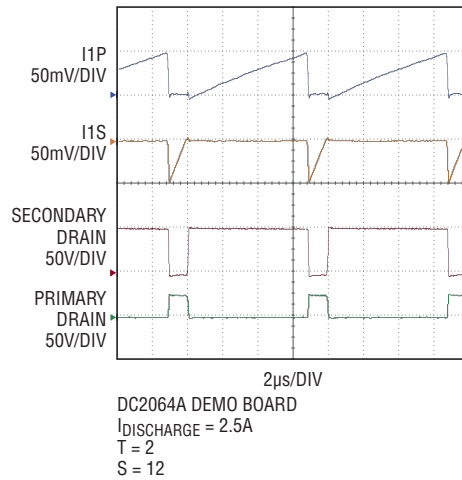

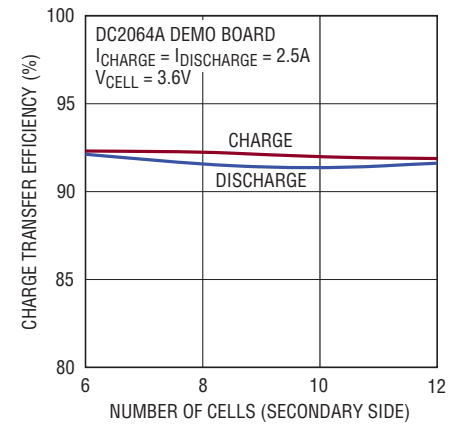Figure 5. Demonstration circuit DC2064A typical discharge mode waveforms for a 2.5A balance current

Figure 6. Cell balancer efficiency verses the number of cells across the transformer secondary winding

high transfer efficiency and manageable voltage stress on the NMOS switches.

Once the current sensing resistors and transformer turns ratio are defined, the primary inductance of the flyback transformer is determined. To do so, the operation frequency needs to be defined. The operating frequency is a function of the cell voltage, the current sensing resistor, the inductance of the primary, the number of cells within the stack, and the turns ratio of the transformer. The operating frequency is generally set to approximately 150kHz to reduce interference with other circuitry that may be in the system and to yield reasonable circuit component sizes with high transfer efficiency. The nominal cell voltage is used in this calculation.

$$L_{PRI} = \frac{S}{S+T} \cdot \frac{V_{CELL} \cdot R_{SENSE(PRI)}}{f_{DISCHARGE} \cdot 50mV}$$

$$L_{PRI} = \frac{S}{S+T} \cdot \frac{V_{CELL} \cdot R_{SENSE(SEC)}}{f_{CHARGE} \cdot 50mV \cdot T}$$

In most designs the average charge and discharge currents are set to be equal, which necessitates $R_{SENSE(SEC)} = R_{SENSE(PRI)} \cdot T$

As a result, the charge and discharge frequencies are equal. Note that the frequency of operation is a linear function of the cell voltage: 10%

shift in cell voltage results in a 10% shift in the operating frequency.

Selection of the NMOS switches is determined by the peak balancing current and the drain-to-source off-state voltage. The drain-to-source off-state voltage can be estimated using the following expressions:

$$V_{DS(PRI)MIN} > V_{CELL} \cdot \left(1 + \frac{S}{T}\right) + \frac{V_{DIODE}}{T}$$

$$V_{DS(SEC)MIN} > V_{CELL} \cdot (S+T) + T \cdot V_{DIODE}$$

Good design practice recommends that the MOSFET breakdown rating be 20% higher than this minimum calculated value to account for voltage spikes due to leakage inductance ringing. Some applications may require a series resistor capacitor snubber in parallel with the drain and source of the NMOS switch to reduce the ringing. These snubber circuits may lower the transfer efficiency but keep the NMOS devices within their safe operating region.

Additional NMOS parameters that need to be considered are the total gate charge (Q_G) and $R_{DS(ON)}$. The product of total gate charge and the operating frequency determines the gate current requirements for the primary and secondary gate drivers. The primary gate drive for cells 1–5 is sourced from the cell above the selected cell. Cell 6 primary gate drive is

sourced from the boost circuitry, which gets its energy from c6. All six secondary gate drivers are sourced from the V_{REG} circuitry. When all six balancers are operating, the secondary gate drivers present a load current on V_{REG} of:

$$I_{V(REG)} = 6 \cdot Q_G \cdot f$$

resulting in a power dissipation of:

$$P_{V(REG)} = (V_{C6} - V_{REG}) \cdot I_{V(REG)}$$

The primary gate drivers generate power dissipation in the LTC3300-1 of

$$P_{PRI(DRIVE)} = 2 \cdot V_{CELL} \cdot 6 \cdot Q_G \cdot f$$

The individual primary and secondary gate drive currents should be limited to less than 4mA.

Figure 4 shows typical charge mode waveforms for a 2.5A cell balancer with a secondary of 12 cells and a transformer turns ratio of 1:2. The primary inductance is 3µH, $R_{SENSE(PRI)}$ is 8mΩ, $R_{SENSE(SEC)}$ is 16mΩ and the cell voltage is 3.6V. Figure 5 shows the same cell balancer in discharge mode. Figure 6 shows the cell balancer efficiency for various numbers of cells connected to the secondary.

INTERLEAVING SECONDARIES IN AN 18-CELL CONFIGURATION

Large strings of cells can be accomodated by the LTC3300-1 by interleaving their secondary windings. Figure 7 shows an 18-cell stack with three LTC3300-1 ICs connected in series via the SPI-compatible serial interface. The transformer secondaries of the bottom LTC3300-1 are connected across (cell 1)⁻ and (cell 12)⁺ while secondaries of the middle LTC3300-1 are connected across (cell 6)⁺ and (cell 18)⁺. The secondaries of the top LTC3300-1 are connected across six cells, (cell 12)⁺ and (cell 18)⁺.

The lower two devices have their BOOST and TOS pins tied to their respective V⁻ pin and BOOST⁺ pins connected to the cell above the cell connected to their respective C6 pins. The top LTC3300-1 has its BOOST and TOS pins tied to the V_REG pin.

A flying capacitor is connected between the BOOST⁻ and BOOST⁺ pins along with a series 6.8Ω resistor and diode connected from the BOOST⁺ pin to cell 6. The V_MODE pin of the bottom LTC3300-1 is tied to its V_REG pin while all other devices have their V_MODE pins tied to their respective V⁻ pins.

CONCLUSION

The LTC3300-1 actively balances the state of charge of individual cells in multicell, series-connected battery stacks using a transformer-based bidirectional scheme. Active balancing extends the run time of battery stacks, which in turn extends their lifetimes. The LTC3300-1 integrates gate drive circuitry and a robust serial interface with built in watchdog timer, undervoltage and overvoltage protection in a 48-lead QFN or LQFP package. Each LTC3300-1 controls up to six cell balancers while larger stacks can be accommodated with multiple LTC3300-1 ICs connected in series using an SPI-compatible serial interface.
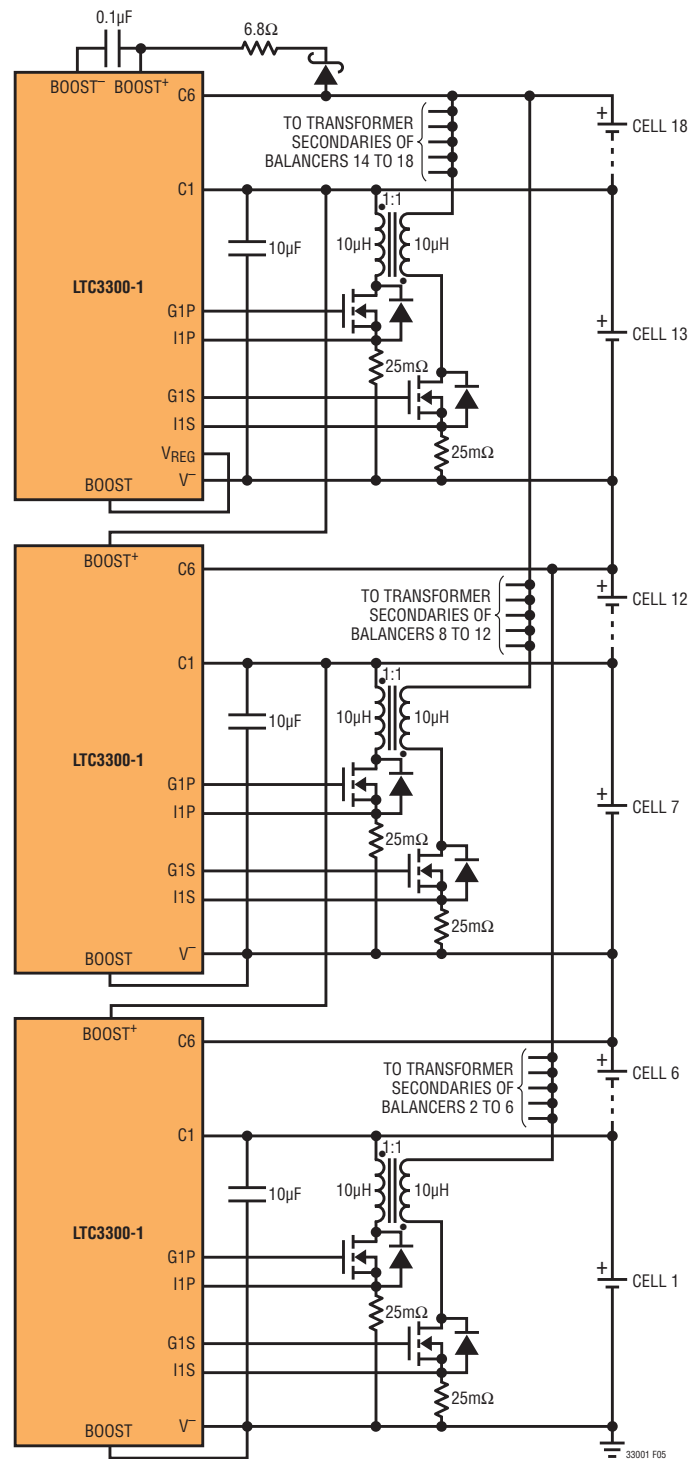

Figure 7. 18-cell active balancer

Visit www.linear.com/LTC3300-1 for data sheets, demo boards and other applications information. ∎