**FEATURES**

- **3000:1 True Color PWM™ Dimming**
- **Wide Input Voltage Range: 6V to 100V**
- **Current Monitoring Up to 100V**
- **High Side PMOS Disconnect and PWM Switch Driver**
- **Constant-Current and Constant-Voltage Regulation**
- **Dual Current Sense Amplifiers with Reporting**
- **C/10 Detection for Battery and SuperCap Charging**
- **Linear Current Sense Threshold Programming**
- **Short-Circuit Protection**
- **Adjustable Frequency: 100kHz to 1MHz**
- **Frequency Synchronization**
- **Programmable Open LED Protection with VMODE Flag**
- **Programmable Undervoltage Lockout with Hysteresis**
- **Soft-Start with Programmable Fault Restart Timer**
- **Low Shutdown Current: <1μA**
- **Available in 28-Lead TSSOP Package**

**APPLICATIONS**

- **High Power LED, High Voltage LED**
- **Battery and SuperCap Chargers**
- **Accurate Current Limited Voltage Regulators**

**DESCRIPTION**

The LT®3796 is a DC/DC controller designed to regulate a constant-current or constant-voltage and is ideal for driving LEDs. It drives a low side external N-channel power MOSFET from an internal regulated 7.7V supply. The fixed frequency and current mode architecture result in stable operation over a wide range of supply and output voltages. Two ground referred voltage FB pins serve as the input for several LED protection features, and also allow the converter to operate as a constant-voltage source. The LT3796 features a programmable threshold output sense amplifier with rail-to-rail common mode range. The LT3796 also includes a separate high side current sensing amplifier that is gain configurable with two resistors. The TG pin inverts and level shifts the PWM signal to drive the gate of the external PMOS. The PWM input provides LED dimming ratios of up to 3000:1, and the CTRL input provides additional analog dimming capability.

**TYPICAL APPLICATION**

Boost LED Driver with Input Current Monitor

![Boost LED Driver with Input Current Monitor Diagram]

**Efficiency vs VIN**

![Efficiency vs VIN Graph]
LT3796

**ABSOLUTE MAXIMUM RATINGS**
(Note 1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN, VS}$</td>
<td>100V</td>
</tr>
<tr>
<td>EN/UVLO</td>
<td>100V</td>
</tr>
<tr>
<td>ISP, ISN</td>
<td>100V</td>
</tr>
<tr>
<td>TG, GATE</td>
<td>Note 3</td>
</tr>
<tr>
<td>CSP, CSN</td>
<td>100V</td>
</tr>
<tr>
<td>$V_S - CSP, V_S - CSN$</td>
<td>$-0.3V$ to $4V$</td>
</tr>
<tr>
<td>$INT_{CC}$ (Note 2)</td>
<td>$8.6V, V_{IN} + 0.3V$</td>
</tr>
<tr>
<td>PWM, VMODE, FAULT</td>
<td>12V</td>
</tr>
<tr>
<td>FB1, FB2, SYNC</td>
<td>8V</td>
</tr>
<tr>
<td>CTRL</td>
<td>15V</td>
</tr>
<tr>
<td>SENSE</td>
<td>0.5V</td>
</tr>
<tr>
<td>ISMON, CSOUT</td>
<td>5V</td>
</tr>
<tr>
<td>$V_C, V_{REF}, SS$</td>
<td>3V</td>
</tr>
<tr>
<td>RT</td>
<td>2V</td>
</tr>
</tbody>
</table>

Operating Junction Temperature Range (Note 4)

- LT3796E/LT3796I: $-40$ to $125°C$
- LT3796H: $-40$ to $150°C$

Storage Temperature Range: $-65$ to $150°C$

**PIN CONFIGURATION**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ISP</td>
</tr>
<tr>
<td>2</td>
<td>ISN</td>
</tr>
<tr>
<td>3</td>
<td>TG</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>ISMON</td>
</tr>
<tr>
<td>6</td>
<td>FB2</td>
</tr>
<tr>
<td>7</td>
<td>FB1</td>
</tr>
<tr>
<td>8</td>
<td>$V_C$</td>
</tr>
<tr>
<td>9</td>
<td>CTRL</td>
</tr>
<tr>
<td>10</td>
<td>$V_{REF}$</td>
</tr>
<tr>
<td>11</td>
<td>SS</td>
</tr>
<tr>
<td>12</td>
<td>RT</td>
</tr>
<tr>
<td>13</td>
<td>SYNC</td>
</tr>
<tr>
<td>14</td>
<td>PWM</td>
</tr>
<tr>
<td>15</td>
<td>FAULT</td>
</tr>
<tr>
<td>16</td>
<td>GMODE</td>
</tr>
<tr>
<td>17</td>
<td>GND</td>
</tr>
<tr>
<td>18</td>
<td>GND</td>
</tr>
<tr>
<td>19</td>
<td>$V_{IN}$</td>
</tr>
<tr>
<td>20</td>
<td>INT$_{CC}$</td>
</tr>
<tr>
<td>21</td>
<td>GND</td>
</tr>
<tr>
<td>22</td>
<td>GND</td>
</tr>
<tr>
<td>23</td>
<td>GND</td>
</tr>
<tr>
<td>24</td>
<td>GND</td>
</tr>
<tr>
<td>25</td>
<td>$V_S$</td>
</tr>
<tr>
<td>26</td>
<td>CSN</td>
</tr>
<tr>
<td>27</td>
<td>CSP</td>
</tr>
<tr>
<td>28</td>
<td>CSOUT</td>
</tr>
</tbody>
</table>

**ORDER INFORMATION**

<table>
<thead>
<tr>
<th>Lead Free Finish</th>
<th>Tape and Reel</th>
<th>Part Marking*</th>
<th>Package Description</th>
<th>Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT3796E#PBF</td>
<td>LT3796E#TRPBF</td>
<td>LT3796FE</td>
<td>28-Lead Plastic TSSOP</td>
<td>$-40°C$ to $125°C$</td>
</tr>
<tr>
<td>LT3796I#PBF</td>
<td>LT3796I#TRPBF</td>
<td>LT3796FE</td>
<td>28-Lead Plastic TSSOP</td>
<td>$-40°C$ to $125°C$</td>
</tr>
<tr>
<td>LT3796H#PBF</td>
<td>LT3796H#TRPBF</td>
<td>LT3796FE</td>
<td>28-Lead Plastic TSSOP</td>
<td>$-40°C$ to $150°C$</td>
</tr>
</tbody>
</table>

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: [http://www.linear.com/leadfree/](http://www.linear.com/leadfree/)

For more information on tape and reel specifications, go to: [http://www.linear.com/tapeandreel/](http://www.linear.com/tapeandreel/)
## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \( T_A = 25^\circ C \), \( V_{\text{IN}} = 24V \), EN/UVLO = 24V, CTRL = 2V, PWM = 5V, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{IN}} ) Minimum Operating Voltage</td>
<td>( V_{\text{IN}} ) Tied to INTVCC</td>
<td>6</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{IN}} ) Shutdown ( I_Q )</td>
<td>( \text{EN/UVLO} = 0V, \text{PWM} = 0V )</td>
<td>1</td>
<td></td>
<td>12</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( V_{\text{IN}} ) Operating ( I_Q ) (Not Switching)</td>
<td>( R_T = 82.5k ) to GND, ( \text{FB1} = 1.5V )</td>
<td>2.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{REF}} ) Voltage</td>
<td>( -100\mu A \leq I_{\text{REF}} \leq 10\mu A )</td>
<td>1.97</td>
<td>2.015</td>
<td>2.06</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{REF}} ) Pin Line Regulation</td>
<td>( 6V &lt; V_{\text{IN}} &lt; 100V )</td>
<td>1.5</td>
<td></td>
<td></td>
<td>m%/V</td>
</tr>
<tr>
<td>( V_{\text{REF}} ) Pin Load Regulation</td>
<td>( -100\mu A &lt; I_{\text{REF}} &lt; 0\mu A )</td>
<td>10</td>
<td></td>
<td></td>
<td>m%/( \mu A )</td>
</tr>
<tr>
<td>SENSE Current Limit Threshold</td>
<td></td>
<td>100</td>
<td>113</td>
<td>125</td>
<td>mV</td>
</tr>
<tr>
<td>SENSE Input Bias Current</td>
<td>Current Out of Pin</td>
<td>60</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>SS Sourcing Current</td>
<td>( SS = 0V )</td>
<td>28</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>SS Sinking Current</td>
<td>( I_{\text{ISP}} - I_{\text{ISN}} = 1V, SS = 2V )</td>
<td>2.8</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
</tbody>
</table>

### Error Amplifier

- **Full Scale LED Current Sense Threshold** (\( V_{\text{ISP-ISMN}} \))
  - \( ISN = 48V \), CTRL \( \geq 1.2V \)
  - \( ISN = 0V \), CTRL \( \geq 1.2V \)
  - 243 mV

- **9/10th LED Current Sense Threshold** (\( V_{\text{ISP-ISMN}} \))
  - CONTROL = 1V, \( ISP = 48V \)
  - 220 mV

- **1/2 LED Current Sense Threshold** (\( V_{\text{ISP-ISMN}} \))
  - CONTROL = 0.6V, \( ISP = 48V \)
  - 119 mV

- **1/10th LED Current Sense Threshold** (\( V_{\text{ISP-ISMN}} \))
  - CONTROL = 0.2V, \( ISP = 48V \)
  - 16 mV

- **ISP/ISN Current Monitor Voltage** (\( V_{\text{ISMON}} \))
  - \( V_{\text{ISP-ISMN}} = 250mV \), \( ISP = 48V \), \( -50\mu A < I_{\text{ISMON}} < 0 \mu A \)
  - 0.96 V

- **CTRL Input Bias Current**
  - Current Out of Pin, \( CTRL = 1.2V \)
  - 50 nA

### Common Mode Range

- **ISP/ISN Input Current Bias Current**
  - PWM = 5V (Active), \( ISP = 48V \)
  - 0 \( \mu A \)

- **FB1, FB2 Pin Input Bias Current**
  - \( FB = V_{\text{FB}} \)
  - 800 \( \mu S \)

### Comparator

- **FB1 Overvoltage Threshold**
  - \( V_{\text{FB}} + 35mV \)

### Other

- **FB1 Amplifier \( g_m \)**
  - 800 \( \mu S \)

- **FB2 Amplifier \( g_m \)**
  - 130 \( \mu S \)

### Additional Specifications

- **FB1, FB2 Amplifier Gate Drive**
  - 100 \( \mu A \)

- **FB1, FB2 Amplifier Gate Drive**
  - 200 \( \mu A \)

- **VC Output Impedance**
  - 2000 k\( \Omega \)

- **VC Standby Input Bias Current**
  - 20 \( \mu A \)

- **C/10 Comparator Threshold** (\( V_{\text{ISP-ISMN}} \))
  - \( V_{\text{FAUL T}} = 250mV \)

- **FB1 Overvoltage Threshold**
  - \( V_{\text{FB}} + 35mV \)

- **FB2 Overvoltage Threshold**
  - \( V_{\text{FB}} + 35mV \)

- **VC Current Mode Gain** (\( \Delta V_{\text{VC}}/\Delta V_{\text{SENSE}} \))
  - 4.2 V/V

---

3796

**LT3796**
### ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \( T_A = 25^\circ C \), \( V_{\text{IN}} = 24V \), EN/UVLO = 24V, CTRL = 2V, PWM = 5V, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Current Sense Amplifier (CSA)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Supply Voltage Range (( V_S ))</td>
<td>●</td>
<td>3</td>
<td>100</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>CSA Input Voltage Common Mode Range (( V_{\text{CSP}} ) and ( V_{\text{CSN}} ))</td>
<td>●</td>
<td>2.5</td>
<td>100</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>CSOUT Maximum Output Current</td>
<td>( CSOUT = 10k\Omega ) to GND</td>
<td>●</td>
<td>200</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>Input Voltage Offset (( V_{\text{CSP-CSN}} ))</td>
<td>●</td>
<td>–3</td>
<td>0</td>
<td>3</td>
<td>mV</td>
</tr>
<tr>
<td>CSP, CSN Input Bias Current</td>
<td>( V_{\text{SNS}} = 0mV ), ( R_{\text{IN1}} = R_{\text{IN2}} = 1k ) (Note 5)</td>
<td>100</td>
<td>nA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CSP, CSN Input Current Offset</td>
<td>( V_{\text{SNS}} = 0mV ), ( R_{\text{IN1}} = R_{\text{IN2}} = 1k ) (Note 5)</td>
<td>0</td>
<td>nA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_S ) Supply Current</td>
<td>( V_S = 48V )</td>
<td>80</td>
<td>( \mu A )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Step Response (to 50% of Output Step)</td>
<td>( \Delta V_{\text{SENSE}} = 100mV ) Step, ( R_{\text{IN1}} = R_{\text{IN2}} = 1k ), ( R_{\text{OUT}} = 10k )</td>
<td>1</td>
<td>( \mu s )</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Linear Regulator</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( INTV_{\text{CC}} ) Regulation Voltage</td>
<td>●</td>
<td>7.4</td>
<td>7.7</td>
<td>8</td>
<td>V</td>
</tr>
<tr>
<td>Dropout (( VIN – INTV_{\text{CC}} ))</td>
<td>( INTV_{\text{CC}} = -20mA ), ( VIN = 6V )</td>
<td>400 mV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( INTV_{\text{CC}} ) Current Limit</td>
<td>( VIN = 100V ), ( INTV_{\text{CC}} = 6V )</td>
<td>20 mA</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( INTV_{\text{CC}} ) Shutdown Bias Current if Externally Driven to 7V</td>
<td>( INTV_{\text{CC}} = 7V )</td>
<td>10 ( \mu A )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( INTV_{\text{CC}} ) Undervoltage Lockout</td>
<td></td>
<td>3.8</td>
<td>4</td>
<td>4.1</td>
<td>V</td>
</tr>
<tr>
<td>( INTV_{\text{CC}} ) Undervoltage Lockout Hysteresis</td>
<td></td>
<td>150</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Oscillator</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>( RT = 82.5k )</td>
<td>85 kHz</td>
<td>125 kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( RT = 19.6k )</td>
<td>340 kHz</td>
<td>480 kHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( RT = 6.65k )</td>
<td>900 kHz</td>
<td>1150 kHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum Off-Time</td>
<td>(Note 6)</td>
<td>190 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum On-Time</td>
<td>(Note 6)</td>
<td>210 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>LOGIC Input/Outputs</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PWM Input Threshold Rising</td>
<td>●</td>
<td>0.96</td>
<td>1</td>
<td>1.04</td>
<td>V</td>
</tr>
<tr>
<td>PWM Pin Bias Current</td>
<td></td>
<td>10 ( \mu A )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN/UVLO Threshold Voltage Falling</td>
<td>●</td>
<td>1.185</td>
<td>1.220</td>
<td>1.250</td>
<td>V</td>
</tr>
<tr>
<td>EN/UVLO Rising Hysteresis</td>
<td></td>
<td>20 ( mV )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN/UVLO Input Low Voltage</td>
<td>( I_{\text{VIN}} ) Drops Below 1( \mu A )</td>
<td>0.4 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN/UVLO Pin Bias Current Low</td>
<td>( EN/\text{UVLO} = 1.15V )</td>
<td>2.5 ( \mu A )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN/UVLO Pin Bias Current High</td>
<td>( EN/\text{UVLO} = 1.30V )</td>
<td>40 ( \mu A )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VMODE OUTPUT Low</td>
<td>( I_{\text{VMODE}} = 0.5mA )</td>
<td>300 mV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FAULT OUTPUT Low</td>
<td>( I_{\text{FAULT}} = 0.5mA )</td>
<td>300 ( mV )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SYNC Pin Resistance to GND</td>
<td></td>
<td>40 ( \Omega )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SYNC Input Low Threshold</td>
<td></td>
<td>0.4 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SYNC Input High Threshold</td>
<td></td>
<td>1.5 V</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$, $V_{IN} = 24V$, $EN/UVLO = 24V$, $CTRL = 2V$, $PWM = 5V$, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Driver</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_r$ NMOS GATE Driver Output Rise Time</td>
<td>$C_L = 3300pF; 10% to 90%$</td>
<td></td>
<td></td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>$t_f$ NMOS GATE Driver Output Fall Time</td>
<td>$C_L = 3300pF; 10% to 90%$</td>
<td></td>
<td></td>
<td>18</td>
<td>ns</td>
</tr>
<tr>
<td>NMOS GATE Output Low ($V_{OL}$)</td>
<td></td>
<td></td>
<td></td>
<td>0.05</td>
<td>V</td>
</tr>
<tr>
<td>NMOS GATE Output High ($V_{OH}$)</td>
<td></td>
<td></td>
<td></td>
<td>INTVCC 0.05</td>
<td>V</td>
</tr>
<tr>
<td>Top Gate Driver Output Rise Time</td>
<td>$C_L = 300pF$</td>
<td></td>
<td></td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>Top Gate Driver Output Fall Time</td>
<td>$C_L = 300pF$</td>
<td></td>
<td></td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>Top Gate On Voltage ($V_{ISP-VTG}$)</td>
<td>$ISP = 48V$</td>
<td></td>
<td></td>
<td>7</td>
<td>8</td>
</tr>
<tr>
<td>Top Gate Off Voltage ($V_{ISP-VTG}$)</td>
<td>$PWM = 0V$, $ISP = 48V$</td>
<td></td>
<td></td>
<td>0</td>
<td>0.3</td>
</tr>
</tbody>
</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Operating maximum for INTVCC is 8V.

**Note 3:** Do not apply a positive or negative voltage source to TG and GATE pins, otherwise permanent damage may occur.

**Note 4:** The LT3796E is guaranteed to meet specified performance from 0°C to 125°C. Specifications over the –40°C to 125°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LT3796I is guaranteed to meet performance specifications over the –40°C to 125°C operating temperature range. The LT3796H is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

**Note 5:** Measured in servo. See Figure 9 for details.

**Note 6:** See Duty Cycle Considerations in the Applications Information section.
TYPICAL PERFORMANCE CHARACTERISTICS

\( T_A = 25^\circ C, \) unless otherwise noted.

\[ V_{\text{ISP-ISN}} \text{ Threshold vs } V_{\text{CTRL}} \]

\[ V_{\text{ISP-ISN}} \text{ Threshold vs } V_{\text{ISP}} \]

\[ V_{\text{ISP-ISN}} \text{ Full-Scale Threshold vs Temperature} \]

\( V_{\text{ISP-ISN}} \text{ Threshold at } V_{\text{CTRL}} = 0.6V \text{ vs Temperature} \)

\( V_{\text{ISP-ISN}} \text{ Threshold vs } V_{\text{FB}} \text{ Voltage} \)

\( V_{\text{FB}} \text{ vs Temperature} \)

ISP/ISN Overcurrent Protection Threshold vs Temperature

ISP/ISN Input Bias Current vs \( V_{\text{ISP}}, V_{\text{ISN}} \)

\( V_{\text{REF}} \text{ Voltage vs Temperature} \)
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ C$, unless otherwise noted.

### VREF vs VIN

- $I_{REF} = 0 \mu A$
- $V_{REF} (V)$ vs $V_{IN} (V)$

### RT vs Switching Frequency

- $R_T (\Omega)$ vs Switching Frequency (kHz)

### Switching Frequency vs Temperature

- $R_T = 19.8 \Omega$
- $Switching Frequency$ vs $Temperature (^\circ C)$

### Switching Frequency vs SS Voltage

- $Switching Frequency (kHz)$ vs $SS Voltage (mV)$
- $PWM = 0V$

### Quiescent Current vs VIN

- $V_{IN} (V)$ vs $I_{IN} (mA)$
- $PWM = 0V$

### VISMON vs V(ISP-ISN)

- $V_{ISMON} (mV)$ vs $V_{ISPN} (mV)$

### EN/UVLO Hysteresis Current vs Temperature

- $EN/UVLO Hysteresis CURRENT (\mu A)$ vs $TEMPERATURE (^\circ C)$

### EN/UVLO Falling/Rising Threshold vs Temperature

- $EN/UVLO RISING/FALING THRESHOLD$ vs $TEMPERATURE (^\circ C)$

### SENSE Current Limit Threshold vs Temperature

- $SENSE THRESHOLD (mV)$ vs $TEMPERATURE (^\circ C)$
**TYPICAL PERFORMANCE CHARACTERISTICS**

\[ T_A = 25^\circ C, \text{ unless otherwise noted.} \]

---

**SENSE Current Limit Threshold vs Duty Cycle**

**INTVCC Current Limit vs \( V_IN \)**

**INTVCC Current Limit vs Temperature**

**INTVCC vs \( V_IN \)**

**INTVCC Dropout Voltage vs Current, Temperature**

**INTVCC vs Temperature**

**\( V_{(CSP-CSN)} \) Offset Voltage with Different \( I_{CSOUT} \) vs \( V_S \)**

**\( V_{(CSP-CSN)} \) Offset Voltage vs Temperature**

**Current Sense Amplifier Gain Error vs Temperature**

---

**SEE NOTE 5 FOR TEST SETUP**
TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ C$, unless otherwise noted.

- **Current Sense Amplifier Gain vs Frequency**
- **NMOS Gate Rise/Fall Time vs Capacitance**
- **Top Gate (PMOS) Rise/Fall Time vs Capacitance**

**Top Gate Driver Rising Edge**

**Top Gate Driver Falling Edge**

$V_S = 48V$, $R_{IN} = 1k$
$R_{OUT} = 10k$, $V_{SENSE} = 100mV$
(NOTE 5)

PMOS VISHAY SILICONIX Si7113DN
PIN FUNCTIONS

ISP (Pin 1): Connection Point for the Positive Terminal of the Current Feedback Resistor \( R_{LED} \). Also serves as positive rail for TG pin driver.

ISN (Pin 2): Connection Point for the Negative Terminal of the Current Feedback Resistor \( R_{LED} \).

TG (Pin 3): Top Gate Driver Output. An inverted PWM signal drives series PMOS device between \( V_{ISP} \) and \( (V_{ISP} - 7V) \) if \( V_{ISP} > 7V \). An internal 7V clamp protects the PMOS gate by limiting VGS. Leave TG unconnected if not used.

GND (Pins 4, 17, 21, 22, Exposed Pad Pin 29): Ground. These pins also serve as current sense input for control loop, sensing negative terminal of current sense resistor in the source of the N-channel MOSFET. Solder the exposed pad directly to ground plane.

ISMON (Pin 5): ISP/ISN Current Report Pin. The LED current sensed by ISP/ISN inputs is reported as \( V_{ISMON} = I_{LED} \cdot R_{LED} \cdot 4 \). Leave ISMON pin unconnected if not used.

When PWM is low, ISMON is driven to ground. Bypass with a 47nF capacitor or higher if needed.

FB2 (Pin 6): Voltage Loop Feedback 2 Pin. This pin is connected to the internal transconductance amplifier positive input node. The internal transconductance amplifier with output \( V_C \) regulates FB2 to 1.25V through the DC/DC converter. If FB2 is driven above 1.3V, the TG pin is pulled high to turn off the external PMOS and GATE pin is driven to GND to turn off the external N-channel MOSFET. Connect to GND if not used.

FB1 (Pin 7): Voltage Loop Feedback 1 Pin. FB1 is intended for constant-voltage regulation or for LED protection/open LED detection. The internal transconductance amplifier with output \( V_C \) regulates FB1 to 1.25V (nominal) through the DC/DC converter. If the FB1 input is regulating the loop and \( V_{ISP-ISN} \) is less than 25mV (normal), the VMODE pull-down is asserted. This action may signal an open LED fault. If FB1 is driven above the 1.3V (by an external power supply spike, for example), the FAULT pull-down is asserted, the GATE pin is pulled low to turn off the external N-channel MOSFET and the TG pin is driven high to protect the LEDs from an overcurrent event. Do not leave the FB1 pin open. If not used, connect FB1 to GND.

\( V_C \) (Pin 8): Transconductance Error Amplifier Output Pin. Used to stabilize the control loop with an RC network. This pin is high impedance when PWM is low, a feature that stores the demand current state variable for the next PWM high transition. Connect a capacitor between this pin and GND; a resistor in series with the capacitor is recommended for fast transient response. Do not leave this pin open.

CTRL (Pin 9): Current Sense Threshold Adjustment Pin. Regulating threshold \( V_{ISP-ISN} \) is \( 0.25 \cdot V_{CTRL} \) plus an offset for \( 0.1V < V_{CTRL} < 1V \). For \( V_{CTRL} > 1.2V \) the current sense threshold is constant at the full-scale value of 250mV. For \( 1V < V_{CTRL} < 1.2V \), the dependence of the current sense threshold upon \( V_{CTRL} \) transitions from a linear function to a constant value, reaching 98% of full-scale value by \( V_{CTRL} = 1.1V \). Connect CTRL to VREF for the 250mV default current threshold. Do not leave this pin open. Pull CTRL pin to GND for zero LED current.

\( V_{REF} \) (Pin 10): Voltage Reference Output Pin. Typically 2.015V. This pin drives a resistor divider for the CTRL pin, either for analog dimming or for temperature limit/compensation of LED load. It can supply up to 100μA.

SS (Pin 11): Soft-Start Pin. This pin modulates oscillator frequency and compensation pin voltage \( V_C \) clamp. The soft-start interval is set with an external capacitor. The pin has a 28μA (typical) pull-up current source to an internal 2.5V rail. This pin can be used as fault timer. Provided the SS pin has exceeded 1.7V, the pull-up current source is disabled and a 2.8μA pull-down current enabled when any one of the following fault conditions happen:

1. LED overcurrent
2. INTVCC undervoltage
3. Thermal limit

The SS pin must be discharged below 0.2V to reinitiate a soft-start cycle. Switching is disabled until SS is recharged.

RT (Pin 12): Switching Frequency Adjustment Pin. Set the frequency using a resistor to GND (for resistor values, see the Typical Performance curve or Table 2). Do not leave the RT pin open.
**PIN FUNCTIONS**

**SYNC (Pin 13):** The SYNC pin is used to synchronize the internal oscillator to an external logic level signal. If SYNC is used, the $R_T$ resistor should be chosen to program an internal switching frequency 20% slower than the SYNC pulse frequency. Gate turn-on occurs a fixed delay after the rising edge of SYNC. Use a 50% duty cycle waveform to drive this pin. If not used, tie this pin to GND.

**PWM (Pin 14):** PWM Input Signal Pin. A signal low turns off switching, idles the oscillator, disconnects the $V_C$ pin from all internal loads, and makes the TG pin high.

**FAULT (Pin 15):** An open-collector pull-down on FAULT asserts when any of the following conditions happen: 1. FB1 overvoltage ($V_{FB1} > 1.3V$), 2. INTVCC undervoltage, 3. LED overcurrent ($V_{ISP-ISN} > 375mV$), or 4. Thermal shutdown. If all faults are removed, FAULT flag returns high. Fault status is only updated during PWM high state and latched during PWM low state. FAULT remains asserted until the SS pin is discharged below 0.2V for cases 2, 3 and 4 above.

**VMODE (Pin 16):** An open-collector pull-down on VMODE asserts if the FB1 input is above 1.19V (typical), and $V_{ISP-ISN}$ is less than 25mV (typical). To function, the pin requires an external pull-up resistor. VMODE status is updated only during PWM high state and latched during PWM low state.

**SENSE (Pin 18):** The current sense input for the control loop. Kelvin connect this pin to the positive terminal of the switch current sense resistor, $R_{SENSE}$, in the source of the N-channel MOSFET. The negative terminal of the current sense resistor should be Kelvin connected to the GND plane of the IC.

**GATE (Pin 19):** N-Channel MOSFET Gate Driver Output. Switches between INTVCC and GND. It is driven to GND during shutdown, fault or idle states.

**INTVCC (Pin 20):** Regulated Supply for Internal Loads, GATE Driver and Top Gate (PMOS) Driver. Supplied from $V_{IN}$ and regulates to 7.7V (typical). INTVCC must be bypassed with a 4.7μF capacitor placed close to the pin. Connect INTVCC directly to $V_{IN}$ if $V_{IN}$ is always less than or equal to 7V.

**$V_{IN}$ (Pin 23):** Input Supply Pin. Must be locally bypassed with a 0.22μF (or larger) capacitor placed close to the IC.

**EN/UVLO (Pin 24):** Enable and Undervoltage Lockout Pin. An accurate 1.22V falling threshold with externally programmable hysteresis detects when power is OK to enable switching. Rising hysteresis is generated by the external resistor divider and an accurate internal 3μA pull-down current. Above the threshold (but below 6V), EN/UVLO input bias current is sub-μA. Below the falling threshold, a 3μA pull-down current is enabled so the user can define the hysteresis with the external resistor selection. An undervoltage condition resets soft-start. Tie to 0.4V, or less, to disable the device and reduce $V_{IN}$ quiescent current below 1μA.

**$V_S$ (Pin 25):** Current Sense Amplifier Power Supply Pin. This pin supply current to the current sense amplifier and can operate from 3V to 100V.

**CSN (Pin 26):** Negative Current Sense Input Terminal. CSN remains functional for voltages up to 100V. Typically connected to $V_S$ and CSP as shown in Figure 9.

**CSP (Pin 27):** Positive Current Sense Input Terminal. The internal sense amplifier sinks current from CSP to regulate it to the same potential as CSN. A resistor ($R_{IN1}$) tied from $V_{IN}$ to CSP sets the output current $I_{CSOUT} = V_{SNS}/R_{IN1}$. $V_{SNS}$ is the voltage developed across $R_{SNS}$. See Figure 9.

**CSOUT (Pin 28):** Current Sense Amplifier Output. CSOUT pin sources the current that is drawn from CSP. Typically is output to an external resistor to GND.
The LT3796 is a constant-frequency, current mode controller with a low side NMOS gate driver. The operation of the LT3796 is best understood by referring to the Block Diagram. In normal operation, with the PWM pin low, the GATE pin is driven to GND, the TG pin is pulled high to ISP to turn off the PMOS disconnect switch, the VC pin goes high impedance to store the previous switching state on the external compensation capacitor, and the ISP and ISN pin bias currents are reduced to leakage levels. When the PWM pin transitions high, the TG pin transitions low after a short delay. At the same time, the internal oscillator wakes up and generates a pulse to set the PWM latch, turning on the external power N-channel MOSFET switch (GATE goes high). A voltage input proportional to the switch current, sensed by an external current sense resistor between the SENSE and GND input pins, is added to a stabilizing slope compensation ramp and the resulting switch current sense signal is fed into the negative terminal of the PWM comparator. The current in the external inductor increases steadily during the time the switch is on. When the switch current sense voltage exceeds the output of the error amplifier, labeled VC, the latch is reset and the switch is turned off. During the switch off phase, the inductor current decreases. At the completion of each oscillator cycle, internal signals such as slope compensation return to their starting points and a new cycle begins with the set pulse from the oscillator. Through this repetitive action, the PWM control algorithm establishes a switch duty cycle to regulate a current or voltage in the load. The VC signal is integrated over many switching cycles and is an amplified version of the difference between the LED current sense voltage, measured between ISP and ISN, and the target difference voltage set by the CTRL pin. If the SENSE pin exceeds the current limit threshold of 113mV (typical), the SR latch is reset regardless of the output state of the PWM comparator. Likewise, any fault condition, i.e. FB1 overvoltage (V_{FB1} > 1.3V), LED over current, or INT V_{CC} undervoltage (INT V_{CC} < 4V), the GATE pin is pulled down to GND immediately.

In voltage feedback mode, the operation is similar to that described above, except the voltage at the VC pin is set by the amplified difference of the internal reference of 1.25V (nominal) and the FB1 and FB2 pins. If FB1 and FB2 are both lower than the reference voltage, the switch current increases; if FB1 or FB2 is higher than the reference voltage, the switch demand current decreases. The LED current sense feedback interacts with the voltage feedback so that neither FB1 or FB2 exceeds the internal reference and the voltage between ISP and ISN does not exceed the threshold set by the CTRL pin. For accurate current or voltage regulation, it is necessary to be sure that under normal operating conditions, the appropriate loop is dominant. To deactivate the voltage loop entirely, FB1 and FB2 can be connected to GND. To deactivate the LED current loop entirely, the ISP and ISN should be tied together and the CTRL input tied to V_{REF}.

Two LED specific functions featured on the LT3796 are controlled by the voltage feedback FB1 pin. First, when the FB1 pin exceeds a voltage 60mV lower (–5%) than the FB1 regulation voltage and V(ISP-ISN) is less than 25mV (typical), the pull-down driver on the VMODE pin is activated. This function provides a status indicator that the load may be disconnected and the constant-voltage feedback loop is taking control of the switching regulator. When the FB1 pin exceeds the FB1 regulation voltage by 50mV (4% typical), the FAULT pin is activated.

LT3796 features a PMOS disconnect switch driver. The PMOS disconnect switch can be used to improve the PWM dimming ratio, and operate as fault protection as well. Once a fault condition is detected, the TG pin is pulled high to turnoff the PMOS switch. The action isolates the LED array from the power path, preventing excessive current from damaging the LEDs.

A standalone current sense amplifier is integrated in the LT3796. It can work as input current limit or open LED protection. The detailed information can be found in the Application Information section.
APPLICATIONS INFORMATION

INTVCC Regulator Bypassing and Operation

The INTVCC pin requires a capacitor for stable operation and to store the charge for the large GATE switching currents. Choose a 10V rated low ESR, X7R or X5R ceramic capacitor for best performance. A 4.7μF ceramic capacitor is adequate for many applications. Place the capacitor close to the IC to minimize the trace length to the INTVCC pin and also to the power ground.

An internal current limit on the INTVCC output protects the LT3796 from excessive on-chip power dissipation. The minimum value of this current limit should be considered when choosing the switching N-channel MOSFET and the operating frequency. I_{INTVCC} can be calculated from the following equation:

\[ I_{INTVCC} = Q_G \cdot f_{OSC} \]

Careful choice of a lower Q_G MOSFET allows higher switching frequencies, leading to smaller magnetics. The INTVCC pin has its own undervoltage disable (UVLO) set to 4V (typical) to protect the external FETs from excessive power dissipation caused by not being fully enhanced. If the INTVCC pin drops below the UVLO threshold, the GATE pin is forced to 0V, TG pin is pulled high and the soft-start pin will be reset. If the input voltage, VIN, will not exceed 7V, then the INTVCC pin should be connected to the input supply. Be aware that a small current (typically 10μA) loads the INTVCC in shutdown. If VIN is normally above, but occasionally drops below the INTVCC regulation voltage, then the minimum operating VIN is close to 6V. This value is determined by the dropout voltage of the linear regulator and the 4V INTVCC undervoltage lockout threshold mentioned above.

Programming the Turn-On and Turn-Off Thresholds with the EN/UVLO Pin

The falling UVLO value can be accurately set by the resistor divider. A small 3μA pull-down current is active when EN/UVLO is below the threshold. The purpose of this current is to allow the user to program the rising hysteresis. The following equations should be used to determine the values of the resistors:

\[ V_{IN(FALLING)} = 1.22 \cdot \frac{R_1 + R_2}{R_2} \]
\[ V_{IN(RISING)} = V_{IN(FALLING)} + 3\mu A \cdot R_1 \]

LED Current Programming

The LED current is programmed by placing an appropriate value current sense resistor R_LED between the ISP and ISN pins. Typically, sensing of the current should be done at the top of the LED string. If this option is not available, then the current may be sensed at the bottom of the string. The CTRL pin should be tied to a voltage higher than 1.2V to get the full-scale 250mV (typical) threshold across the sense resistor. The CTRL pin can also be used to dim the LED current to zero, although relative accuracy decreases with the decreasing voltage sense threshold. When the CTRL pin voltage is less than 1V, the LED current is:

\[ I_{LED} = \frac{V_{CTRL} - 100mV}{R_{LED} \cdot 4}, \ 0.1V < V_{CTRL} \leq 1V \]
\[ I_{LED} = 0, \ V_{CTRL} = 0V \]

When the CTRL pin voltage is between 1V and 1.2V, the LED current varies with CTRL, but departs from the previous equation by an increasing amount as the CTRL voltage increases. Ultimately above 1.2V, the LED current no
APPLICATIONS INFORMATION

Longer varies with CTRL. The typical $V_{(ISP-ISN)}$ threshold vs CTRL is listed in the Table 1.

Table 1. $V_{(ISP-ISN)}$ Threshold vs CTRL

<table>
<thead>
<tr>
<th>$V_{CTRL}$ (V)</th>
<th>$V_{(ISP-ISN)}$ (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>225</td>
</tr>
<tr>
<td>1.05</td>
<td>236</td>
</tr>
<tr>
<td>1.1</td>
<td>244.5</td>
</tr>
<tr>
<td>1.15</td>
<td>248.5</td>
</tr>
<tr>
<td>1.2</td>
<td>250</td>
</tr>
</tbody>
</table>

When CTRL is higher than 1.2V, the LED current is regulated to:

$$I_{LED} = \frac{250\text{mV}}{R_{LED}}$$

The CTRL pin should not be left open (tie to $V_{REF}$ if not used). The CTRL pin can also be used in conjunction with a thermistor to provide overtemperature protection for the LED load, or with a resistor divider to $V_{IN}$ to reduce output power and switching current when $V_{IN}$ is low. The presence of a time varying differential voltage signal (ripple) across ISP and ISN at the switching frequency is expected. The amplitude of this signal is increased by high LED load current, low switching frequency and/or a smaller value output filter capacitor.

Programming Output Voltage (Constant-Voltage Regulation) or Open LED/Overvoltage Threshold

The LT3796 has two voltage feedback pins, FB1 and FB2. Either one can be used for a boost or SEPIC application. The difference between these two pins is FB1 has a comparator that senses when FB1 exceeds $V_{FB} - 60\text{mV}$ (VMODE threshold) and asserts the VMODE output if $V_{(ISP-ISN)}$ is less than 25mV. This indicates that the output is in voltage regulation mode and not current regulation. FB2 does not have this extra comparator. The output voltage can be set by selecting the values of R3 and R4 (see Figure 2) according to the following equation:

$$V_{OUT} = 1.25 \cdot \frac{R_3 + R_4}{R_4}$$

For a boost type LED driver, set the resistor from the output to the FB1 pin such that the expected $V_{FB1}$ during normal operation does not exceed 1.15V. For an LED driver of buck mode or a buck-boost mode configuration, the FB voltage is typically level shifted to a signal with respect to GND as illustrated in Figure 3. The output can be expressed as:

$$V_{OUT} = 1.25 \cdot \frac{R_5}{R_8} \cdot \frac{R_6 + R_7}{R_6}$$
Applications Information

Open LED Detection

The LT3796 provides an open-collector status pin, VMODE, that pulls low when the FB1 pin is above 1.19V and V(ISP-ISN) is less than 25mV. If the open LED clamp voltage is programmed correctly using the resistor divider, then the FB1 pin should never exceed 1.15V when LEDs are connected, therefore, the only way for the FB1 pin to be within 60mV of the 1.25V regulation voltage is for an open LED event to have occurred.

LED Over Current Protection Feature

The ISP and ISN pins have a short-circuit protection feature independent of the LED current sense feature. This feature prevents the development of excessive switching currents and protects the power components. The short-circuit protection threshold (375mV, typ) is designed to be 50% higher than the default LED current sense threshold. Once the LED over current is detected, the GATE pin is driven to GND to stop switching, and TG pin is pulled high to disconnect the LED array from the power path.

A typical LED short-circuit protection scheme for boost or buck-boost mode converter is shown in Figure 4. The Schottky diode D2 should be put close to the drain of M2 on the board. It protects the LED+ node from swinging well below ground when being shorted to ground through a long cable. Usually, the internal protection loop takes about 1µs to respond. Including PNP helper Q1 is recommended to limit the transient short-circuit current.

With the PNP helper, the short-circuit current can be limited to 2A, whereas the short-circuit current can reach to 20A without the PNP helper as shown in Figure 5 and Figure 6 respectively. Refer to boost LED driver with output short-circuit protection and LED current monitor for the test schematic. Note that the impedance of the short-circuit cable affects the peak current.

![Figure 4. The Simplified LED Short-Circuit Protection Schematic for Boost/Buck-Boost Mode LED Driver](image)

![Figure 5. Short-circuit Current without PNP Helper](image)

![Figure 6. Short-circuit Current with PNP Helper](image)

![Figure 7. The Simplified LED Short-Circuit Protection Schematic for Buck Mode Converter](image)
APPLICATIONS INFORMATION

Similar to boost, Schottky diodes D2, D3 and PNP transistor Q1 are recommended to protect short-circuit event in the buck mode.

PWM Dimming Control for Brightness

There are two methods to control the LED current for dimming using the LT3796. One method uses the CTRL pin to adjust the current regulated in the LEDs. A second method uses the PWM pin to modulate the LED current between zero and full current to achieve a precisely programmed average current, without the possibility of color shift that occurs at low current in LEDs. To make PWM dimming more accurate, the switch demand current is stored on the VC node during the quiescent phase when PWM is low. This feature minimizes recovery time when the PWM signal goes high. To further improve the recovery time, a disconnect switch should be used in the LED current path to prevent the output capacitor from discharging during the PWM signal low phase. The minimum PWM on or off time depends on the choice of operating frequency through the RT input. For best current accuracy, the minimum PWM high time should be at least three switching cycles (3μs for fsw = 1MHz).

A low duty cycle PWM signal can cause excessive start-up times if it were allowed to interrupt the soft-start sequence. Therefore, once start-up is initiated by PWM > 1V, it will ignore a logical disable by the external PWM input signal. The device will continue to soft-start with switching and TG enabled until either the voltage at SS reaches the 1.0V level, or the output current reaches one-fourth of the full-scale current. At this point the device will begin following the dimming control as designated by PWM. If at any time an output overcurrent is detected, GATE and TG will be disabled even as SS continues to charge.

Programming the Switching Frequency

The RT frequency adjust pin allows the user to program the switching frequency from 100kHz to 1MHz to optimize efficiency/performance or external component size. Higher frequency operation yields smaller component size but increases switching losses and gate driving current, and may not allow sufficiently high or low duty cycle operation. Lower frequency operation gives better performance at the cost of larger external component size. For an appropriate RT resistor value see Table 2. An external resistor from the RT pin to GND is required—do not leave this pin open.

| Table 2. Typical Switching Frequency vs RT Value (1% Resistor) |
|------------------|------------------|
| fosc(kHz)        | RT(Ω)            |
| 1000             | 6.65             |
| 900              | 7.50             |
| 800              | 8.87             |
| 700              | 10.2             |
| 600              | 12.4             |
| 500              | 15.4             |
| 400              | 19.6             |
| 300              | 26.1             |
| 200              | 39.2             |
| 100              | 82.5             |

Frequency Synchronization

The LT3796 switching frequency can be synchronized to an external clock using the SYNC pin. For proper operation, the RT resistor should be chosen for a switching frequency 20% lower than the external clock frequency. The SYNC pin is disabled during the soft-start period. Observation of the following guidelines about the SYNC waveform will ensure proper operation of this feature. Driving SYNC with a 50% duty cycle waveform is always a good choice, otherwise, maintain the duty cycle between 20% and 60%. When using both PWM and SYNC features, the PWM signal rising edge must have the aligned rising edges to achieve the optimized high PWM dimming ratio. If the SYNC pin is not used, it should be connected to GND.

Duty Cycle Considerations

Switching duty cycle is a key variable defining converter operation, therefore, its limits must be considered when programming the switching frequency for a particular application. The fixed minimum on-time and minimum
off-time (see Figure 8) and the switching frequency define the minimum and maximum duty cycle of the switch, respectively. The following equations express the minimum/maximum duty cycle:

Min Duty Cycle = minimum on-time • switching frequency
Max Duty Cycle = 1 – minimum off-time • switching frequency

When calculating the operating limits, the typical values for on/off-time in the data sheet should be increased by at least 100ns to allow margin for PWM control latitude, GATE rise/fall times and SW node rise/fall times.

Setting Input Current Limit

The LT3796 has a standalone current sense amplifier. It can be used to limit the input current. As shown in Figure 9, the input current signal is converted to voltage output at CSOUT pin. When the CSOUT voltage exceeds FB2 regulation voltage, the GATE is pulled low, and the converter stops switching. The input current limit is calculated as follows:

\[ I_{IN} = 1.25 \times \frac{R_{IN1}}{R_{OUT} \times R_{SNS}} \]

For buck applications, filter components, \( R_{IN2(OPT)} \) and \( C_{OPT} \), are recommended to be placed close to LT3796 to suppress the substantial transient signal or noise at across CSN and CSP pins. For boost and buck-boost applications, \( R_{IN2(OPT)} \) and \( C_{OPT} \) are not required.

Thermal Considerations

The LT3796 is rated to a maximum input voltage of 100V. Careful attention must be paid to the internal power dissipation of the IC at higher input voltages to ensure that a junction temperature of 150°C is not exceeded. This junction limit is especially important when operating at high ambient temperatures. The majority of the power dissipation in the IC comes from the supply current needed to drive the gate capacitance of the external power N-channel MOSFET. This gate drive current can be calculated as:

\[ I_{GATE} = f_{SW} \times Q_{G} \]

A low \( Q_{G} \) power MOSFET should always be used when operating at high input voltages, and the switching frequency should also be chosen carefully to ensure that the IC does not exceed a safe junction temperature. The internal junction temperature, \( T_J \) of the IC can be estimated by:

\[ T_J = T_A + [I_{IN} \times (I_Q + f_{SW} \times Q_G) \times \theta_{JA}] \]

where \( T_A \) is the ambient temperature, \( I_Q \) is the \( V_{IN} \) operating current of the part (2.5mA typical) and \( \theta_{JA} \) is the package thermal impedance (30°C/W for the TSSOP package). For example, an application with \( T_A(\text{MAX}) = 85°C, V_{IN(\text{MAX})} = 60V, f_{SW} = 400kHz, \) and having a N-channel MOSFET with
APPLICATIONS INFORMATION

Q_S = 20nC, the maximum IC junction temperature will be approximately:

\[ T_J = 85°C + [60V \cdot (2.5mA + 400kHz \cdot 20nC) \cdot 30°C/W] \approx 104°C \]

The exposed pad on the bottom of the package must be soldered to a ground plane. This ground should then be connected to an internal copper ground plane with thermal vias placed directly under the package to spread out the heat dissipated by the IC.

It is best if the copper plane is extended on either the top or bottom layer of the PCB to have the maximum exposure to air. Internal ground layers do not dissipate thermals as much as top and bottom layer copper does. See recommended layout as an example.

Input Capacitor Selection

The input capacitor supplies the transient input current for the power inductor of the converter and must be placed and sized according to the transient current requirements. The switching frequency, output current and tolerable input voltage ripple are key inputs to estimating the capacitor value. An X7R type ceramic capacitor is usually the best choice since it has the least variation with temperature and DC bias. Typically, boost and SEPIC converters require a lower value capacitor than a buck mode converter. Assuming that a 100mV input voltage ripple is acceptable, the required capacitor value for a boost converter can be estimated as follows (T_{SW} = 1/\text{f_{OSC}}):

\[ C_{IN} (\mu F) = I_{LED} (A) \cdot \frac{V_{LED}}{V_{IN}} \cdot T_{SW} (\mu s) \cdot \frac{1 \mu F}{A \cdot \mu s \cdot 2.8} \]

Therefore, a 2.2\mu F capacitor is an appropriate selection for a 400kHz boost regulator with 12V input, 48V output and 500mA load.

With the same V_{IN} voltage ripple of less than 100mV, the input capacitor for a buck converter can be estimated as follows:

\[ C_{IN} (\mu F) = I_{LED} (A) \cdot \frac{V_{LED}}{V_{IN}} \cdot \frac{V_{IN} - V_{LED}}{V_{IN}^2} \cdot T_{SW} (\mu s) \cdot \frac{10 \mu F}{A \cdot \mu s} \]

A 10\mu F input capacitor is an appropriate selection for a 400kHz buck mode converter with 24V input, 12V output and 1A load.

In the buck mode configuration, the input capacitor has large pulsed currents due to the current returned through the Schottky diode when the switch is off. It is important to place the capacitor as close as possible to the Schottky diode and to the GND return of the switch (i.e., the sense resistor). It is also important to consider the ripple current rating of the capacitor. For best reliability, this capacitor should have low ESR and ESL and have an adequate ripple current rating. The RMS input current for a buck mode LED driver is:

\[ I_{IN (RMS)} = I_{LED} \cdot \sqrt{(1-D)D} \cdot \frac{V_{LED}}{V_{IN}} \]

where D is the switch duty cycle.

Output Capacitor Selection

The selection of the output capacitor depends on the load and converter configuration, i.e., step-up or step-down and the operating frequency. For LED applications, the equivalent resistance of the LED is typically low and the output filter capacitor should be sized to attenuate the current ripple. Use of an X7R type ceramic capacitor is recommended.

To achieve the same LED ripple current, the required filter capacitor is larger in the boost and buck-boost mode applications than that in the buck mode applications. Lower operating frequencies will require proportionately higher capacitor values.

Table 3. Recommended Ceramic Capacitor Manufacturers

<table>
<thead>
<tr>
<th>MANUFACTURER</th>
<th>WEB</th>
</tr>
</thead>
<tbody>
<tr>
<td>TDK</td>
<td><a href="http://www.tdk.com">www.tdk.com</a></td>
</tr>
<tr>
<td>Kemet</td>
<td><a href="http://www.kemet.com">www.kemet.com</a></td>
</tr>
<tr>
<td>Murata</td>
<td><a href="http://www.murata.com">www.murata.com</a></td>
</tr>
<tr>
<td>Taiyo Yuden</td>
<td><a href="http://www.t-yuden.com">www.t-yuden.com</a></td>
</tr>
<tr>
<td>AVX</td>
<td><a href="http://www.avx.com">www.avx.com</a></td>
</tr>
</tbody>
</table>
Applications Information

Power MOSFET Selection
For applications operating at high input or output voltages, the power N-channel MOSFET switch is typically chosen for drain voltage V_DS rating and low gate charge Q_G. Consideration of switch on-resistance, R_DS(ON), is usually secondary because switching losses dominate power loss. The INTVCC regulator on the LT3796 has a fixed current limit to protect the IC from excessive power dissipation at high VIN, so the MOSFET should be chosen so that the product of Q_G at 7.7V and switching frequency does not exceed the INTVCC current limit. For driving LEDs be careful to choose a switch with a V_DS rating that exceeds the threshold set by the FB pin in case of an open load fault. Several MOSFET vendors are listed in Table 4. The MOSFETs used in the application circuits in this data sheet have been found to work well with the LT3796. Consult factory applications for other recommended MOSFETs.

Table 4. MOSFET Manufacturers

<table>
<thead>
<tr>
<th>VENDOR</th>
<th>WEB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vishay Siliconix</td>
<td><a href="http://www.vishay.com">www.vishay.com</a></td>
</tr>
<tr>
<td>Fairchild</td>
<td><a href="http://www.fairchildsemi.com">www.fairchildsemi.com</a></td>
</tr>
<tr>
<td>International Rectifier</td>
<td><a href="http://www.irf.com">www.irf.com</a></td>
</tr>
<tr>
<td>Infineon</td>
<td><a href="http://www.infineon.com">www.infineon.com</a></td>
</tr>
</tbody>
</table>

High Side PMOS Disconnect Switch Selection
A high side PMOS disconnect switch with a minimum V_TH of –1V to –2V is recommended in most LT3796 applications to optimize or maximize the PWM dimming ratio and protect the LED string from excessive heating during fault conditions as well. The PMOS disconnect switch is typically selected for drain-source voltage V_DS and continuous drain current I_D. For proper operations, V_DS rating must exceed the open LED regulation voltage set by the FB1 pin, and I_D rating should be above I_LED.

Schottky Rectifier Selection
The power Schottky diode conducts current during the interval when the switch is turned off. Select a diode rated for the maximum SW voltage. If using the PWM feature for dimming, it is important to consider diode leakage, which increases with the temperature, from the output during the PWM low interval. Therefore, choose the Schottky diode with sufficiently low leakage current. Table 5 has some recommended component vendors.

Table 5. Schottky Rectifier Manufacturers

<table>
<thead>
<tr>
<th>VENDOR</th>
<th>WEB</th>
</tr>
</thead>
<tbody>
<tr>
<td>On Semiconductor</td>
<td><a href="http://www.onsemi.com">www.onsemi.com</a></td>
</tr>
<tr>
<td>Diodes, Inc</td>
<td><a href="http://www.diodes.com">www.diodes.com</a></td>
</tr>
<tr>
<td>Central Semiconductor</td>
<td><a href="http://www.centralsemi.com">www.centralsemi.com</a></td>
</tr>
<tr>
<td>Rohm Semiconductor</td>
<td><a href="http://www.rohm.com">www.rohm.com</a></td>
</tr>
</tbody>
</table>

Sense Resistor Selection
The resistor, R_SENSE, between the source of the external N-channel MOSFET and GND should be selected to provide adequate switch current to drive the application without exceeding the 113mV (typical) current limit threshold on the SENSE pin of LT3796. For buck mode applications, select a resistor that gives a switch current at least 30% greater than the required LED current. For buck mode, select a resistor according to:

\[ R_{SENSE(BUCK)} \leq \frac{0.07V}{I_{LED}} \]

For buck-boost mode, select a resistor according to:

\[ R_{SENSE(BUCK-BOOST)} \leq \frac{V_{IN} \times 0.07V}{(V_{IN} + V_{LED})I_{LED}} \]

For boost, select a resistor according to:

\[ R_{SENSE(BOOST)} \leq \frac{V_{IN} \times 0.07V}{V_{LED} \times I_{LED}} \]

The placement of R_SENSE should be close to the source of the NMOS FET and GND of the LT3796. The SENSE input to LT3796 should be a Kelvin connection to the positive terminal of R_SENSE.

70mV is used in the equations above to give some margin below the 113mV (typical) sense current limit threshold.
APPLICATIONS INFORMATION

Inductor Selection

The inductor used with the LT3796 should have a saturation current rating appropriate to the maximum switch current selected with the RSENSE resistor. Choose an inductor value based on operating frequency, input and output voltage to provide a current mode signal on SENSE of approximately 20mV magnitude. The following equations are useful to estimate the inductor value (T\text{SW} = 1/f\text{OSC}):

\[
L_{\text{BUCK}} = \frac{T_{\text{SW}} \cdot R_{\text{SENSE}} \cdot V_{\text{LED}} (V_{\text{IN}} - V_{\text{LED}})}{V_{\text{IN}} \cdot 0.02V}
\]

\[
L_{\text{BUCK, BOOST}} = \frac{T_{\text{SW}} \cdot R_{\text{SENSE}} \cdot V_{\text{LED}} \cdot V_{\text{IN}}}{(V_{\text{LED}} + V_{\text{IN}}) \cdot 0.02V}
\]

\[
L_{\text{BOOST}} = \frac{T_{\text{SW}} \cdot R_{\text{SENSE}} \cdot V_{\text{IN}} (V_{\text{LED}} - V_{\text{IN}})}{V_{\text{LED}} \cdot 0.02V}
\]

Table 6 provides some recommended inductor vendors.

<table>
<thead>
<tr>
<th>VENDOR</th>
<th>WEB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sumida</td>
<td><a href="http://www.sumida.com">www.sumida.com</a></td>
</tr>
<tr>
<td>Würth Elektronik</td>
<td><a href="http://www.we-online.com">www.we-online.com</a></td>
</tr>
<tr>
<td>Coiltronics</td>
<td><a href="http://www.cooperet.com">www.cooperet.com</a></td>
</tr>
<tr>
<td>Vishay</td>
<td><a href="http://www.vishay.com">www.vishay.com</a></td>
</tr>
<tr>
<td>Coilcraft</td>
<td><a href="http://www.coilcraft.com">www.coilcraft.com</a></td>
</tr>
</tbody>
</table>

Loop Compensation

The LT3796 uses an internal transconductance error amplifier whose V_C output compensates the control loop. The external inductor, output capacitor and the compensation resistor and capacitor determine the loop stability. The inductor and output capacitor are chosen based on performance, size and cost. The compensation resistor and capacitor at V_C are selected to optimize control loop response and stability. For typical LED applications, a 22nF compensation capacitor at V_C is adequate, and a series resistor should always be used to increase the slew rate on the V_C pin to maintain tighter regulation of LED current during fast transients on the input supply to the converter.

Soft-Start Capacitor Selection

For many applications, it is important to minimize the inrush current at start-up. The built-in soft-start circuit significantly reduces the start-up current spike and output voltage overshoot. The soft-start interval is set by the soft-start capacitor selection according to the equation:

\[
T_{SS} = C_{SS} \cdot \frac{2V}{28\mu A}
\]

A typical value for the soft-start capacitor is 0.1\mu F. The soft-start pin reduces the oscillator frequency and the maximum current in the switch. Soft-start also operates as fault protection, which forces the converter into hiccup or latchoff mode. Detailed information is provided in the Fault Protection: Hiccup Mode and Latchoff Mode section.

Fault Protection: Hiccup Mode and Latchoff Mode

If an LED overcurrent condition, INTVCC undervoltage, or thermal limit happens, an open-drain pull-down on FAULT asserts. The TG pin is pulled high to disconnect the LED array from the power path, and the GATE pin is driven low. If the soft-start pin is charging and still below 1.7V, then it will continue to do so with a 28\mu A source. Once above 1.7V, the pull-up source is disabled and a 2.8\mu A pull-down is activated. While the SS pin is discharging, the GATE is forced low. When SS pin is discharged below 0.2V, a new cycle is initiated. This is referred as hiccup mode operation. If the fault still exists when SS crosses below 0.2V, then a full SS charge/discharge cycle has to complete before switching is enabled and the FAULT flag is deasserted.

If a resistor is placed between V_REF pin and SS pin to hold SS pin higher than 0.2V during a fault, then the LT3796 will enter latchoff mode with GATE pin low, TG pin high and FAULT pin low. To exit latchoff mode, the EN/UVLO pin must be toggled low to high.
Board Layout

The high speed operation of the LT3796 demands careful attention to board layout and component placement. The exposed pad of the package is the GND terminal of the IC and is also important for thermal management of the IC. It is crucial to achieve a good electrical and thermal contact between the exposed pad and the ground plane of the board. To reduce electromagnetic interference (EMI), it is important to minimize the area of the high dV/dt switching node between the inductor, switch drain and anode of the Schottky rectifier. Use a ground plane under the switching node to eliminate interplane coupling to sensitive signals. The lengths of the high dI/dt traces: 1) from the switch node through the switch and sense resistor to GND, and 2) from the switch node through the Schottky rectifier and filter capacitor to GND should be minimized. The ground points of these two switching current traces should come to a common point then connect to the ground plane under the LT3796. Likewise, the ground terminal of the bypass capacitor for the INTVCC regulator should be placed near the GND of the switching path. Typically, this requirement results in the external switch being closest to the IC, along with the INTVCC bypass capacitor. The ground for the compensation network and other DC control signals should be star connected to the underside of the IC. Do not extensively route high impedance signals such as FB1, FB2, RT and VC, as they may pick up switching noise. Since there is a small variable DC input bias current to the ISN and ISP inputs, resistance in series with these pins should be minimized to avoid creating an offset in the current sense threshold. Likewise, minimize resistance in series with the SENSE input to avoid changes (most likely reduction) to the switch current limit threshold.

Figure 10 is a suggested two sided layout for a boost converter. Note that the 4-layer layout is recommended for best performance. Please contact the factory for the reference layout design.
APPLICATIONS INFORMATION

Figure 10. Boost Converter Suggested Layout

COMPONENT DESIGNATIONS REFER TO BOOST LED DRIVER WITH OUTPUT SHORT CIRCUIT PROTECTION AND LED CURRENT MONITOR
TYPICAL APPLICATIONS

Boost LED Driver with Output Short Circuit Protection and LED Current Monitor

Fault (Short LED) Protection without R11: Hiccup Mode

Fault (Short LED) Protection with R11: Latchoff Mode
TYPICAL APPLICATIONS

Buck LED Driver with Open LED Flag and LED Current Reporting

Efficiency vs $V_{IN}$

M1: VISHAY SILICONIX Si7454DP
M2: VISHAY SILICONIX Si7113DN
D1: DIODES INC PDS3100
L1: COILTRONICS HC9-220
LED: CREE XLAMP XM-L

M1: VISHAY SILICONIX Si7454DP
M2: VISHAY SILICONIX Si7113DN
D1: DIODES INC PDS3100
L1: COILTRONICS HC9-220
LED: CREE XLAMP XM-L

Efficiency vs $V_{IN}$
TYPICAL APPLICATIONS

SEPIC LED Driver Using FB2 for Input Overvoltage Protection

Efficiency vs V_IN

Optional input current reporting

Optional input current reporting

M1: VISHAY SILICONIX Si7456DP
M2: ZETEX ZXMP6A13F
L1: COILTRONICS DRQ127-330
D1: DIODES INC PDS5100
LED: CREE XLAMP XR-E
SEPIC Sealed Lead Acid (SLA) Battery Charger

VCHARGE, VFLOAT vs Temperature

-40  -30  -20  -10   0    10    20    30    40    50    60    70    80
  12.5  13.0  13.5  14.0  14.5  15.0  15.5  16.0  16.5  17.0  17.5

VCHARGE = 14.6V
VFLOAT = 13.5V
AT 25°C

M1: VISHAY SILICONIX SI7456DP
M2: VISHAY SUD19P06-60-E3
M3: ZETEX ZXM61N03F
L1: COILCRAFT MSS1550-333
D1: ON SEMI MBRS260T3G
D2: CENTRAL SEMI CMDZ15L
R11: MURATA NCP18XH103F03RB

10nF
0.1µF
2.2µF
4.7µF
10µF
0.1µF
100µF
10k
100k
80k
2k
20k
49.9k
49.9k
19.6k
400kHz
400kHz
400µA
400µA
100V (TRANSIENT)

OPTIONAL INPUT CURRENT REPORTING

M1: VISHAY SILICONIX SI7456DP
M2: VISHAY SUD19P06-60-E3
M3: ZETEX ZXM61N03F
L1: COILCRAFT MSS1550-333
D1: ON SEMI MBRS260T3G
D2: CENTRAL SEMI CMDZ15L
R11: MURATA NCP18XH103F03RB
**TYPICAL APPLICATIONS**

**28V\(_{\text{IN}}\) to 28V SuperCap Charger with Input Current Limit and Charge Done Flag**

**Input and Output Current vs Output Voltage**

- **VIN**: 28V
- **C1**: 10µF
- **C2**: 4.7µF
- **C6**: 10µF
- **R1**: 20k
- **L1**: 33µH
- **R2**: 120k
- **R3**: 47k
- **R4**: 30.1k
- **R5**: 1M
- **R6**: 100k
- **R7**: 100k
- **L1A**: 150mΩ
- **R8**: 536k
- **R9**: 24.9k
- **L1B**: 150mΩ
- **VOUT**: 0V to 28V
- **CSP**: VSVIN
- **CSN**: CSOUT
- **CTRL**: PWM
- **SYNC**: VCVREF
- **R1**
- **R2**
- **R3**
- **R4**
- **R5**
- **R6**
- **R7**
- **R8**
- **R9**
- **L1**
- **L1A**
- **L1B**
- **D1**: ON SEMI MBRS260T3G
- **M1**: VISHAY SILICONIX Si7850
- **Q1**: ZETEX FMMT591A
- **SS**: EN/UVLO
- **ISMON**: ISN
- **SYNC**: FB2
- **CSOUT**: FB1
- **CTRL**: INTVCC
- **VREF**: GND
- **RT**: 19.6k
- **400kHz
- **GATE**: INTVCC

**Components Specified**
- L1: COILCRAFT MSD1260-333
- D1: ON SEMI MBR5260T3G
- M1: VISHAY SILICONIX Si7850
- Q1: ZETEX FMMT591A

**Supercap Specifications**
- M1: 1.67A MAX

**Input Current Reporting and Limit**
- L1A: 33µH
- L1B: 150mΩ

**Output Current Limit**
- VOUT: 0V TO 28V

**Charge Done Flag**
- CHGDONE

**Fault**
- FAULT

**Voltage References**
- VREF

**Ground**
- GND

**Sensors**
- RT

**Frequency**
- 400kHz

**Supercap**
- SUPERCAP

**Miscellaneous**
- C5: 0.1µF
- C7: 0.1µF
- R10: 499k
- C4: 0.1µF
- C3: 0.1µF
- C2: 4.7µF
- C6: 10µF
- C1: 10µF
- C5: 0.1µF
- C4: 0.1µF
- C2: 4.7µF
- C1: 10µF

**Linearity**
- VIN vs VOUT

**Power Calculations**
- Input Power: VIN x IIN
- Output Power: VOUT x IOUT

**Efficiency**
- Efficiency = (Output Power / Input Power) x 100%

**Performance Metrics**
- Voltage Ripple
- Current Ripple
- Temperature
- Noise

**Reference Sources**
- [Linear Technology](https://www.linear.com)
**Typical Applications**

SEPIC Converter with $R_{\text{Wire}}$ Compensation and Output Current Limit

Line Impedance Compensation

Load Step Response
TYPICAL APPLICATIONS

Solar Panel Driven SLA Battery Charger with Maximum Power Point Tracking

WÜRTH SOLAR PANEL
V_{OC} = 37.5V
V_{MPP} = 28V

LT3796

Vin (V)
0.2
0.4
0.6
0.8
1.0

I_{CHARGE} (A)

20 25 30 35 40

V_{IN} (V)

I_{CHARGE} vs V_{IN}

M1: VISHAY SILICONIX S7456DP
M2: VISHAY SJU18P06-60-E3
M3: ZETEX ZXN61N03F
L1: COILCRAFT MS1260-333
D1: ON SEMI MBRS260T3G
D2: CENTRAL SEMI CMDZ15L
R9: MURATA NCP18XH103F03RB

VREF
ISMON
SYNC
GATE
CTRL
CSOUT
FB2
PWM
V_{IN}

C6 2.2µF 100V
L1A 33µH
C5 4.7µF
R7 49.9k
C6 0.1µF

V_{MPP} = 28V

3796f
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev I)
Exposed Pad Variation EB

Recommended Solder Pad Layout

NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
   *DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

Exposed Pad Heat Sink on Bottom of Package

MILLIMETERS (INCHES) *

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.
**TYPICAL APPLICATION**

Buck-Boost Mode LED Driver with Open LED Clamp and Output Voltage Limit

**Efficiency vs V_IN**

<table>
<thead>
<tr>
<th>V_IN (V)</th>
<th>EFFICIENCY (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>95</td>
</tr>
<tr>
<td>10</td>
<td>90</td>
</tr>
<tr>
<td>15</td>
<td>85</td>
</tr>
<tr>
<td>20</td>
<td>80</td>
</tr>
<tr>
<td>25</td>
<td>75</td>
</tr>
<tr>
<td>30</td>
<td>70</td>
</tr>
<tr>
<td>35</td>
<td>65</td>
</tr>
<tr>
<td>40</td>
<td>60</td>
</tr>
<tr>
<td>45</td>
<td>55</td>
</tr>
<tr>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>55</td>
<td>45</td>
</tr>
<tr>
<td>60</td>
<td>40</td>
</tr>
</tbody>
</table>

**RELATED PARTS**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT3791</td>
<td>60V Synchronous Buck-Boost 1MHz LED Controller</td>
<td>V_IN: 4.7V to 60V, V_OUT Range: 0V to 60V, True Color PWM, Analog = 100:1, ISD &lt; 1µA, TSSOP-38E Package</td>
</tr>
<tr>
<td>LT3755/LT3755-1 LT3755-2</td>
<td>High Side 60V, 1MHz LED Controller with True Color 3,000:1 PWM Dimming</td>
<td>V_IN: 4.5V to 40V, V_OUT Range: 5V to 60V, True Color PWM, Analog = 3000:1, ISD &lt; 1µA, 3mm × 3mm QFN-16, MSOP-16E Packages</td>
</tr>
<tr>
<td>LT3756/LT3756-1 LT3756-2</td>
<td>High Side 100V, 1MHz LED Controller with True Color 3,000:1 PWM Dimming</td>
<td>V_IN: 6V to 100V, V_OUT Range: 5V to 100V, True Color PWM, Analog = 3000:1, ISD &lt; 1µA, 3mm × 3mm QFN-16, MSOP-16E Packages</td>
</tr>
<tr>
<td>LT3743</td>
<td>Synchronous Step-Down 20A LED Driver with Three-State LED Current Control</td>
<td>V_IN: 5.5V to 36V, V_OUT Range: 5.5V to 35V, True Color PWM, Analog = 3000:1, ISD &lt; 1µA, 4mm × 5mm QFN-28, TSSOP-28E Packages</td>
</tr>
<tr>
<td>LTC3780</td>
<td>High Efficiency, Synchronous, 4-Switch Buck-Boost Controller</td>
<td>V_IN: 4V to 36V, V_OUT Range: 0.8V to 30V, ISD &lt; 55µA, SSOP-24, QFN-32 Packages</td>
</tr>
<tr>
<td>LTC3789</td>
<td>High Efficiency, Synchronous, 4-Switch Buck-Boost Controller</td>
<td>V_IN: 4V to 36V, V_OUT Range: 0.8V to 38V, ISD &lt; 40mA, 4mm × 5mm QFN-28, SSOP-28 Packages</td>
</tr>
<tr>
<td>LT3517</td>
<td>1.3A, 2.5MHz High Current LED Driver with 3,000:1 Dimming</td>
<td>V_IN: 3V to 30V, True Color PWM, Analog = 3000:1, ISD &lt; 1µA, 4mm × 4mm QFN-16 Package</td>
</tr>
<tr>
<td>LT3518</td>
<td>2.3A, 2.5MHz High Current LED Driver with 3,000:1 Dimming</td>
<td>V_IN: 3V to 30V, True Color PWM, Analog = 3000:1, ISD &lt; 1µA, 4mm × 4mm QFN-16 Package</td>
</tr>
<tr>
<td>LT3474/LT3474-1</td>
<td>36V, 1A (ILED), 2MHz, Step-Down LED Driver</td>
<td>V_IN: 4V to 36V, V_OUT Range = 13.5V, True Color PWM = 400:1, ISD &lt; 1µA, TSSOP-16E Package</td>
</tr>
<tr>
<td>LT3475/LT3475-1</td>
<td>Dual 1.5A (ILED), 36V, 2MHz, Step-Down LED Driver</td>
<td>V_IN: 4V to 36V, V_OUT Range = 13.5V, True Color PWM, Analog = 3000:1, ISD &lt; 1µA, TSSOP-20E Package</td>
</tr>
</tbody>
</table>