Projet 5 - K3501 / Onduleur 12V DC - 220V AC.

Projet : PROJETS-IUT1

Info : kit Velleman, [DATA012].

Révision : 24 janvier 2000

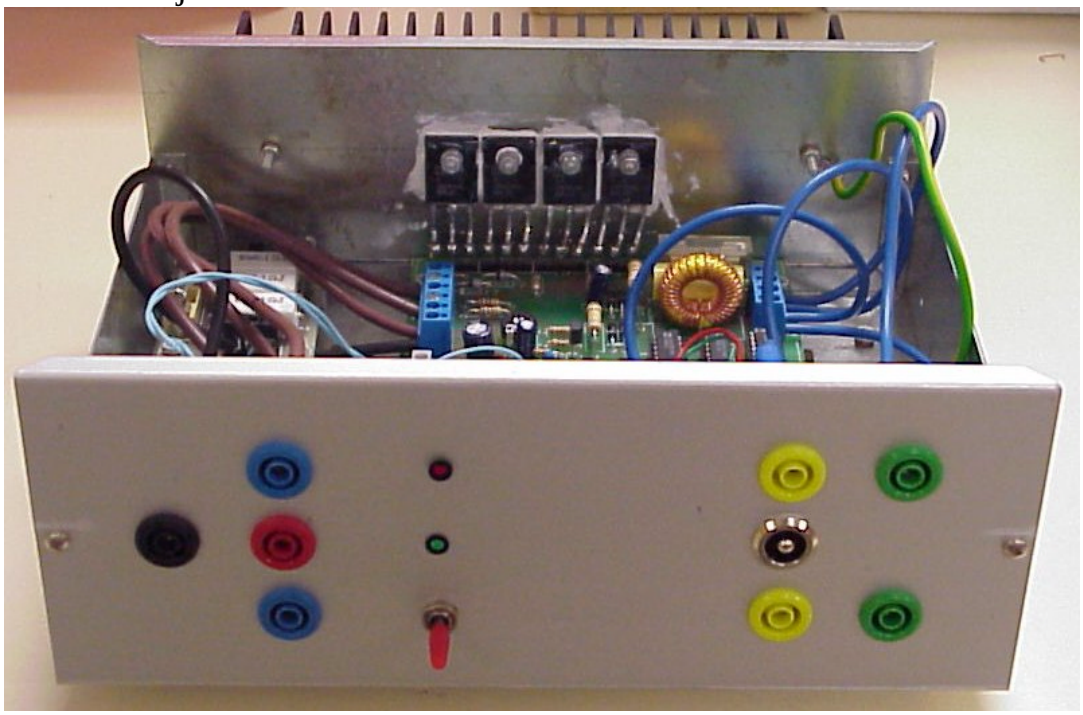


Figure 5.1. Face avant (images-maquettes\onduleur2.jpg).

5.1 Liste des documents

- Liste des composants.
- Schéma électronique.
- Implantation des composants.
- Circuit imprimé coté cuivre.
- Documentation des composants
- Recherche des montages équivalents.

5.2 Documentation des composants

IRFP140 31A, 100V, 0.070 Ohm, N-Channel Power MOSFET, July 1999.

HCF4011B QUAD 2 INPUT HCC/HCF 4011B.

MC14013B Dual D-type flip-flop.

HEF4060B January 1995, MSI 14-stage ripple-carry binary counter/divider and oscillator.

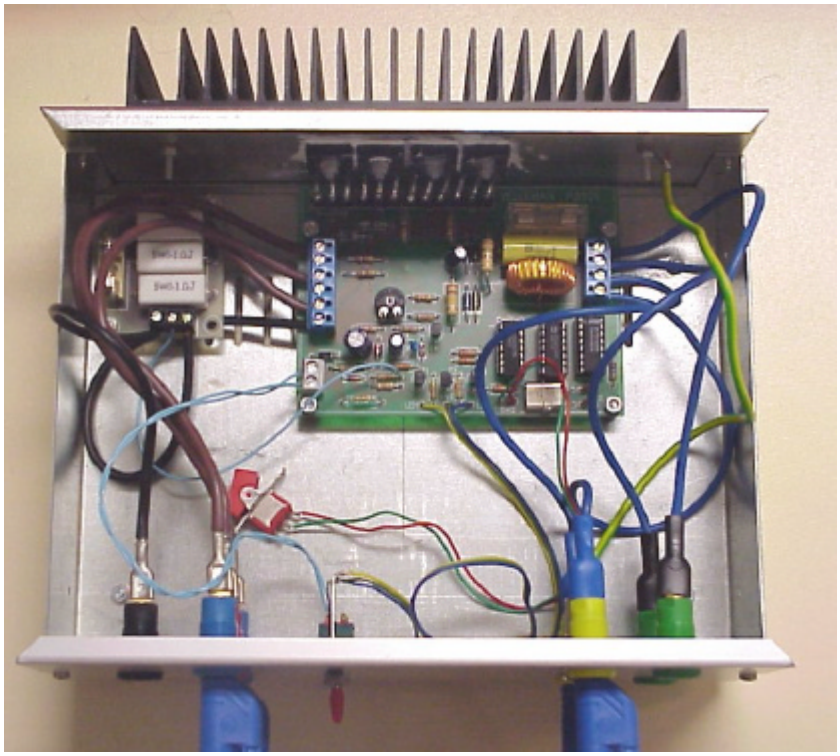


Figure 5.2. Câblage du montage (images-maquettes\onduleur1.jpg).

5.3 Recherche des montages équivalents

[DATA011] K3501, *Convertisseur 12V ou 24V DC en 220V AC*, Kit Velleman.

[99ART098] R. RATEAU, *Convertisseur 12V/220V 50 Hz - 220VA*, Radio Plans - Electronique Loisirs N° 423, pp. 43-52.

[DATA021] G. ISABEL, *Un convertisseur 12V/200V - 250VA*, Electronique Pratique, no. 186, pp. 39-44.

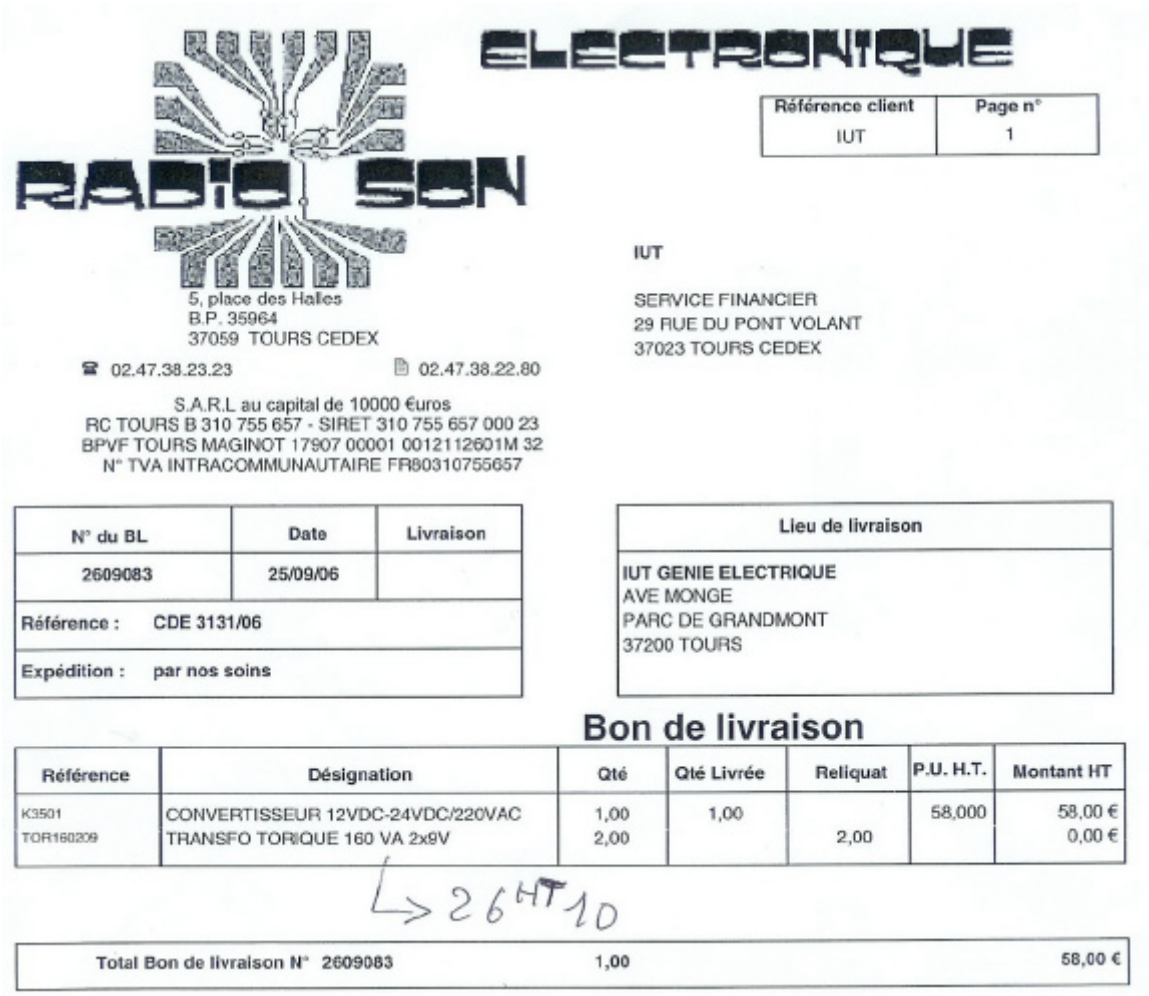
[DATA022] Réalisation flash, *Convertisseur 12V/200V - 30 VA*, Le haut-parleur hors série, pp. 45-47.

[DATA068] G. LAVERGNE, J. ROULLET, *Onduleur à point milieux 12V/220V*, projet IUT GEII, mars 1999.

[DATA014] E. AYMERIAL, N. MOUKHLISS, *Onduleur de secours 12V --> 220V 50 Hz*, projet IUT GEII TOURS, mars 2000.

[DATA016] M. CHI, R. CUZON, *Onduleur de secours 12V --> 220V 50 Hz*, projet IUT GEII TOURS, mars 2000, 60 pages.

5.4 Facture 2006 Radioson



RADIO SON ELECTRONIQUE

Référence client	Page n°
IUT	1

5, place des Halles
B.P. 35964
37059 TOURS CEDEX

☎ 02.47.38.23.23 02.47.38.22.80

S.A.R.L au capital de 10000 €uros
RC TOURS B 310 755 657 - SIRET 310 755 657 000 23
BPVF TOURS MAGINOT 17907 00001 0012112601M 32
N° TVA INTRACOMMUNAUTAIRE FR80310755657

IUT

SERVICE FINANCIER
29 RUE DU PONT VOLANT
37023 TOURS CEDEX

N° du BL	Date	Livraison
2609083	25/09/06	
Référence : CDE 3131/06		
Expédition : par nos soins		

Lieu de livraison
IUT GENIE ELECTRIQUE AVE MONGE PARC DE GRANDMONT 37200 TOURS

Bon de livraison

Référence	Désignation	Qté	Qté Livrée	Reliquat	P.U. H.T.	Montant HT
K3501	CONVERTISSEUR 12VDC-24VDC/220VAC	1,00	1,00		58,000	58,00 €
TOR160209	TRANSFO TORIQUE 160 VA 2x9V	2,00		2,00		0,00 €

↳ 26 HT 10

Total Bon de livraison N° 2609083	1,00	58,00 €

Figure 5.3. Commande Radioson 2006 (images-maquettes\K3501-Radioson-2006.jpg).

Data Sheet July 1999 File Number 2086.3

31A, 100V, 0.077 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17421.

Ordering Information

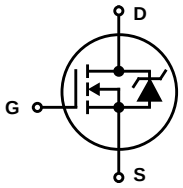
PART NUMBER	PACKAGE	BRAND
IRFP140	TO-247	IRFP140

NOTE: When ordering, include the entire part number.

Features

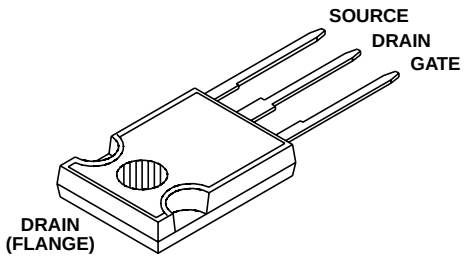
- 31A, 100V
- $r_{DS(ON)} = 0.077\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

JEDEC STYLE TO-247



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

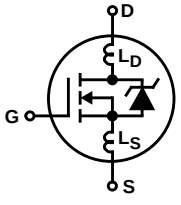
		IRFP140	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	100	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	100	V
Continuous Drain Current	I_D	31	A
$T_C = 100^oC$	I_D	22	A
Pulsed Drain Current (Note 3)	I_{DM}	120	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	180	W
Linear Derating Factor		1.2	$W/^oC$
Single Pulse Avalanche Energy Rating (Note 4)	E_{AS}	100	mJ
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

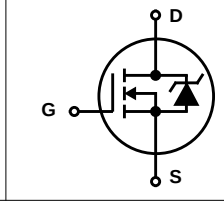
NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA (Figure 10)		100	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA		2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V		-	-	25	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_J = 125^oC$		-	-	250	μA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, V_{GS} = 10V		31	-	-	A
Gate to Source Leakage	I_{GSS}	V_{GS} = ±20V		-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 19A (Figures 8, 9)		-	0.055	0.077	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq 50V$, I_D = 19A (Figure 12)		9.3	14	-	S
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, $I_D \approx$ 28A, R_{GS} = 9.1Ω, R_L = 1.7Ω, V_{GS} = 10V MOSFET Switching Times are Essentially Independent of Operating Temperature		-	15	23	ns
Rise Time	t_r			-	72	110	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	40	60	ns
Fall Time	t_f			-	50	75	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	V_{GS} = 10V, $I_D \approx$ 27A, V_{DS} = 0.8 x Rated BV_{DSS}, $I_{G(REF)}$ = 1.5mA (Figure 14) Gate Charge is Essentially Independent of Operating Temperature		-	38	59	nC
Gate to Source Charge	Q_{gs}			-	10	-	nC
Gate to Drain "Miller" Charge	Q_{gd}			-	21	-	nC
Input Capacitance	C_{ISS}	V_{GS} = 0V, $V_{DS} \approx$ 25V, f = 1.0MHz (Figure 11)		-	1275	-	pF
Output Capacitance	C_{OSS}			-	550	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	160	-	pF
Internal Drain Inductance	L_D	Measured between the Contact Screw on Header that is Closer to Source and Gate Pins and Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the Source Lead, 6mm (0.25in) From Header to Source Bonding Pad		-	12.5	-	nH
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	0.83	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation		-	-	30	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode		-	-	31	A
Pulse Source to Drain Current (Note 3)	I_{SDM}			-	-	120	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^oC$, $I_{SD} = 31A$, $V_{GS} = 0V$ (Figure 13)		-	-	2.5	V
Reverse Recovery Time	t_{rr}	$T_J = 25^oC$, $I_{SD} = 28A$, $dI_{SD}/dt = 100A/\mu s$		70	150	300	ns
Reverse Recovered Charge	Q_{RR}	$T_J = 25^oC$, $I_{SD} = 28A$, $dI_{SD}/dt = 100A/\mu s$		0.44	0.91	1.9	µC

NOTES:

2. Pulse test: pulse width ≤ 300µs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. $V_{DD} = 25V$, starting $T_J = 25^oC$, L = 160µH, $R_G = 50\Omega$, peak $I_{AS} = 31A$.

Typical Performance Curves Unless Otherwise Specified

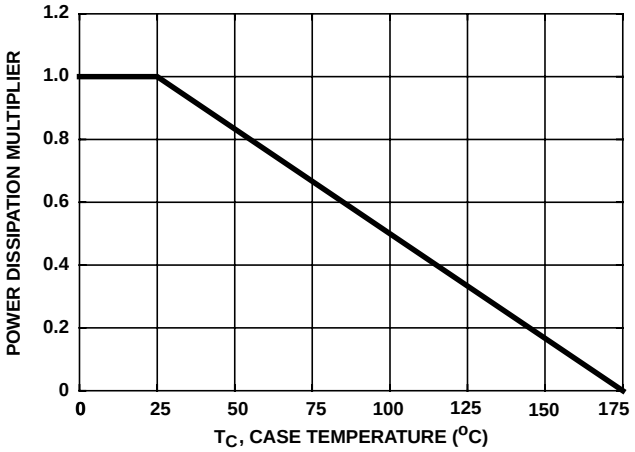


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

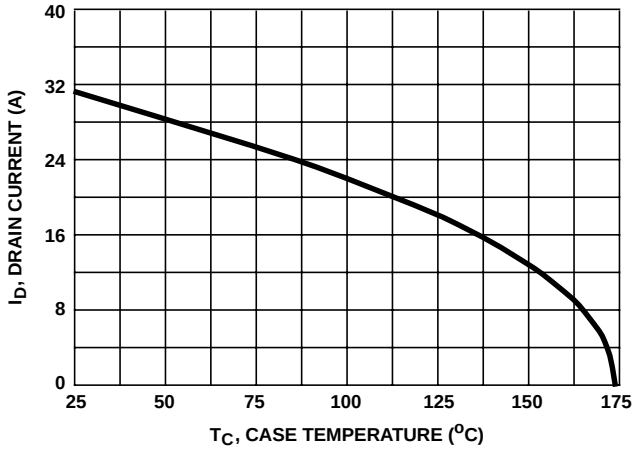


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

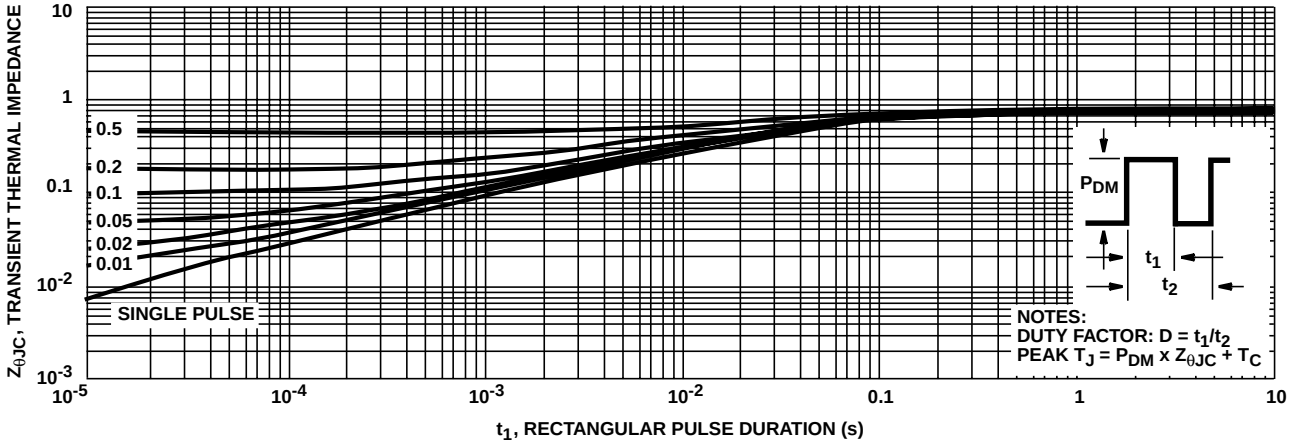


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves Unless Otherwise Specified (Continued)

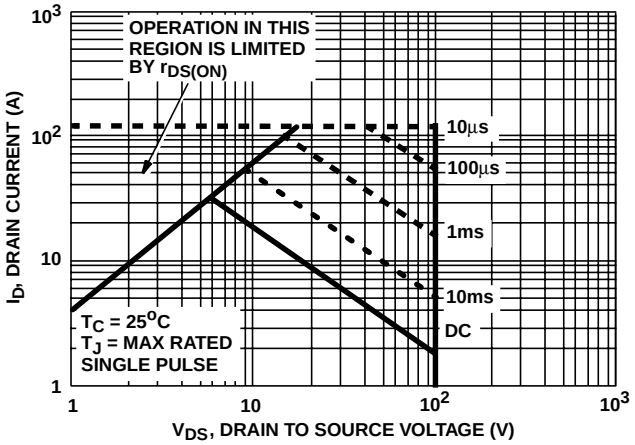


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

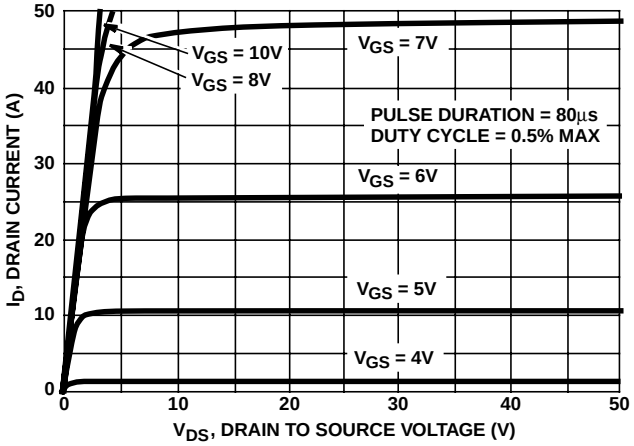


FIGURE 5. OUTPUT CHARACTERISTICS

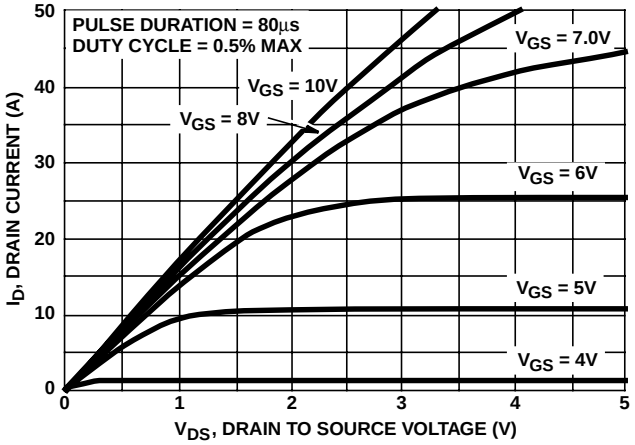


FIGURE 6. SATURATION CHARACTERISTICS

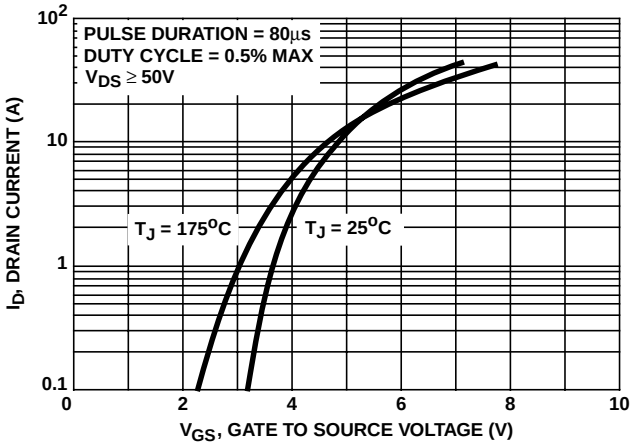
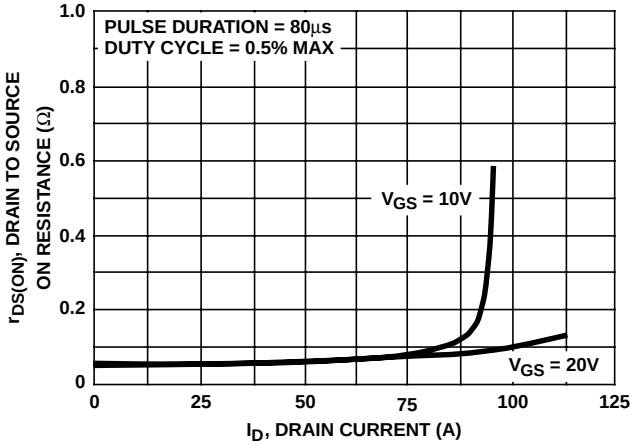


FIGURE 7. TRANSFER CHARACTERISTICS



NOTE: Heating effect of 2µs pulse is minimal.

FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

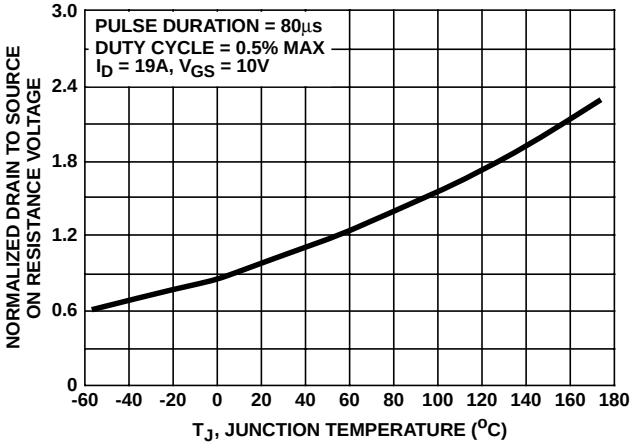


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

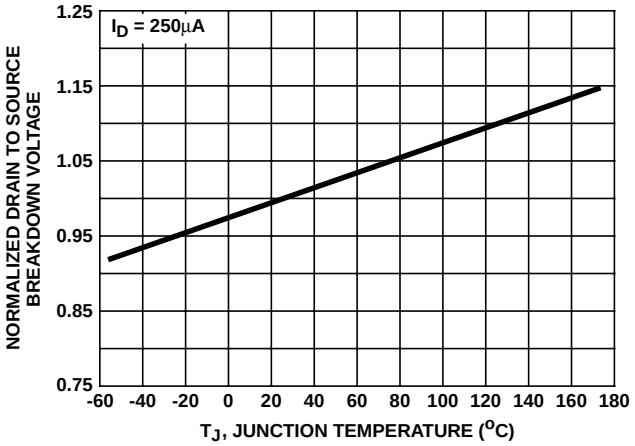


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

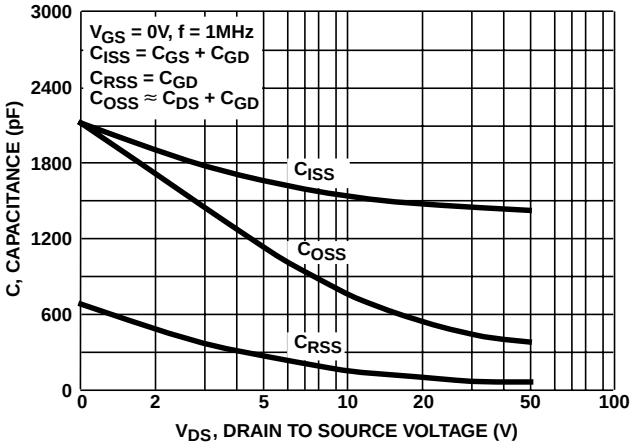


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

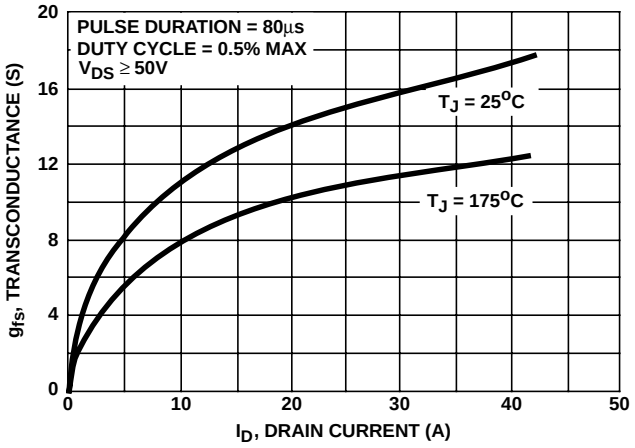


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

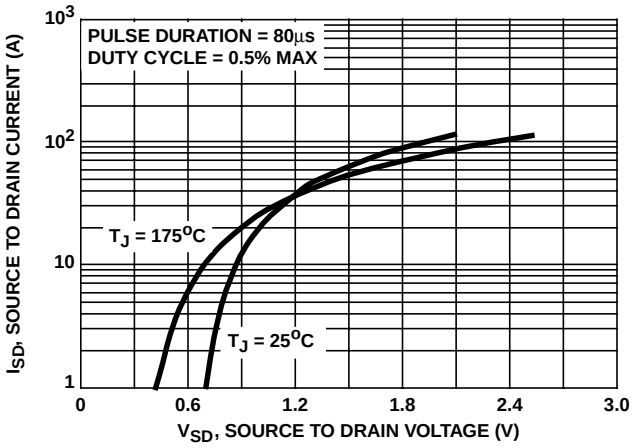


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

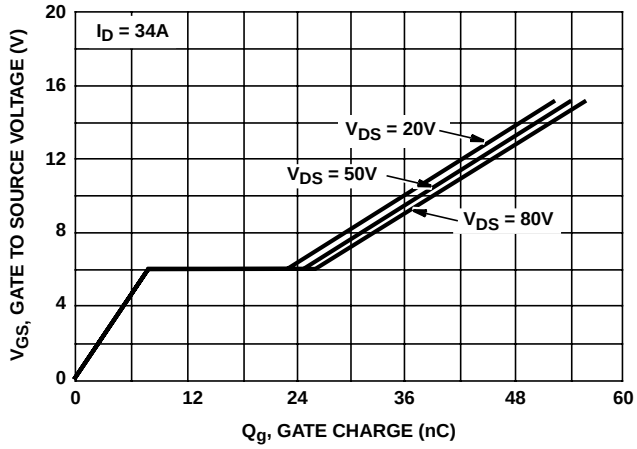


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

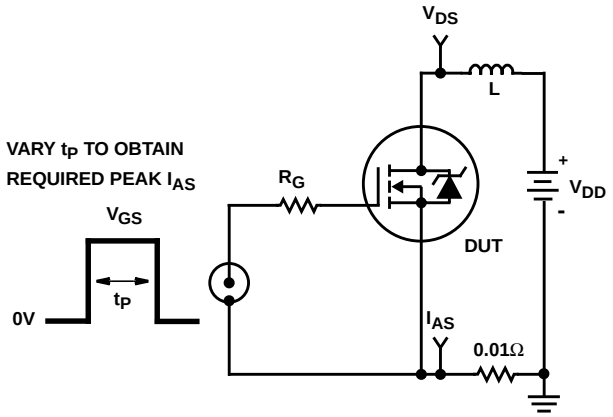


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

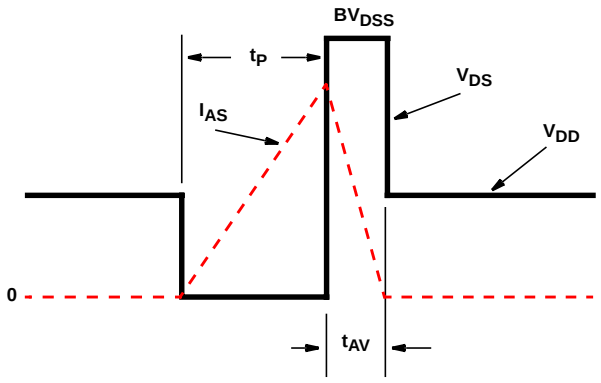


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

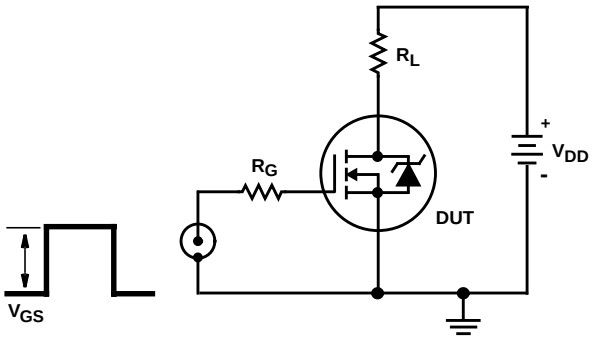


FIGURE 17. SWITCHING TIME TEST CIRCUIT

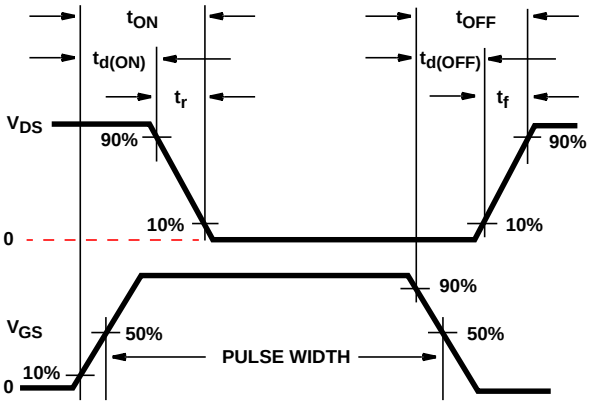


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

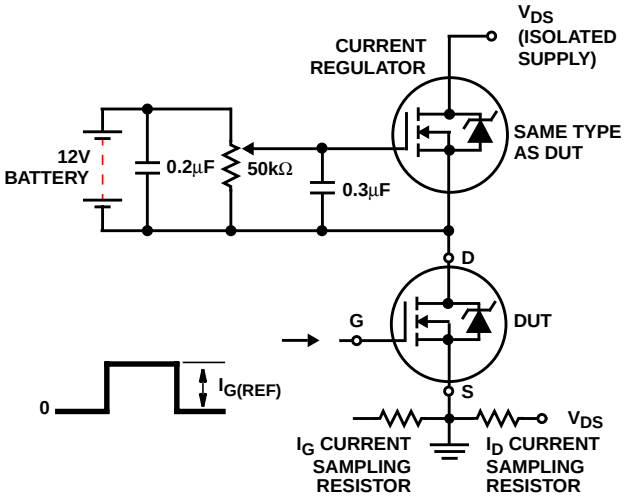


FIGURE 19. GATE CHARGE TEST CIRCUIT

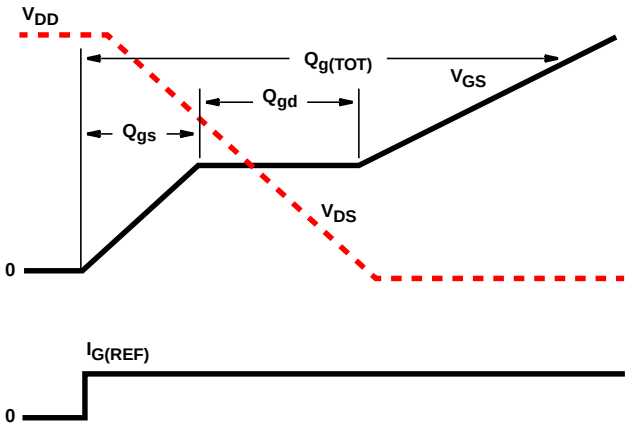


FIGURE 20. GATE CHARGE WAVEFORMS

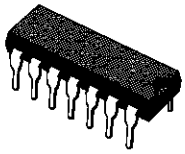
SGS-THOMSON MICROELECTRONICS

HCC4011B/12B/23B
HCF4011B/12B/23B

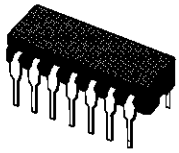
NAND GATES

QUAD 2 INPUT HCC/HCF 4011B
DUAL 4 INPUT HCC/HCF 4012B
TRIPLE 3 INPUT HCC/HCF 4023B

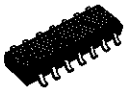
- PROPAGATION DELAY TIME = 60ns (typ.) AT C_L = 50pF, V_{DD} = 10V
- BUFFERED INPUTS AND OUTPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- 5V, 10V AND 15V PARAMETRIC RATINGS
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



EY
(Plastic Package)



F
(Ceramic Frit Seal Package)



M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

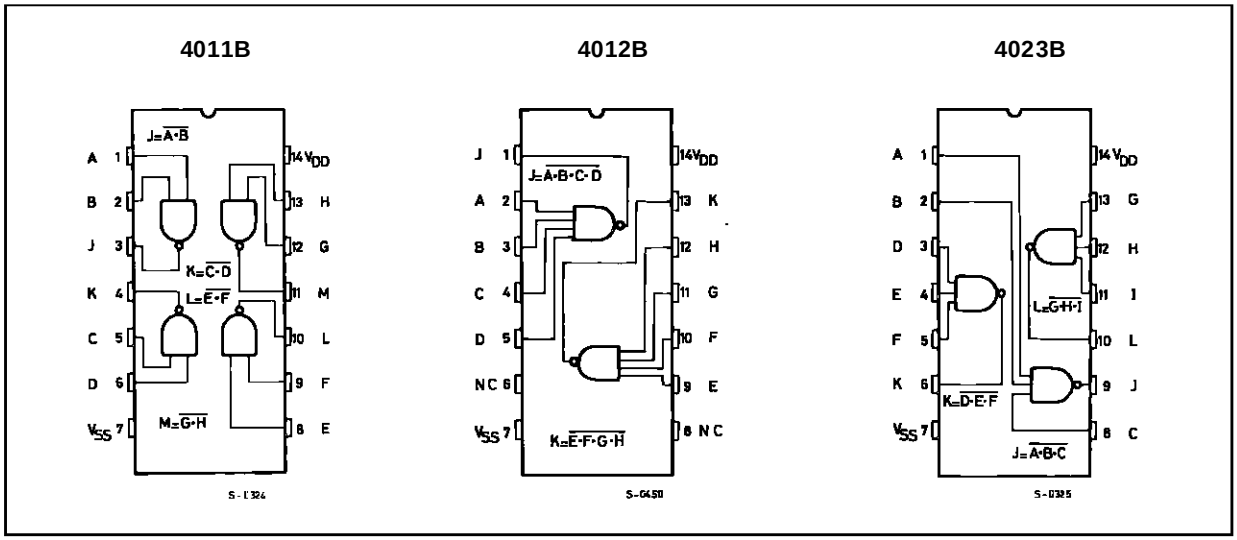
HCC40XXBF	HCF40XXBM1
HCF40XXBEY	HCF40XXBC1

DESCRIPTION

The **HCC4011B, HCC4012B** and **HCC4023B** (extended temperature range) and **HCF4011B, HCF4012B** and **HCF4023B** (intermediate temperature range) are monolithic, integrated circuit, available in 14-lead dual in-line plastic or ceramic package and plastic micropackage.

The **HCC/HCF4011B, HCC/HCF4012B** and **HCC/HCF4023B** NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of COS/MOS gates. All inputs and outputs are buffered.

PIN CONNECTIONS



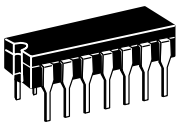
MC14011B/12B (see pg 6-5)
MC14011UB/12UB (see pg 6-14)

MC14013B

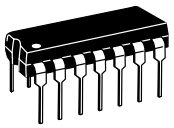
Dual Type D Flip-Flop

The MC14013B dual type D flip–flop is constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. Each flip–flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and $\overline{Q}$). These devices may be used as shift register elements or as type T flip–flops for counter and toggle applications.

- Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge–Clocked Flip–Flop Design
  Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive–going edge of the clock pulse
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range
- Pin–for–Pin Replacement for CD4013B



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646

D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

T_A = – 55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

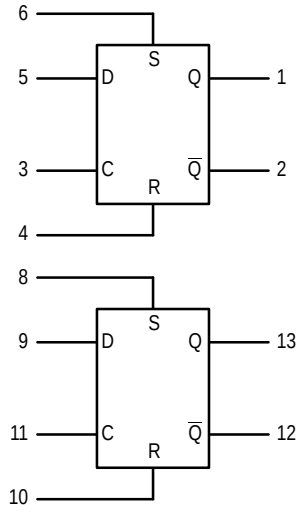
* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C
Ceramic “L” Packages: – 12 mW/°C From 100°C To 125°C

TRUTH TABLE

Inputs				Outputs		
Clock†	Data	Reset	Set	Q	$\overline{Q}$	
↗	0	0	0	0	1	
↗	1	0	0	1	0	
↘	X	0	0	Q	$\overline{Q}$	No Change
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

X = Don’t Care
† = Level Change

BLOCK DIAGRAM



V_{DD} = PIN 14
V_{SS} = PIN 7

REV 3
1/94

14-stage ripple-carry binary counter/divider and oscillator

HEF4060B MSI

DESCRIPTION

The HEF4060B is a 14-stage ripple-carry binary counter/divider and oscillator with three oscillator terminals (RS, R_{TC} and C_{TC}), ten buffered outputs (O_3 to O_9 and O_{11} to O_{13}) and an overriding asynchronous master reset input (MR). The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter (O_3 to O_9 and O_{11} to O_{13} = LOW), independent of other input conditions.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

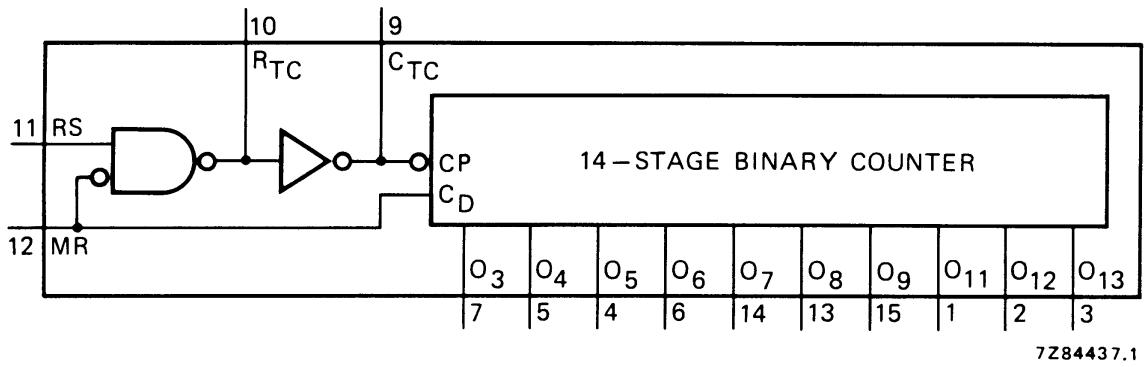


Fig.1 Functional diagram.

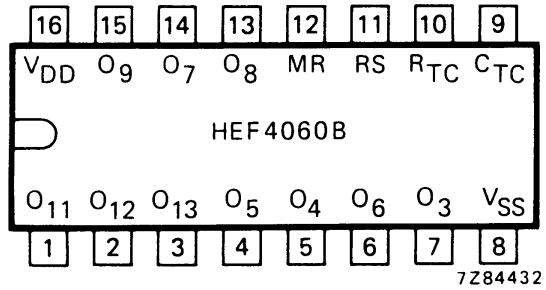


Fig.2 Pinning diagram.

PINNING

MR	master reset
RS	clock input/oscillator pin
R_{TC}	oscillator pin
C_{TC}	external capacitor connection
O_3 to O_9 O_{11} to O_{13}	counter outputs

HEF4060BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4060BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4060BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

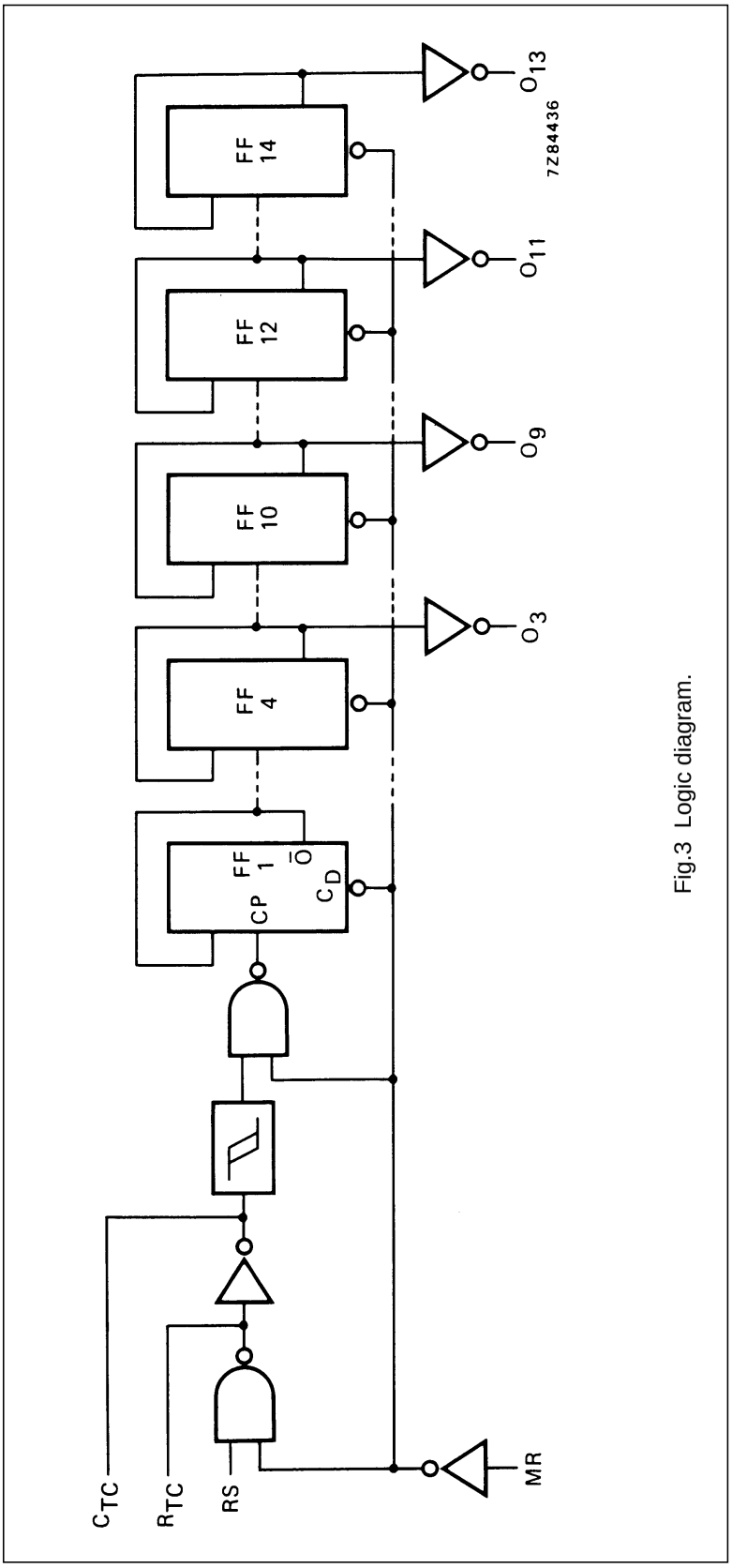


Fig.3 Logic diagram.