JEDEC STANDARD

Temperature, Bias, and Operating Life

JESD22-A108-B
(Revision of JESD22-A108-A)

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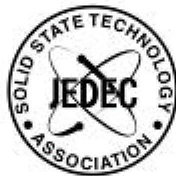
JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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TEST METHOD A108-B
TEMPERATURE, BIAS, AND OPERATING LIFE

(From JEDEC Board Ballots JCB-99-89 and JCB-99-89A, formulated under the cognizance of JC-14.1 Committee on Reliability Test Methods for Packaged Devices.)

1 Purpose

This test is used to determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way, and is primarily for device qualification and reliability monitoring. A form of high temperature bias life using a short duration, popularly known as burn-in, may be used to screen for infant mortality-related failures. The detailed use and application of burn-in is outside the scope of this document.

1.1 Applicable documents

EIA/JESD 47	Stress-Test Driven Qualification of Integrated Circuits
EIA/JEP 122	Failure Mechanism and Models for Silicon Semiconductor Devices

2 Apparatus

The performance of this test requires equipment that is capable of providing the particular stress conditions to which the test samples will be subjected.

2.1 Circuitry

The circuitry through which the samples will be biased must be designed with several considerations:

2.1.1 Device schematic

The biasing and operating schemes must consider the limitations of the device and shall not overstress the devices or contribute to thermal runaway.

2.1.2 Power

The test circuit should be designed to limit power dissipation such that, if a device failure occurs, excessive power will not be applied to other devices in the sample.

2.2 Device mounting

Equipment design, if required, shall provide for mounting of devices to minimize adverse effects while parts are under stress , (e.g., improper heat dissipation).

2 Apparatus (cont'd)

2.3 Power supplies and signal sources

Instruments (such as DVMs, oscilloscopes, etc.) used to set up and monitor power supplies and signal sources shall be calibrated and have good long-term stability .

2.4 Environmental chamber

The environmental chamber shall be capable of maintaining the specified temperature within a tolerance of ± 5 °C throughout the chamber while parts are loaded and unpowered.

3 Definitions

3.1 Maximum operating voltage

The maximum supply voltage at which a device is specified to operate in compliance with the applicable device specification or data sheet.

3.2 Absolute maximum rated voltage

The maximum voltage that may be applied to a device, beyond which damage (latent or otherwise) may occur; it is frequently specified by device manufacturers for a specific device and/or technology.

3.3 Absolute maximum rated junction temperature

The maximum junction temperature of an operating device, beyond which damage (latent or otherwise) may occur; it is frequently specified by device manufacturers for a specific device and/or technology.

NOTE Manufacturers may also specify maximum case temperatures for specific packages.

4 Procedure

The sample devices shall be subjected to the specified or selected stress conditions for the time and temperature required.

4.1 Stress duration

The bias life duration is intended to meet or exceed an equivalent field lifetime under use conditions. The duration is established based on the acceleration of the stress (see EIA/JEP 122). The stress duration is specified by internal qualification requirements, EIA/JESD 47 or the applicable procurement document. Interim measurements may be performed as necessary per restrictions in clause 6.

4 Procedure (cont'd)

4.2 Stress conditions

The stress condition shall be applied continuously (except during interim measurement periods). The time spent elevating the chamber to accelerated conditions, reducing chamber conditions to room ambient, and conducting the interim measurements shall not be considered a portion of the total specified test duration.

4.2.1 Ambient temperature

Unless otherwise specified, the ambient temperature and bias for high temperature stress shall be adjusted to result in a minimum junction temperature of the devices under stress of 125 °C. Unless otherwise specified, the ambient temperature for low temperature stress shall be a maximum of –10 °C.

4.2.2 Operating voltage

Unless otherwise specified, the operating voltage should be the maximum operating voltage specified for the device unless the conditions of 4.2.1 cannot be met. A higher voltage is permitted in order to obtain lifetime acceleration from voltage as well as temperature; this voltage must not exceed the absolute maximum rated voltage for the device, and must be agreed upon by the device manufacturer.

4.2.3 Biasing configurations

Biasing configurations may be bias stress (static or pulsed) or operating stress (dynamic). Depending upon the biasing configuration, supply and input voltages may be grounded or raised to a maximum potential chosen to ensure a stressing temperature not higher than the maximum-rated junction temperature. Device outputs may be unloaded or loaded, to achieve the specified output voltage level. If a device has a thermal shutdown feature it shall not be biased in a manner that could cause the device to go into thermal shutdown.

4.2.3.1 High temperature forward bias (HTFB)

The HTFB test is configured to forward bias major power handling junctions of the device samples. The devices may be operated in either a static or a pulsed forward bias mode. Pulsed operation is used to stress the devices at, or near, maximum-rated current levels. The particular bias conditions should be determined to bias the maximum number of the solid state junctions in the device. The HTFB test is typically applied on power devices, diodes, and discrete transistor devices (not typically applied to integrated circuits).

4.2 Stress conditions (cont'd)

4.2.3.2 High temperature operating life (HTOL) / Low temperature operating life (LTOL)

The HTOL / LTOL test is configured to bias the operating nodes of the device samples. The devices may be operated in a dynamic operating mode. Typically, several input parameters may be adjusted to control internal power dissipation. These include: supply voltages, clock frequencies, input signals, etc., that may be operated even outside their specified values, but resulting in predictable and nondestructive behavior of the devices under stress. The particular bias conditions should be determined to bias the maximum number of potential operating nodes in the device. The HTOL test is typically applied on logic and memory devices. The LTOL test is intended to look for failures caused by hot carriers, and is typically applied on memory devices or devices with submicron device dimensions.

4.2.3.3 High temperature reverse bias (HTRB)

The HTRB test is configured to reverse bias major power handling junctions of the device samples. The devices are characteristically operated in a static operating mode at, or near, maximum-rated breakdown voltage and/or current levels. The particular bias conditions should be determined to bias the maximum number of the solid state junctions in the device. The HTRB test is typically applied on power devices.

4.2.3.4 High temperature gate bias (HTGB)

The HTGB test biases gate or other oxides of the device samples. The devices are normally operated in a static mode at, or near, maximum-rated oxide breakdown voltage levels. The particular bias conditions should be determined to bias the maximum number of gates in the device. The HTGB test is typically used for power devices.

5 Cool-down

Devices on high temperature stress shall be cooled to 55 °C or lower before removing the bias. Cooling under bias is not required for a given technology if verification data is provided by the manufacturer. The interruption of bias for up to one minute, for the purpose of moving the devices to cool-down positions separate from the chamber within which life testing was performed, shall not be considered removal of bias. All specified electrical measurements shall be completed prior to any reheating of the devices, except for interim measurements subject to restrictions of clause 6.

NOTE Bias refers to application of voltage to power pins.

6 Measurements

The measurements specified in the applicable life test specification shall be made initially, at the end of each interim period, and at the conclusion of the life test. Interim and final measurements may include high temperature testing. However, testing at elevated temperatures shall only be performed after completion of specified room (and lower) temperature test measurements. After interim testing, bias shall be applied to the parts before heat is applied to the chamber, or within ten minutes of loading the final parts into a hot chamber. Electrical testing shall be completed as soon as possible and no longer than 96 hours after removal of bias from devices. If the availability of test equipment or other factors make meeting this requirement difficult, bias must be maintained on the devices either by extending the Bias Life Stress or keeping the devices under bias at room temperature until this 96 hour window can be met. This and the high temperature testing restrictions of this clause need not be met if verification data for a given technology is provided.

NOTE If the devices have been removed from bias and the 96 hour window is not met, the stress must be resumed prior to completion of the measurements. The duration of this stress shall be 24 hours for any portion of each week the limit is exceeded (i.e., 24 hours if the limit is exceeded by ? 168 hours, 48 hours if the limit is exceeded by > 168 hours but ? 336 hours, etc.). After an interim measurement, the stress shall be continued from the point of interruption.

7 Failure criteria

A device is defined as a failure if it does not meet the requirements of the applicable procurement document.

8 Summary

The following items shall be specified in the applicable life test specification:

a) Special preconditioning, when applicable.

b) Stress temperature (chamber ambient)

c) Stress duration.

d) Stress mounting, if special instructions are needed.

e) Stress condition and stress circuit schematic.

f) Sample size and acceptance number.

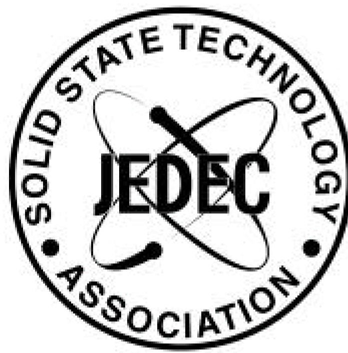
g) Time to complete endpoint measurements, if other than specified in paragraph 5.

h) Operating mode.

i) Interim read points, if required.

j) Maximum junction temperature during stress.

k) Verification data if cool-down under bias is not performed.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