7th INTERNATIONAL SYMPOSIUM ON THE PHYSICAL AND FAILURE ANALYSIS OF INTEGRATED CIRCUITS

IPFA 99

PROGRAMME

5 - 9 July 1999
Orchard Hotel, Singapore

Organised by:
IEEE Reliability/CPMT/ED
Singapore Chapter

IEEE

Co-sponsored by:
IEEE Electron Device Society

In Cooperation with:
Centre for Integrated Circuit Failure Analysis and Reliability (CICFAR) - NUS
and
Institute of Microelectronics, Singapore

IPFA '99 –TECHNICAL PROGRAMME

DAY 1: 6 July 1999

8.00 AM **Registration**

8.30 AM **Symposium Opening**

8.45 AM **Keynote Address:** Impact of New Materials, Changes in Physics and Continued ULSI Scaling on Failure Mechanisms and Analysis
Yoshio Nishi and J. W. McPherson
Texas Instruments, USA

9:30 AM **SESSION 1: FAILURE ANALYSIS TECHNIQUES I**

1.1 **Invited Paper:** Can Failure Analysis Keep Pace with IC Technology Development?
Christian Boit
Siemens Semiconductors, Germany

1.2 Laser Voltage Probe (LVP): A Novel Optical Probing Technology for Flip-Chip Packaged Microprocessors
W.M. Yee, M. Paniccia*, T. Eiles* and V.R.M. Rao*
*Intel Microelectronics, Malaysia; *Intel Corporation, USA*

10:20 AM **COFFEE BREAK**

10:50 AM **SESSION 2: BUILDING-IN-RELIABILITY**

2.1 Influence of Passivation Anneal Position on Metal Coverage Dependent Mismatch and Hot Carrier Reliability
S. Chetlur. S. Sen, E. Harris, H. Vaidya, I. Kizilyalli, R. Gregor and B. Harding
Lucent Technologies, USA

2.2 The Effect of Nitrogen Pre-Annealing on the Sidewall Oxidation of WSi_x and on the Related Electrical Properties of WSi_x/Poly Si Gate Structure
D.H Kang, H.S. Kim, M.J. Chung, K.H. Ahn, G.S. Cho, J.B. Park and Y.H.Koh
Hyundai Electronic Industries., Korea

2.3 Radiation-Induced Leakage Current of Ultra-Thin Gate Oxide Under X-Ray Lithography Conditions
B.J. Cho, S.J. Kim, C.H. Ling, M.S. Joo* and I.S. Yeo*
*National University of Singapore, Singapore; *Hyundai Electronics Industries., Korea*

2.4 Excellent Quality Ultra-Thin Oxides Prepared by Room Temperature Anodic Oxidation
J.S. Liu and M.C. Chiang
National Nano Device Laboratory, Taiwan, ROC

12:15 PM **LUNCH**

1:45 PM **SESSION 3: PACKAGING AND METALLIZATION I**

3.1 Impact of Test Structure Design on Electromigration of Metal Interconnect
Q. Guo, K.F. Lo, X. Zeng and S.P. Neo
Chartered Semiconductor Manufacturing, Singapore

3.2 A New Test for Delamination as an Interconnect Failure Mechanism
B.K. Jones, J.P. Guo, G. Trefan and A. Braghieri*
*Lancester University, UK; *University of Parma, Italy*

3.3 Detection of Underfill Epoxy Defects in Flip Chip Packages with the Aid of SAM, Parallel Polishing & FIB
T.N. Tang, H.C. Heng, S.Y. Chan and M. Hiew
Advanced Micro Devices Export, Malaysia

3.4 Monte-Carlo Simulation of Electromigration in Polycrystalline Metal Stripes
S. Di Pascoli and G. Iannaccone
University of Pisa, Italy

3.5 Impact of Intermetal Dielectric Process on Al Via Electromigration Reliability
X. Liu, K. F. Lo, K.Y. Chin, Q. Guo and G.L. Teh,
Chartered Semiconductor Manufacturing, Singapore

3:30 PM COFFEE BREAK

4:00 PM SESSION 4: FAILURE ANALYSIS TECHNIQUES II

4.1 Failure Analysis of uBGA - New Approaches in Fault Isolation
S.K. Kuan and S.T. Teh
Advanced Micro Devices Export, Malaysia

4.2 New FIB-Supported Approaches for EELS-Capable TEM-Lamella Preparation
P. Jacob, A. Schertel* and L. Peto**
*EMPA Duebendorf, Switzerland; *Micrion Europe, Germany; **Micrion Corp Ltd., UK*

4.3 Illumination-Sensitive Failure Mechanism - A Case Study on Transient I_{cc} Failure
S.T. Teh and W.Y. Teoh
Advanced Micro Devices Export, Malaysia

DAY 2: 7 July 1999

9:00 AM SESSION 5: DIELECTRICS I

5.1 Origin of the Substrate Current After Soft-Breakdown in Thin Oxide n-MOSFETs
F. Crupi, G. Iannaccone, B. Neri, R. Degraeve*, G. Groeseneken*, H.E. Maes*;
*University of Pisa, Italy; *IMEC, Belgium*

5.2 A Study of Quasi-Breakdown Mechanism in Ultra-Thin Gate Oxide by Using DCIV Technique
H. Guan, B.J. Cho, M.F. Li, Y.D. He, Z. Xu and Z. Dong*
*National University of Singapore, Singapore; *Chartered Semiconductor Manufacturing, Singapore*

5.3 A Detailed Analysis of the Pre-Breakdown Current Fluctuations in Thin Oxide MOS Capacitors
B. Neri, F. Crupi, G. Basso, and S. Lambardo*
*University of Pisa, Italy; *Instituto Nazionale di Metodologie e Tecnologie per la Microelettronica, Italy*

10:15 AM COFFEE BREAK

10:45 AM SESSION 6: HOT-CARRIER I

6.1 A New DC Voltage-Voltage Method to Measure the Interface Traps in Deep Sub-Micrometer MOS Transistors
B.B. Jie, M.F. Li, W.K. Chim, D.S.H. Chan and K.F. Lo*;
*National University of Singapore, Singapore; *Chartered Semiconductor Manufacturing, Singapore*

6.2 Channel-Width Effect on Hot-Carrier Degradation in NMOSFETs with Recessed-LOCOS Isolation Structure

J.M.P. Yue, W.K. Chim, B.J. Cho, W.H. Qin, D.S.H. Chan, Y.B. Kim*, S.A.Jang* and I.S. Yeo*

*National University of Singapore, Singapore; *Hyundai Electronics Industries, Korea*

6.3 Series Resistance and Effective Channel Mobility Degradation in LDD NMOSFETs Under Hot-Carrier Stressing

G.G. Oh, W.K. Chim, D.S.H. Chan and C.L. Lou*

*National University of Singapore, Singapore; *Hewlett-Packard, Singapore*

12:00 NOON LUNCH

1:30 PM SESSION 7: FAILURE ANALYSIS TECHNIQUES III

7.1 Automatic DRAM Cell Location in the SEM

J.T.L Thong, Y. Zhu and J.C.H. Phang

National University of Singapore, Singapore

7.2 Characterization and Application of Highly-Sensitive Infra-Red Emission Microscopy for Integrated Circuit Backside Failure Analysis

T.H. Loh, W.M. Yee and Y.Y. Chew

Intel Microelectronics, Malaysia

7.3 An Integrated (Automated) Photon Emission Microscope and MOSFET Characterization System for Combined Microscopic and Macroscopic Device Analysis

T.H. Ng, W.K. Chim, D.S.H. Chan, J.C.H. Phang, Y.Y. Liu, C.L. Lou*, S.E. Leang** and J.M. Tao**

*National University of Singapore, Singapore; *Hewlett-Packard., Singapore; **Chartered Semiconductor Manufacturing, Singapore*

7.4 Novel Backside Sample Preparation Processes for Advanced CMOS Integrated Circuits Failure Analysis

Y.Y. Chew, K.H. Siek and W.M. Yee

Intel Microelectronics, Malaysia

3:00 PM COFFEE BREAK

3:30 PM SESSION 8: PACKAGING AND METALLIZATION II

8.1 Impact of Failure Criterion on Electromigration of W-plug Contact

Q. Guo, K.F. Lo, X, Zeng, X. Liu, P. Yao and P.Y. Tan

Chartered Semiconductor Manufacturing, Singapore

8.2 Identification of Processing Defects by Focused Ion Beam (FIB) Induced Voltage Contrast

C.S. Liu and Y. F. Hsieh

United Microelectronics Corporation, Taiwan, ROC

8.3 Long Term Noise Measurements to Characterize Electromigration in Metal Lines of ICs

C. Ciofi, V. Dattilo and B. Neri

University of Pisa, Italy

DAY 3: 8 July 1999

9:00 AM SESSION 9: DIELECTRICS II

9.1 An Empirical Breakdown Model of the Gate Oxide Under Current Stress
J.H. Seo and J.C.S. Woo
University of California, USA

9.2 A Comparison of Interface Trap Generation by Fowler-Nordheim Electron Injection and Hot-Hole Injection Using the DCIV Method
K.H. Ng, B.B. Jie, Y.D. He, W.K. Chim, M.F. Li and K.F. Lo*,
*National University of Singapore, Singapore; *Chartered Semiconductor Manufacturing, Singapore*

9.3 The Electric Field, Oxide Thickness, Time and Fluence Dependence of Trap Generation in Silicon Oxides and Their Support of the E-Model of Oxide Breakdown
D. Qian and D. Dumin
Clemson University, USA

10:15 AM COFFEE BREAK

10:45 AM SESSION 10: EOS/ESD AND LATCHUP

10.1 A Novel Dual-Direction IC ESD Protection Device
A.Z. Wang, C.H. Tsay* and Q.W. Shan@
*Illinois Institute of Technology, USA; *National Semiconductor, USA; @OminVision Technologies, USA*

10.2 Latent Damage Investigation on Lateral Non-Uniform Charge Generation and Stress-Induced Leakage Current in Silicon Dioxides Subjected to Low-Level Electrostatic Discharge Impulse Stressing
P.S. Lim and W.K. Chim
National University of Singapore, Singapore

10.3 An Analytical Model of Positive H.B.M. ESD Current Distribution and Modified Multi-Finger Protection Structure
J.H. Lee, J.R. Shih, H.L. Hwang*, B.K. Liew
*Taiwan Semiconductor Manufacturing; *Tsing-Hua University, Taiwan, ROC*

10.4 A Latch-up Immunized Lateral Trench-Gate Conductivity Modulated Power Transistor
J. Cai and K.F. Lo
Chartered Semiconductor Manufacturing, Singapore

12:15 PM LUNCH

1:45 PM SESSION 11: PHYSICAL ANALYSIS AND RELIABILITY OF SPECIALIST DEVICES

11.1 **Invited Paper:** Physical Analysis and Modeling of the Reliability of AlGaAs/GaAs HBTs
J. J. Liou and Tim Henderson*
*University of Central Florida, *Texas Instruments; USA*

11.2 Study on LED Degradation Using CL, EBIC and a Two-Diode Parameter Extraction Model
H. Xiao, Y.Y, Liu, J.C.H. Phang, D.S.H. Chan, W.K. Chim, K.P. Yan*;
*National University of Singapore, Singapore; *Siemens Components, Malaysia*

11.3 Temperature Distribution in Power GaAs Field Effect Transistors Using Spatially Resolved Photoluminescence Mapping

E. Martin, J.P. Landesman and P. Braun*

*Thomson-CSF, France; *United Monolithic Semiconductors, Germany*

11.4 Analysis of Surface-State Effects on Gate-Lag Phenomena in Recessed-Gate and Buried-Gate GaAs MESFETs

K. Horio, A. Wakabayashi and T. Yamada

Shibaura Institute of Technology, Japan

3:15 PM COFFEE BREAK

3:45 PM SESSION 12: HOT-CARRIER II

12.1 Low-Voltage Forward Gated Diode: An Early Monitor of Hot-Carrier Degradations in Scaled MOSFETs

M.J. Chen and T. K. Kang

National Chiao-Tung University, Taiwan, ROC

12.2 A Comparative Study of Charge Trapping Effects in LDD Surface-Channel and Buried-Channel PMOS Transistors Using Charge Profiling and Threshold Voltage Shift Measurements

C.K. Kok, W.C. Chew, W.K. Chim, D.S.H. Chan, S.E. Leang*;

*National University of Singapore, Singapore; *Chartered Semiconductor Manufacturing, Singapore*

12.3 Energy Dependence of Interface Trap Density - Investigated by the DCIV Method

B.B. Jie, M.F. Li and K.F. Lo*

*National University of Singapore, Singapore; *Chartered Semiconductor Manufacturing; Singapore*