ISOSMART™ Half Bridge Driver Chipsets

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<th>Temperature Range</th>
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<td>Full-Feature Low-Side Driver</td>
<td>16-Pin P-DIP</td>
<td>-40 to +85°C</td>
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<tr>
<td>IXBD4411PI</td>
<td>Full-Feature High-Side Driver</td>
<td>16-Pin P-DIP</td>
<td>-40 to +85°C</td>
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<tr>
<td>IXBD4410SI</td>
<td>Full-Feature Low-Side Driver</td>
<td>16-Pin SO</td>
<td>-40 to +85°C</td>
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<td>IXBD4412PI</td>
<td>Basic Low-Side Driver</td>
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<td>-40 to +85°C</td>
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<td>Basic High-Side Driver</td>
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<td>Basic Chipset Evaluation Kit PCB</td>
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<td>0 to +70°C</td>
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The IXBD4410/IXBD4411 and the IXBD4412/IXBD4413 ISOSMART™ chipsets are designed to control the gates of two Power MOSFETs, or Power IGBTs, that are connected in a half-bridge (phase leg) configuration for driving multiple-phase motors, or used in applications that require half-bridge power circuits. The IXBD4410/IXBD4411 is a full-feature chipset consisting of two 16-Pin-DIP or SO devices interfaced and isolated by two small-signal ferrite pulse transformers. The IXBD4412/IXBD4413 is a basic, low-cost chipset consisting of two 8-Pin-DIP devices interfaced and isolated by a single pulse transformer. The small-signal transformers in both chipsets provide greater than 1200 V isolation.

Even with commutating noise ambients greater than ±50 V/ns and up to 1200 V potentials, these chipsets establish error-free two-way communications between the system ground-reference IXBD4410 resp. IXBD4412 and the inverter output-reference IXBD4411 resp. IXBD4413. They incorporate undervoltage $V_{DD}$ or $V_{EE}$ lockout, and overcurrent or desaturation shutdown to protect the IGBT or Power MOSFET devices from damage.

Both chipsets provide the necessary gate drive signals to control the grounded-source low-side power device, as well as the floating-source high-side power device. Additionally, the IXBD4410/4411 chipset provides a negative-going, off-state gate drive signal for improved turn-off of IGBTs, or Power MOSFETs, and a system logic-compatible status fault output, FLT, to indicate overcurrent or desaturation, and undervoltage $V_{DD}$ or $V_{EE}$. During a status fault, both chipsets keep their respective gate drive outputs off; at $V_{EE}$ for the IXBD4410/4411 and at 0 V for the IXBD4412/4413.

### Features
- 1200 V or greater low- to high-side isolation.
- Drives Power Systems Operating on up to 575 V AC mains
- dv/dt immunity of greater than ±50 V/ns
- Proprietary low- to high-side level-translation and communication
- On-chip negative gate-drive supply to ensure Power MOSFET or IGBT turn-off
- 5 V logic compatible HCMOS inputs with hysterisis
- Available in either the 16-Pin DIP or the 16-Pin wide-body, small-outline plastic package (IXBD4410/4411)
- 20 ns switching time with 1000 pF load, 100 ns switching time with 10000 pF load
- 100 ns propagation delay time
- 2 A peak output drive capability
- Self shut-down of output in response to over-current or short-circuit
- Under-voltage and over-voltage $V_{DD}$ lockout protection
- Protection from cross conduction of the half bridge
- Logic compatible fault indication from both low and high-side driver (IXBD4410/4411).

### Applications
- 1- or 3-Phase Motor Controls
- Switch Mode Power Supplies (SMPS)
- Uninterruptible Power Supplies (UPS)
- Induction Heating and Welding Systems
- Switching Amplifiers
- General Power Conversion Circuits

IXYS reserves the right to change limits, test conditions and dimensions.

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Symbol | Definition | Maximum Ratings
--- | --- | ---
V\textsubscript{DD}/V\textsubscript{EE} | Supply Voltage | 4410/4411: -0.5 ... 24 V, 4412/4413: -0.5 ... 24 V
V\textsubscript{DD}/GND | Input Voltage (INH, INL) | 4412/4413: -0.5 ... 24 V
V\textsubscript{in} | Input Voltage (INH, INL) | -0.5 ... +0.5 V
I\textsubscript{in} (rev) | Peak Reverse Output Current (OUT) | 2 A
P\textsubscript{D} | Maximum Power Dissipation | 600 mW
T\textsubscript{A} | Operating Ambient Temperature | -40 ... 85 °C
T\textsubscript{J\textsubscript{max}} | Maximum Junction Temperature | 150 °C
T\textsubscript{stg} | Storage Temperature Range | -55 ... 150 °C
T\textsubscript{L} | Lead Soldering Temperature for 10 s | 300 °C

Recommended Operating Conditions

Symbol | Definition/Condition | Characteristic Values
--- | --- | ---
V\textsubscript{DD}/V\textsubscript{EE} | Supply Voltage | 4410/4411: 10 ... 20 V, 4412/4413: 10 ... 20 V, 10 ... 16.5 V
V\textsubscript{DD}/GND | Input Voltage | 10 ... 20 V
L\textsubscript{CM}/R\textsubscript{CM} | Maximum Common Mode dv/dt | ±50 V/ns

Symbol | Definition/Condition | Characteristic Values
--- | --- | ---
V\textsubscript{t\textsuperscript{+}} | Positive-Going Threshold | 3.65 V
V\textsubscript{t\textsuperscript{-}} | Negative-Going Threshold | 1 V
V\textsubscript{ih} | Input Hysteresis | 1 V
I\textsubscript{leak} | Input Leakage Current/V\textsubscript{DD} or LG | -1 µA
C\textsubscript{in} | Input Capacitance | 10 pF

Open Drain Fault Output (referred to LG for 4410/4411)

Symbol | Definition/Condition | Characteristic Values
--- | --- | ---
V\textsubscript{oh} | HI Output/R\textsubscript{\text{HI}} = 10 kΩ to V\textsubscript{DD} | V\textsubscript{DD} - 0.05 V
V\textsubscript{ol} | LO Output/I\textsubscript{L} = 4 mA | 0.3 V, 0.5 V

OUT Output (referred to LG)

Symbol | Definition/Condition | Characteristic Values
--- | --- | ---
V\textsubscript{oh} | HI Output/I\textsubscript{L} = -5 mA | V\textsubscript{DD} - 0.05 V
V\textsubscript{ol} | LO Output/I\textsubscript{L} = 5 mA | V\textsubscript{EE} + 0.05 V
R\textsubscript{o} | Output HI Res./I\textsubscript{L} = -0.1 A | 3 Ω, 5 Ω
R\textsubscript{o} | Output LO Res./I\textsubscript{L} = 0.1 A | 3 Ω, 4 Ω
I\textsubscript{pk} | Peak Output Current/C\textsubscript{L} = 10 nF | 1.5 A, 2 A

IM Input (referred to KG for 4410/4411 and to LG for 4412/4413)

Symbol | Definition/Condition | Characteristic Values
--- | --- | ---
V\textsubscript{t\textsuperscript{+}} | Positive-Going Threshold | 0.24 V, 0.3 V, 0.45 V
C\textsubscript{in} | Input Capacitance | 10 pF
R\textsubscript{s} | Shorting Device Output Resistance | 50 Ω, 75 Ω, 100 Ω

VEE Supply (referred to LG for 4410/4411)

Symbol | Definition/Condition | Characteristic Values
--- | --- | ---
V\textsubscript{EE} | Output Voltage/C\textsubscript{L} = 1 mA, C\textsubscript{C} = 1 µF | -5 V, -6.5 V, -7.5 V
I\textsubscript{out} | Output Current/C\textsubscript{out} = 0.70 · V\textsubscript{EE} | -20 mA, -25 mA
f\textsubscript{inv} | Inverting Frequency | 600 kHz
V\textsubscript{EEF} | Undervoltage Fault Indication | -3 V, -4.8 V

Dimensions in inch (1" = 25.4 mm)

16-Pin Plastic DIP

Cross view for both packages

8-Pin Plastic DIP

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Symbol | Definition/Condition | Characteristic Values  
--- | --- | ---  
$V_{DD}$ | Undervoltage Lockout  
$V_{UV}$ | Drop Out | 9.5 | 10.5 | 11.5 | V  
$V_{uh}$ | Hysteresis | 0.1 | 0.15 | 0.3 | V  

**Quiescent Power Supply Current**  
$I_{DD}$ | $V_{DD}$ Current/ $V_{in} = V_{DD}$ or LG, $I_o = 0$ | 20 | mA  

**INL and INH Inputs** (Fig. 1a - 1c)  
$t_{o(h)}$ | Turn-on delay time; $C_L = 1nF$  
4410/4412 | $t_{r}$ | Rise time; $C_L = 10 nF$ | 70 | 100 | ns  
4411/4413 | $t_{d(off)}$ | Turn-off delay time $C_L = 1nF$ | 70 | 150 | ns  
4410/4412 | $t_f$ | Fall time $C_L = 10 nF$ | 70 | 150 | ns  
4411/4413 | $t_{d(on)}$ | Turn-on delay time vs.  
4410/4412 | $C_L = 1nF$ | 4411/4413 | Turn-off delay time | 60 | 150 | ns  
$t_{d(on)}$ | Turn-on delay time vs.  
4410/4412 | $C_L = 1nF$ | 4411/4413 | Turn-off delay time | 60 | 150 | ns  
$t_{d(off)}$ | Turn-off delay time $C_L = 1nF$ | 70 | 150 | ns  
4410/4412 | $t_{dlh(on)}$ | Turn-on delay time vs.  
4410/4412 | $C_L = 1nF$ | 4411/4413 | Turn-off delay time | 60 | 150 | ns  
$t_{dlh(on)}$ | Turn-on delay time vs.  
4410/4412 | $C_L = 1nF$ | 4411/4413 | Turn-off delay time | 60 | 150 | ns  

**Fault Output Delay for any Fault Conditions (4410/4411)**  
$t_{FLT}$ | FLT Delay/R$_{pu} = 2\, \text{k}\Omega$ | 200 | 300 | ns  

**Overcurrent Protection Delay**  
$t_{oc}$ | Driver-Off delay time $C_L = 1\, nF$ | 200 | 300 | ns  

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Chipset Overview

The ISOSMART™ chipsets are pairs of integrated circuits providing isolated high- and low-side drivers for phase leg motor control, or any other application which utilizes a half bridge, 2- or 3-phase drive configuration. They consist of two drive control inputs (INL and INH) for two Power-MOSFET/IGBT gate-drive outputs. Both inputs operate from a common ground, and are activated by HCMOS compatible logic levels. The low-side output operates near input ground, while the high-side output operates from a floating ground that is nominally the source connection of the high-side phaseleg power device. Both outputs typically provide 2 A of transient current drive for fast switching of the phase leg power device.

IXBD4410/IXBD4411

The full featured ISOSMART™ driver chipset incorporates a IXBD4410 as the low-side driver (Fig. 3) and a IXBD4411 as the high-side driver (Fig. 2). When input "INL" is set to a positive logic level, the low-side gate output goes high (turns on); when "INH" is set to a positive logic level, the high-side gate drive output goes high. The high-side IC is isolated from the low-side IC by a magnetic barrier, across which the turn on/off signal is transmitted to the high-side gate drive. In the case of the IXBD4410/4411 chipset, the IXBD4411 fault signal is also transmitted back to the IXBD4410 driver. This isolation only depends on the low cost communications transformer, which is designed to withstand 1200 V or more.

There are two magnetic transmission channels between the low- and high-side IC’s for bi-directional communication (IXBD4410/4411). One sends a signal from the low-side IXBD4410 IC up to the high-side IXBD4411 IC, and the other sends a signal back from the high-side to the low-side IC. The signal that is sent up controls the IXBD4411 gate-drive output. The signal sent from the IXBD4411 back to the IXBD4410 indicates a high-side fault has occurred (overcurrent, or under-voltage of the high-side power supplies). This is detected at the IXBD4410 driver and sets “FLT” pin low, to indicate the high-side fault. The fault signal that is returned from the IXBD4411 is strictly for status; any gate-drive shutdown because of a high-side fault is done

Fig. 2: IXBD4411, high-side driver block diagram

Fig. 3: IXBD4410, low-side driver block diagram

Fig. 4: Logic representation of IXBD4410 FLT signal
locally within the high-side IXBD411. The IXBD4411 gate-drive will turn-off the power device whenever an overcurrent or under voltage condition arises. The overcurrent sensing is active only while the gate driver output is "high" (on). The overcurrent fault condition is latched and is reset on the next INH gate input positive transition. The FLT (pin 8) of the IXBD4411 is not used and should be grounded.

The low-side IXBD4410 driver provides an output pin 8 (FLT) to indicate a high-side (IXBD4411) or a low-side (IXBD4410) fault. This output pin is an "open-drain" output. The IXBD4410 low-side driver fault indications are similar to the IXBD4411 high-side driver indications as outlined above. A "graphic" logic diagram of the chipset's FLT function is presented in Fig. 4. Note that this diagram presents the logic of this function at the "low-side" IXBD4410 driver and is not the actual circuit. It describes the combined logic of the "fault logic" and "hi-side fault sense" blocks in both the IXBD4410 and IXBD4411 as shown in Fig. 2 and 3.

**IXBD4412/IXBD4413**

The basic, lower cost ISOSMART™ ICs: IXBD4412 (low-side driver) and the IXBD4413 (high-side driver). It operates similarly to the IXBD4410/4411 pair, but does not include the negative drive or the fault indications option. This pair requires only a single magnetics isolated transmission channel.

The most efficient method of providing power for the high-side driver is by bootstrapping. This method is illustrated in the functional drawing on page 4 and in the application example (Fig. 6 and 9) by diode D1 and capacitor C1. Using this method, the power is drawn through a high-voltage diode onto a reservoir capacitor whenever the floating high-side ground returns to near the real ground of the low-side driver; when the high-side gate is turned on, and the floating ground moves towards a higher potential, the bootstrapping diode back-biases, and the high-side driver draws its power solely from the reservoir capacitor. Power may also be provided via an isolated power supply (usually an extra secondary on the system housekeeping supply switching transformer).

Both the IXBD4410 and IXBD4411 contain on-board negative charge pumps to provide negative gate drive, which ensures turn-off of the high- or low-side power device in the presence of currents induced by power device Miller capaci- tance or from inductive ground transients. These charge pumps provide -5 V relative to the local driver ground when VDD is at +15 V, and at rated average currents of 25 mA. The charge pump requires two external capacitors (C7 and C11 in Fig. 6). The charge pump frequency is nominally 600 kHz. The charge pump clock is turned off whenever the difference between the VDD and VDD supplies exceed 20 V, to prevent exceeding the breakdown rating of the IC.

Both the IXBD4410 and IXBD4411 drivers possess two local grounds each, a common logic ground, and "Kelvin" ground. The Kelvin ground and logic grounds are first connected directly to each other, and then to the Kelvin-source of the power device for accurate overcurrent measurement in the presence of inductive transients on the power device source terminal.

Power MOSFET or IGBT overcurrent sensing utilizes an on-chip comparator with a typical 300 mV threshold. In a typical application, the current mirror pin of the Power MOSFET or IGBT is connected to a grounded, low-value resistor, and to the overcurrent comparator input on the high- or low-side driver. The comparator will respond typically within 150 ns to an overcurrent condition to shutdown the driver output. The power switches could be protected also by desaturation detection (see Fig. 6, 7 and 9).

To assure maximum protection for the phaseleg power devices, the chipset incorporates the following Power MOSFET and IGBT protection circuits:

- Power device overcurrent or desaturation protection. The IXBD4410/4411 or 4412/4413 will turn off the driver device within 150 ns of sensing an output overcurrent, or desaturation condition.

- Gate-drive lockout circuitry to prevent cross conduction (simultaneous conduction of the low- and high-side phaseleg power devices), either under normal operating conditions or when a fault occurs.

- During power-up, the chipset's gate-drive outputs will be low (off), until the voltage reaches the under-voltage trip point.

- Under-voltage gate-drive lockout on the low- and/or high-side driver whenever the respective positive power supply falls below 9.5 V typically.

- Under-voltage gate-drive lockout on the low- and high-side driver whenever the respective negative power supply rises above -3 V typically (IXBD4410/4411).

### Pin Description

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<tr>
<th>Sym.</th>
<th>Pin Description of IXBD 4410/4411</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>1 Positive power supply.</td>
</tr>
<tr>
<td>INL</td>
<td>2 Logic input signal referenced to LG (logic ground). In the IXBD4410, a &quot;high&quot; to this pin turns on its gate drive output and resets its fault logic. A &quot;low&quot; to this pin turns off the gate drive output. In the IXBD4411 this pin is not used and should be connected to its ground (LG). No Connection (IXBD 4411)</td>
</tr>
<tr>
<td>INH</td>
<td>3 Logic input signal referenced to LG (logic ground). In the IXBD4410, this signal is transmitted to the IXBD4411 &quot;high-side&quot; driver through pins 4 and 5 (T- and T+). A &quot;high&quot; to this pin turns on the IXBD4411 gate drive output and resets its fault logic. A &quot;low&quot; to this pin turns off the IXBD4411 gate drive output. In the IXBD4411 this pin is not used and should be connected to its ground (LG). No Connection (IXBD 4411)</td>
</tr>
<tr>
<td>T-</td>
<td>4 Transmitter output complemen-</td>
</tr>
<tr>
<td>T+</td>
<td>5ary drive signals. Direct drive of the low-side transformer, which is connected to the receiver of the chipset's companion device. In the IXBD4410, this signal transmits the on/off command to its companion IXBD4411. In the IXBD4411, this signal transmits the fault indication to its companion IXBD4410 driver.</td>
</tr>
<tr>
<td>R-</td>
<td>6 Receiver input complimentary</td>
</tr>
<tr>
<td>R+</td>
<td>7 signal. Directly connected to the corresponding transformer, which is driven by the chipset's companion device. In the IXBD4410, this signal receives the fault indication from its companion IXBD4411 driver. In the IXBD4411, this signal receives the on/off command from its companion IXBD4410 driver.</td>
</tr>
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### Sym. Pin Description of IXBD 4411/4412/4413

#### IXBD4411 (High-Side Driver)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LG</td>
<td>Logic and power ground.</td>
</tr>
<tr>
<td>KG</td>
<td>Kelvin ground. This ground is used as Kelvin connection for overcurrent or desaturation sensing.</td>
</tr>
<tr>
<td>CB</td>
<td>Capacitor terminals for negative charge pump (V&lt;sub&gt;EE&lt;/sub&gt;); &quot;+&quot; terminal is CB (pin 12).</td>
</tr>
<tr>
<td>CA</td>
<td>Negative supply terminal.</td>
</tr>
<tr>
<td>VEE</td>
<td>Gate drive output. In the IXBD4410 this output responds to the INL signal. A &quot;high&quot; at INL will turn it on (&quot;high&quot;), a &quot;low&quot; will turn it off (&quot;low&quot;). In the IXBD4411, this output responds to the transmitted signal from the companion IXBD4410. A &quot;high&quot; at INH of the IXBD4410 drives it will turn on (&quot;high&quot;). A &quot;low&quot; will turn it off (&quot;low&quot;). This output will turn off (&quot;low&quot;) also in response to any fault condition.</td>
</tr>
</tbody>
</table>

#### IXBD4412 (Low-Side Driver)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INL</td>
<td>Logic input signal referenced to GND. A &quot;high&quot; to this pin turns on the gate drive output and resets the fault logic. A &quot;low&quot; to this pin turns off the gate drive output.</td>
</tr>
<tr>
<td>INH</td>
<td>Logic input signal referenced to GND. A &quot;high&quot; to this pin is transmitted to the &quot;high-side&quot; driver (IXBD4413), turns on the &quot;high-side&quot; gate drive output and resets its fault logic. A &quot;low&quot; to this pin is transmitted to the &quot;high-side&quot; driver (IXBD4413) and turns off its gate drive output.</td>
</tr>
<tr>
<td>T-</td>
<td>Transmitter output complementary signal. Direct drive of the low signal transformer, which is connected to the receiver of the companion IXBD4413 &quot;high-side&quot; driver. This signal transmits the on/off command to the companion driver.</td>
</tr>
<tr>
<td>T+</td>
<td>Current sense or desaturation detection input. This input is active only while the OUT pin is &quot;low&quot; (off). This input is pulled to ground through a 70 Ω resistor. Any voltage at this pin above the threshold of 0.3 V typical will turn the output (pin 15) off. This pin is used for power device overcurrent protection.</td>
</tr>
</tbody>
</table>

#### IXBD4413 (High-Side Driver)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IM</td>
<td>Current sense or desaturation detection input. This input is active only while the OUT pin is &quot;high&quot; (on). When the OUT pin is &quot;low&quot; (off) this input is pulled to ground through a 70 Ω resistor. Any voltage at this pin, above the threshold of 0.3 V typical, will turn the output (pin 7) off. This pin is used for power device overcurrent protection.</td>
</tr>
<tr>
<td>GND</td>
<td>Logic and power ground.</td>
</tr>
<tr>
<td>OUT</td>
<td>Gate drive output. This output responds to the INL signal. A &quot;high&quot; at INL will turn it on (&quot;high&quot;), a &quot;low&quot; will turn it off (&quot;low&quot;). Any fault condition will also turn this output off (&quot;low&quot;).</td>
</tr>
<tr>
<td>VDD</td>
<td>Positive power supply.</td>
</tr>
</tbody>
</table>
Application

The IXBD4410/4411 or IXBD 4412/4413 chipset devices are specifically designed as MOS-gated transistor drivers in half-bridge power converters, 1- and 3-phase motor controls, and UPS applications. The phaseleg PWM command is normally generated by previous (user provided) circuitry. It must be decomposed into two separate logic signals, one for the high-side and one for the low-side power transistors, with appropriate deadtime for each state transition. The deadtime insures non-overlapping conduction even if the turn-on and turn-off delay times of the power devices are unequal. The minimum deadtime should be greater than $t_{dlh}$.

A separate circuit, or an IC device like the IXYS deadtime generator IXDP630, can be used to perform this function. The ISOSMART™ chipset family of devices do not generate deadtime, although there is an internal lockout that prohibits one device form being commanded "on" before the other is commanded "off". This simplifies start-up and shutdown protection circuitry, preventing logic error during power-up from turning on both high-and low-side transistors simultaneously.

Negative $V_{ee}$ Charge Pump Circuit Design

The on-chip $V_{ee}$ generator provided in the IXBD4410/4411 generates a negative power supply, regulated at 20 V below the positive $V_{dd}$ rail. (Note: this circuit is not present in the lower-cost IXBD4412/4413 chipset). If $V_{dd}$ is +10 V, $V_{ee}$ will be -10 V. If $V_{dd}$ is +15 V, $V_{ee}$ will be -5 V. This negative drive potential in the off-state is either desirable or required in many instances. When switching a clamped inductive load (Fig. 5), the turn-on of Q2 will commutate the freewheeling diode around Q1. Whether this diode is intrinsic (as in a MOSFET) or extrinsic (IGBT or bipolar), its reverse recovery is critical to proper circuit operation.

At high turn-on di/dt in Q2, and near its rated voltage, the recovery of D1 can get quite "snappy" (the di/dt in the second half of the recovery process, after the diode has begun to recover its blocking capability, can get very large), creating a very high dv/dt across Q1. This dv/dt is impressed across the Miller capacitance of Q1, forcing a large current to flow across the terminal of the device. If this current pulse causes a high enough voltage drop across the output impedance of the gate drive circuit, $R_{out}$, Q1 will be turned on.

The Q1 conduction in every instance Q2 is turned on (and Vice Versa), aside from degrading efficiency, can lead to catastrophic failure of both power transistors. At high temperature, where the -6 to -7 mV/°C temperature coefficient of IGBT/MOSFET threshold reduces the voltage required to create a failure, this problem is even more likely to occur. In an industrial module package (e.g.: a 150 A/1200 V IGBT phaseleg module), the series inductance contributed by the long gate leads and connectors further complicate the design.

Fig. 5: Switching a clamped inductive load

In a heavily snubbered converter, or in a power supply design with low transformer leakage inductance, the design problem is relatively simple and negative drive is seldom required. In these applications, the IXBD4412/4413 is adequate. However, in a modern snubberless or lightly snubber converter design, it is important to keep the gate drive impedance high enough during transistor turnoff to limit the reapplied dv/dt (the transistor is its own ‘active’ snubber). This is always important for EMI control, and in the case of IGBT may be required to achieve the necessary RBSOA. At the same time, it is mandatory to keep the off-state gate drive impedance very low to assure the transistor remain off during induced dv/dt (including diode recovery dv/dt). In some instances, it is simply not possible to satisfy both criteria with 0 V applied in the off-state. In these cases the IXBD4410/4411 with $V_{ee}$ negative bias generator must be used.

The internal $V_{ee}$ generator is a charge pump circuit. Referring to Fig. 6, an external charge pump capacitor is required between the CA and CB.
terminals (C7, C11), and an output reservoir capacitor between VEE and GND (C10, C14). A 0.1 µF charge pump capacitor (C7, C11) is recommended. The voltage regulation method used in the IXBD4410/4411 allows a 1 to 2 V ripple frequency depends on the size of the V<sub>EE</sub> output reservoir capacitor (C10, C14) and the average load current. The minimum recommended output reservoir capacitor (C10, C14) is 4.7 µF tantalum, or 10 µF if aluminium electrolytic construction is chosen. Note that this reservoir capacitor is in addition to a good quality high frequency bypass capacitor (0.1 µF) that should be placed from VEE to GND (C9, C13).

A small resistor in series with the charge pump capacitor, (R7, R8) reduces the peak charging currents of the charge pump. A value of 68 Ω or greater is recommended, as illustrated in the applications example in Fig. 6.

Current Sense / Desaturation Detection Circuit

All members of the ISOSMART™ driver family provide a very flexible overcurrent/short circuit protection capability that works with both standard three-terminal power transistors, and with 4- and 5-terminal current sensing power devices. Overcurrent detection is accomplished as illustrated in Fig. 7a (for a current mirror power device) and Fig. 7b (for a standard three terminal power transistor). Desaturation detection is accomplished with the same internal circuits by measuring the voltage across the power transistor in the on-state with an external resistor divider (Fig. 7c).

The IM input trip point V<sub>IM</sub>, typically 300 mV, is referenced to the Kelvin ground pin KG.

Current Mirror MOSFET and IGBT devices allow good control of peak let-thru currents and excellent short circuit protection when combined with the ISOSMART™ driver family of devices. The sense resistor is chosen to develop 300 mV at the desired peak transistor current, assuming a trip point of 30 A is desired:

\[
R_s = \frac{300 \text{ mV}}{30 \text{ A}} = 10 \text{ mΩ}
\]

It is important to realize that C<sub>oss</sub> per unit area of the mirror cells is much larger that C<sub>oss</sub> per unit area of the bulk of the chip (due to periphery effects). This causes a large transient current pulse at the mirror output whenever the transistor switches (C • dv/dt currents), which can cause false overcurrent trigger. The RC filter indicated in Fig. 7a will eliminate this problem.

Standard three-terminal MOSFET and IGBT devices in discrete as well as modern industrial single transistor and phaseleg modules) can also be protected from short circuit with the ISOSMART™ driver family devices. In discrete device designs, where the source/emitter terminal is available, overcurrent protection with an external power resistor can be implemented. The resistor is placed in series with the device emitter, with the full device current flowing through it (Fig. 7b). The sense resistor is again selected to develop 300 mV at the desired peak transistor current, assuming a trip point of 30 A is desired:

\[
R_s = \frac{300 \text{ mV}}{30 \text{ A}} = 10 \text{ mΩ}
\]

It is important to recognize that “non-inductive” is a relative term, especially when applied to current sense resistor construction and characterization. There is always significant series inductance inserted with the sense resistor, and L • di/dt voltage transients can cause false overcurrent trigger.

The RC filter indicated in Figure 7b will eliminate this problem. Choosing the RC pole at the current sense resistor RL zero should exactly compensate for series inductance. Because the exact value is not normally known (and can vary depending on PC layout and component lead dress) this is not normally a good idea. Usually, the RC time constant should be two to ten times longer than the suspected RL time constant.

Desaturation detection as in Figure 7c is probably the most common method of short circuit protection in use today. While not strictly an “overcurrent” detector, if the power transistor gain, and consequently short circuit let-thru current, is well controlled (as with modern MOSFET and IGBT) this methodology offers very effective protection.

Both the IXBD4410/4411 one-phase (half-bridge) circuits in Fig. 6 and the IXBD4412/4413 circuit in Fig. 9 uses desaturation detection. In Fig. 8, the voltage across the two Power MOSFET devices (or IGBTs) are monitored by two sets of voltage-divider networks, R10 and R13 for the high-side gate driver, and R13 and R14 for the low-side gate driver. The dividers are set to trip the IM input comparators when either Power MOSFET device V<sub>DS</sub> exceeds a reasonable value, perhaps 50 V (usually a value of 10 % of the nominal DC bus voltage works well). R10 or R13 are chosen to tolerate the applied steady state DC bus voltage at an acceptable power dissipation. Dielectric withstand capability, power handling, temperature rise, and PC board creep and strike spacings, must all be carefully considered in the design of the voltage-divider networks.

In the off-state, the voltage across the Power MOSFET device may go as high as the DC bus potential. To keep this normal condition from setting the internal fault flip-flop of the IXBD4410 or the IXBD4411, an internal CMOS switch is turned on and placed across IM and KG pins shorting them together. This effectively discharges C8 or C12 in Fig. 6 and maintains zero potential with respect to KG at IM.
When the command arrives to switch on the Power MOSFET device, the CMOS switch shorting IM to KG is turned off. The driven Power MOSFET device is switched on approximately 100 ns to 1 µs later, and with typical load conditions, its drain-to-source potential, $V_{DS}$, may take an additional 10 µs of delay to collapse to the normal on-state voltage level. To prevent false triggering due to this, C8 or C12 in parallel combination with R10 and R11, or R13 and R14, delays the IM input signal. During this turn-on interval, the voltage across C8 or C12 will rise until the Power MOSFET device finally comes on and pulls the voltage across C8 or C12 back down. If the MOSFET device load circuit is shorted, its $V_{DS}$ voltage cannot collapse at turn-on. In this case, the voltage across C8 or C12 rises rapidly until it reaches 300 mV, tripping the fault flip-flop and shutting down the driver output. To prevent false triggering, C8 or C12 in parallel combination with R10 and R11, or R13 and R14, delays the IM input signal.

Three Phase Motor Controls

Fig. 8 is a block diagram of a typical 3-phase PWM voltage-source inverter motor control. The power circuit consists of six power switching transistors with freewheeling diodes around each of them. The control function may be performed digitally by a microprocessor, microcontroller, DSP chip, or user custom IC; or it may be performed by a PC board full of random logic and analog circuits. In any of these cases, the PWM command for all six power transistors is generated in one circuit, and this circuit is usually referred to system ground potential - the bottom terminal of the power bridge.

The ISOSMART™ family of drivers is the interface between the world of control logic and the world of power, 5 V input logic commands precisely control actions at high voltage and current (1200 V and 100 A in a typical application). Fig. 6 is a detailed schematic of one phase of three 3-phase motor control, showing the interconnection of the IXBD4410/4411 and its associated circuitry. This application utilizes the full feature set of the IXBD4410/4411 family of devices in a 460 V–line operated inverter. In situations that would not benefit from the negative gate drive, and do not require the fault status output, the IXBD4412/4413 chipset may prove adequate. Fig. 9 is a complete schematic of one phase of a 3-phase inverter using the lower cost IXBD4412/4413 chipset. Notice the reduction in total parts count. With the smaller 8-pin packages of the devices themselves, the IXBD4412/4413 chipset offers a 70 % reduction in PC board real estate for a modest reduction in feature set compared to the IXBD4410/4411 devices.

PCB Layout Considerations

The IXBD4410/4411 or IXBD4412/4413 is intended to be used in high voltage, high speed, high dv/dt applications.

To ensure proper operation, great care must be taken in layouting the printed circuit board. The layout critical areas include the communication links, current sense, gate drive, and supply bypassing. The communication path should be as short as possible. Added inductance disturbs the frequency response of the signal path, and these distortions may cause false triggering in the receiver. The transformer should be placed between the two ICs with the orientation of one IC reversed (Fig. 10).

 capacitance between the high- and low-side should be minimized. No signal trace should run underneath the communication path, and high- and low-side traces should be separated on the PCB. The dv/dt of the high-side during power stage switching may cause false logic transitions in low-side circuits due to capacitive coupling. The low signal pulse transformer provides the isolation between high-and

![Fig. 8: Typical 3-phase motor control system block diagram](image)

![Fig. 9: Lower cost IXBD4412/4413 single phase circuit with deadtime generator IXDP630](image)
low-side circuits. For 460 V line operation, a spacing of 4 mm is recommended between low- and high-side circuits, and a transformer HIPOT specification of at least 1500 V is required. This creep spacing is usually adequate to control leakage currents on the PCB with up to 1200 V applied after 10 to 15 years of accumulated dust and particulates in a standard industrial environment. In other environments, or at other line voltages, this spacing should be appropriately modified.

Power Circuit Noise Considerations

In a typical transistor inverter, the output MOSFET may switch on or off with di/dt >500 A/µs. Referring to Fig. 11 and assuming that the MOSFET source terminal has a one inch path on the PCB to system ground, a voltage as high as \( V = 27 \text{ nH} \times 500 \text{ A/µs} = 13.5 \text{ V} \) can be developed. If the MOSFET switched 25 A, the transient will last as long as (25/500) µs or 50 ns, which is more than the typical 6 or 7 ns propagations or of a 74HC series gate.

![Fig. 10: Suggested IC Orientation](image)

The current sense/desaturation detect input is noise sensitive. The 300 mV trip point is referred to the KG (Kelvin ground) pin, and the applied signal must be kept as clean as possible. A filter is recommended, preferably a monolithic ceramic capacitor placed close to the IC as possible directly between IM and KG. To preserve maximum noise immunity, the KG pin should first be connected directly to the LG pin, and the pair then sent directly to the power transistor source/emitter terminal, or (if a desaturation detection circuit is used) to the bottom of the divider resistor chain.

All supply pins must be bypassed with a low impedance capacitor (preferably monolithic ceramic construction) with minimum lead length. The output driver stage draws 2 A (typical) currents during transitions at di/dt values in excess of 100 A/µs. Supply line inductance will cause supply and ground bounce on the chip that can cause problems (logic oscillations and, in severe cases, possible latchup failure) without proper bypassing. These bypass elements are in addition to the reservoir capacitors required for the negative Vee supply and the high-side bootstrapped supply if these features are used.

![Fig. 11: Potential layout problems that create functional problems](image)

Three traces while positioning the transistors next to their heat sink and meeting UL/VDE voltage spacings is just too difficult.

Grounding the gate driver as in option (a) in Fig. 11 solves the MOSFET turn on problem by eliminating LS1 from the source feedback loop. Now, unfortunately, the gate driver will oscillate every time it is turned on or off. As the IXDP630 output goes "high", the gate drive output follows (after its propagation delay) and the MOSFET starts to conduct. The voltage transient induced across LS1 \( V = LS1 \times di/dt \) raises the local ground (point a) until it exceeds \( V_{LS1} \) \( (630) - V_{il} (4410/4412) \) and the driver (after its propagation delay) turns the MOSFET off. Now the MOSFET current falls, \( V(LS1) \) drops, point (a) drops to system ground (or slightly below), and the driver detects a "1" at its input. After its propagation delay, it again turns the MOSFET on, continuing the oscillation for one more cycle.

To eliminate this problem, a ground level transformation circuit must be added, that rejects this common mode transient. The simplest is a de-coupling circuit, also illustrated in Fig. 11. The capacitor voltage \( C_{il} \) remains constant while the transient voltage is dropped across \( R_s \) and the driver detects no input transition, eliminating the oscillation. This circuit does add significantly to turn-on and turn-off delay time, and cannot be used if the transient lasts longer than the allowable delays. Delay times must be considered in selection of system dead time.

The most complex (and most effective) method of eliminating the effects of transients between grounds is isolation.
Optocouplers and pulse transformers are the most commonly used isolation techniques, and work very well in this case. The IXDP630/631 has been specifically designed to directly drive a high speed optocoupler like the Hewlett Packard HCPL22XX family or the General Instrument 740L60XX opticologic family. These optos are especially well suited to motor control and power conversion equipment due to their very high common mode dv/dt rejection capabilities.

Transformer Considerations

The transformer is the communication link and isolation barrier between the high- and low-side ICs. The high-side gate and fault signals are transmitted through the transformer while maintaining the proper isolation. The transmitter signal is in the form of a square wave, but the receiver responds only to the logic edges. This allows for much smaller transformer designs, since a 10 kHz switching frequency does not require a 10 kHz pulse transformer.

The recommended ferrite bead is Fair Rite Products' part number 2661000101. It is manufactured by:

Fair-Rite Products Corp.
Wallkill, NY
Phone: (914) 895-2055

Several transformer manufacturers have produced custom transformers for the IXBD4410/4411 and IXBD4412/4413 chip set, to the above specifications:

1) 12 Pin DIP outline-
   Part Number 500 - 1914
   BH Electronics
   Buinville, MN
   Phone: (612) 894-9690

2) 8 Pin DIP outline-
   Part Number 23Z129
   Fil-Mag
   San Diego, CA
   Phone: (619) 569-6577

3) Transformer, type 23Z119 for IXBD4412/4413 and 23Z129 for IXBD4410/4411
   FEE, Rodgau/Germany
   Phone: +49-6106-2011
   Fax: +49-6106-24286

As seen in the application drawings (Fig. 6, 9 and 13) a coupling capacitor (22 nF) and a damping resistor (22 Ω) are added in series with the primary side of the transformer. The capacitor will control the small amount of energy needed to transfer the signal to the companion driver. The resistor will control the damping of the signal and limit the peak transmitter output current. The receiver is designed to operate over a wide common mode input range. To reduce noise pickup, the receiver has ±250 mV of input hysteresis.

If the signal is being distorted at the transmitter, the transmitter is probably running into current limit. A decrease in the coupling capacitance or an increase in the damping resistance should solve this problem. The receiver operates over a wide input range. The minimum amplitude for one side of the receiver is about 1 V and a maximum of about 3 V. It is critical that there be no overshoot on the transformer secondary waveform. Each signal should be slightly overdamped. If significant overshoot exists, the received signal may be logically inverted. An increase of the damping resistor will solve this problem.

The nominal electrical specifications of the transformer are as follows:
- Open circuit inductance (100 kHz; 20 mV): 3 μH
- Intertwinding capacitance: 2 pF
- Primary leakage inductance: 0.1 μH
- Turns ratio: 6:2
- Primary-to-secondary isolation (1min): 1500 V~
- Core permeability (μi): 125

The recommended coupling capacitor is a 22 nF and a 22 Ω damping resistor. The receiver is designed to operate over a wide input range. The minimum amplitude for one side of the receiver is about 1 V and a maximum of about 3 V. It is critical that there be no overshoot on the transformer secondary waveform. Each signal should be slightly overdamped. If significant overshoot exists, the received signal may be logically inverted. An increase of the damping resistor will solve this problem.

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The recommended transformer for this ISOSMART™ driver chipset is fabricated using a very small ferrite shield bead (see Fig. 12), onto which a six-turn primary and a two-turn secondary winding of 38 AWG magnet wire are made. The two windings are segment wound to achieve primary-to-secondary isolation of up to 2500 V~. The six-turn primaries are connected to the respective IXBD4410/4411 transmitter outputs and the two-turn secondaries are connected to their respective receiver inputs.

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