Failure Analysis of Tungsten Stud Defects from the CMP Process

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Abstract

This paper describes a failure analysis that effectively combined multiple analytic techniques to find the cause of I/O leakage in a flawed chip produced for an OEM (Original Equipment Manufacturer) product. Internal probing was initially used for defect isolation and a Tungsten (W) stud open circuit flaw was isolated by electrical characterization with internal probing. SEM (Scanning Electron Microscopy), TEM (Transmission Electron Microscopy, and FE-AES (Field Emission Auger Electron Spectroscopy) analysis with FIB (Focused Ion Beam) preparation were used for physical analysis. Cross-sectional SEM and TEM observations showed a gap with foreign material (FM) between the bottom of the metal line and the top of the W stud, possibly from the W CMP (chemical mechanical polish) process. FE-AES is effective for the analysis of light materials and their chemical composition, so a flat milling FIB process was used to prepare a cross-section for FE-AES analysis of the FM and the interfaces of the open defect. The spectra showed that the FM was traceable to the W CMP process. From these analytical results and problem reproduction experiments in the W CMP process on the manufacturing line, the failure mechanism was identified.

Introduction

Failure analysis is very important to improve and maintain production yield in manufacturing lines, because low yield wastes production resources and decreases business profits. Quick and accurate feedback from analysis to manufacturing lines is necessary in order to take corrective actions. Failure analysis generally involves two steps.

The first step is to localize a defect. Electrical analysis such as electrical diagnosis, EMS (emission microscopy), OBIC (optical beam induced current) technique, LCT (liquid crystal technique), internal probing and so on are used for defect localization.

The second step is physical analysis of the defect. SEM, TEM, FE-AES, FIB, and SIMS (secondary ion mass spectroscopy) are used for physical analysis. The mentioned analytical techniques are useful by themselves, but when they are combined, they become more effective.

One of the most important goals of failure analysis is to determine the root cause of failure. This paper describes the effectiveness of these combined analysis techniques to analyze the I/O leakage failure of the OEM product, leading to the correct conclusion.

Failure Description

The problem was low yield of the OEM product. The main features were 0.5 um design rules, single poly-Si with W silicide and 4 layers of metallurgy. Also CMP technology was used for each interconnect layer. According to electrical diagnostic result from an LSI tester, the detected failures showed up in the following categories: Functional failures, I_{DD} (power supply current) leakage failures, and I/O leakage failures.

It was necessary to perform failure analysis, and feedback to the manufacturing line was desired as soon as possible. However, analysis of the functional failure or I_{DD} leakage failure might be very difficult, because there was a lot of process information but relatively little design information. Since it seemed that the same root cause led to all three failures, we tried to analyze the I/O leakage failure, because the I/O circuits were simpler than the others.

Defect Isolation

There are three types of I/O that can be performed (Input, Output and Common input/output). We decided to analyze the input circuit, because this circuit is simpler than the output or common input/output circuits. Figure 1 is the schematic of the input circuit. It has two V_{DD} (power supply voltage) inputs labeled V_1 and V_2. V_1 is a power supply for the protective devices, and V_2 is for the receiver circuits and internal LSI logic. An input line from the pad is connected to the gates of a receiver circuit through protective devices.

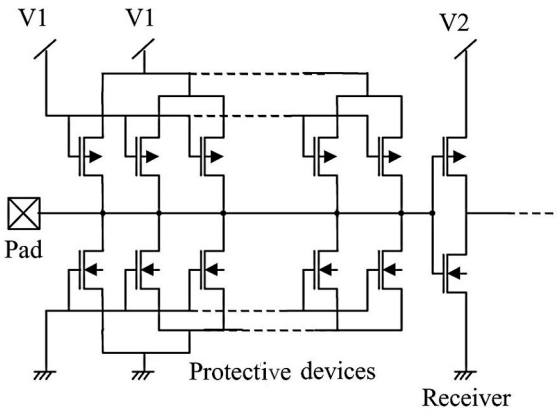

Figure.1 Schematic of Input

Electrical Characterization

I/O leakage measurement from Pad

Electrical characterization at pad level was done to verify the I/O leakage failures. Figure 2 shows the I/O leakage for the same conditions as the LSI tester measurements. The conditions are shown in Table 1. The leakage value was same as measured with the LSI tester.

Figure 3 shows the characteristics of pad-GND, which is normal and figure 4 shows the characteristic of pad-V_1, which has a short.

From these results, the following modes were considered most likely as the cause of the input leakage:

1) A short between an input pad and V_1
2) A leakage path from input pad to V_1 through a P-FET of one of the protective devices

Table 1 I/O leakage measurement

I/O leakage measurement condition	
V1	3.5 V
V2	3.5 V
GND	0 V
VP (Voltage applied to the pad.)	0 V to 3.5 V (sweep)
measurement result	
IP(leakage corrent)= -1.27 mA / VP=0 V	

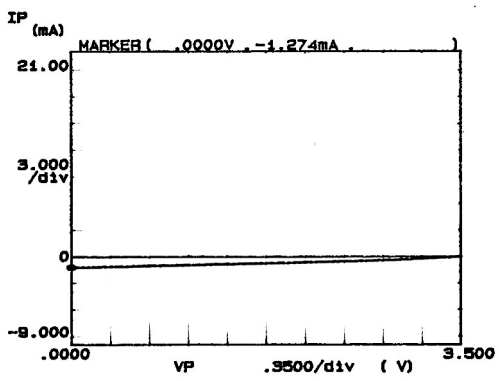

Figure.2 I/O leakage at pad

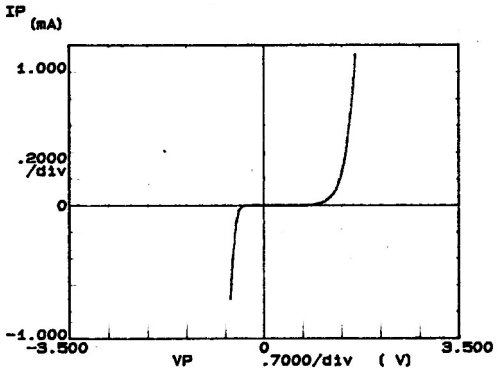

Figure.3 Pad – GND characteristic VP = -3.5 V to 3.5 V (sweep)

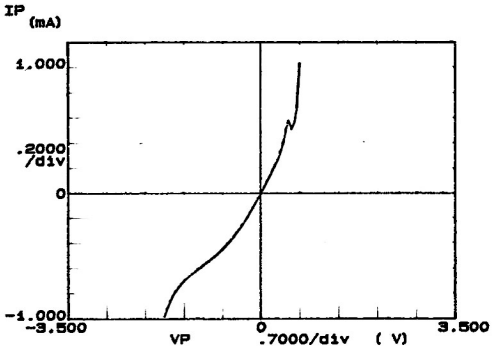

Figure.4 Pad – V1 characteristic VP = -3.5 V to 3.5 V (sweep)

Planar Polishing and Internal Probing

Optical observations with planar polishing made clear that M_4, M_3, M_2 and M_1 were normal. There was no short between the input line and the V_1 line. The cause of the failure was suspected to be leakage through a P-FET of one of the protective devices. The connections of the input circuit were analyzed.

Figures 5 and 6 show the M_1 level optical image of the input circuits. Figure 7 shows the optical image of the P-FET after M_1 was removed. Figure 8 is the schematic of input circuit that was composed of M_1

and a poly-Si gate. At the M_1 level, the common source of the P-FETs can be divided into several sources, and most of the P-FETs are connected in parallel in pairs except at each end.

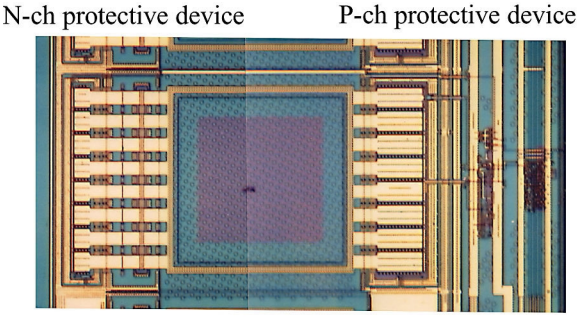

Figure.5 Optical image of Input after M2 removal

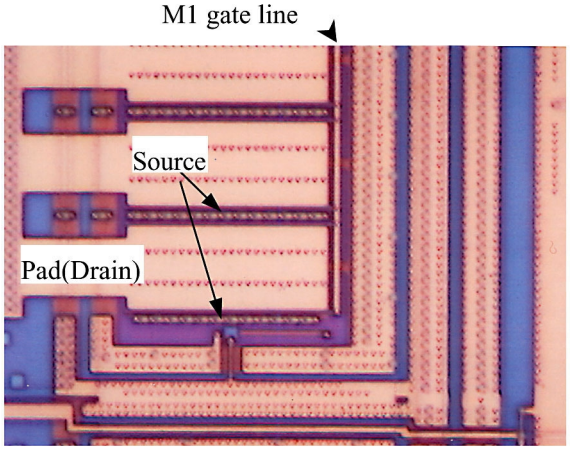

Figure.6 Optical image of Input after M2 removal (higher mag.)

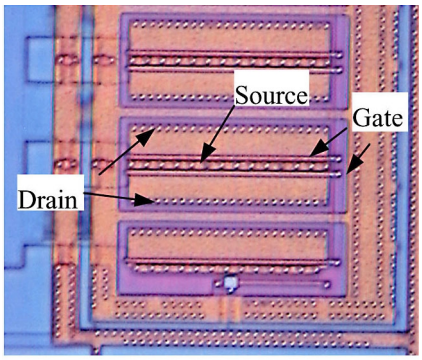

Figure.7 Optical image of P-FET after M1 removal

The static characteristics of each P-FET pair were measured one by one with internal probing. Figures 9, 10 and 11 show the measurement results. The conditions of the measurements are shown in Table 2.

Current through a good P-FET pair is shown in Figure 9. It is twice as much as from a single P-FET, which is shown in Figure 10. However, for a bad P-FET pair, as shown in Figure 11, the current flow is only half the current of a good P-FET pair. To sum it up, the current of the failed P-FET pair is equal to a single P-FET. This result reveals that one gate of the bad P-FET pair did not turn 'on'.

This indicated that a floating gate caused the input leakage failure, and it was suspected that the cause of the floating gate was an open W stud defect, where the stud connects M_1 to the gate.

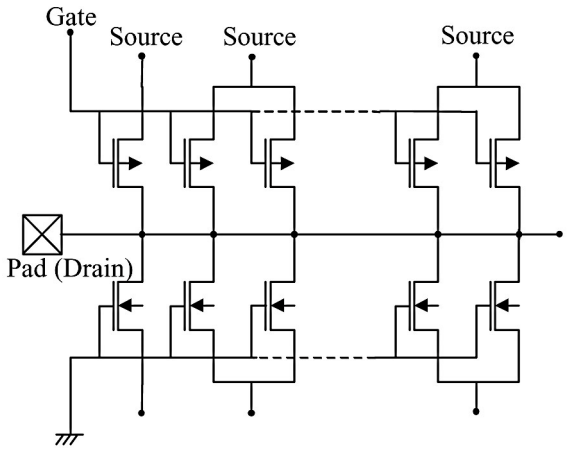

Figure.8 Schematic of Input at M1 level

Table 2 Static characteristic of P-FET

Measurement condition	
VS, VNW	0 V
GND	0 V
VDS	0 V to -3.5 V sweep
VG	0 V to -3 V /-1V step
Measurement results	
Circuit	**ID**
Good P-FET pair	-11.2mA
good single P-FET	- 5.8mA
Fail P-FET pair	- 6mA

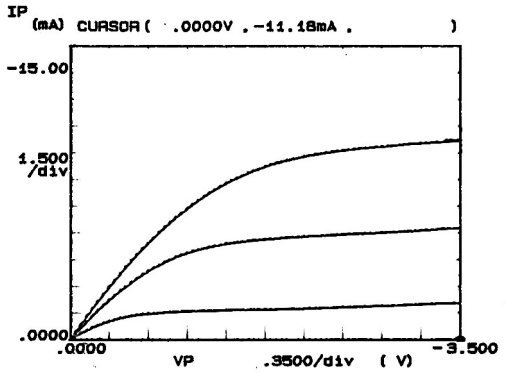

Figure.9 Static characteristic of good P-FET pair

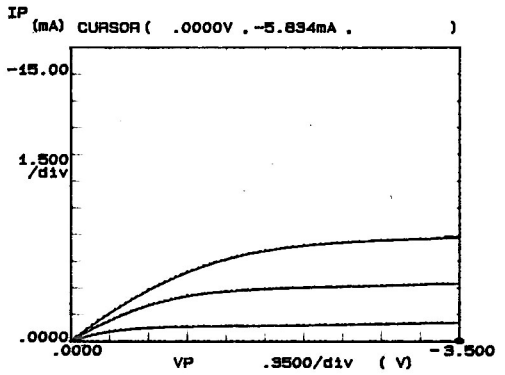

Figure.10 Static characteristic of single P-FET

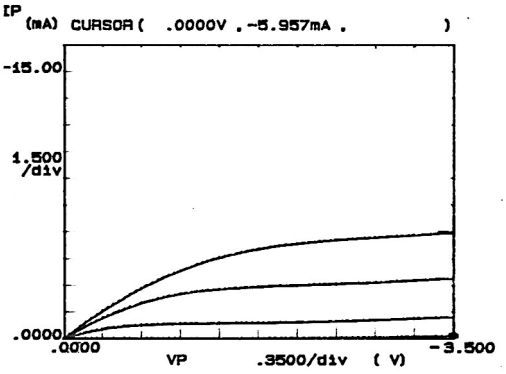

Figure.11 Static characteristic of fail P-FET pair

Cross-sectional Observation (SEM)

A cross-sectional SEM image of the suspicious contacts was made to confirm the open defect. The sample was prepared by mechanical polishing.

Figure 12 shows the result. It was found that there was a space between the bottom of M_1 and the top of the W stud. Part of the space was filled with FM, which from its contrast seems to be an organic material. This result made it clear that one of the suspicious contacts was open and this caused the gate to float, but it was unclear whether the FM was originally inside the space or if it was debris from the mechanical polishing.

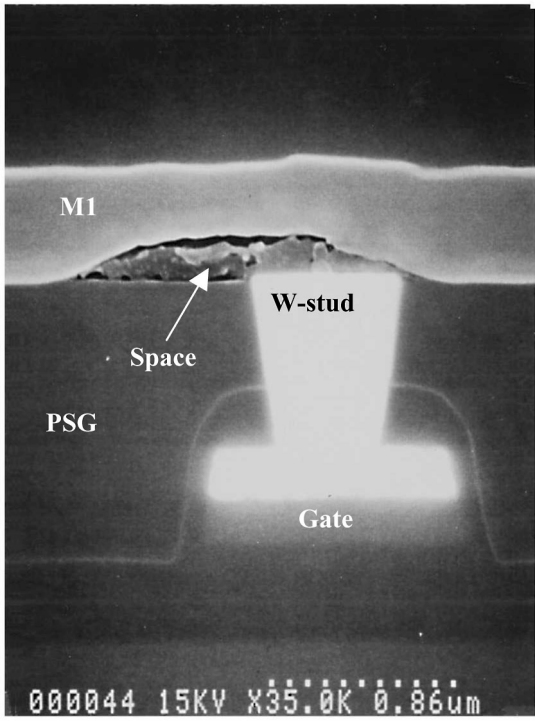

Fig.12 Cross sectional SEM observation

Fig.12 Cross sectional SEM observation

Detailed Cross-sectional Observation (TEM)

Another open stud was isolated using the same method. This time a TEM specimen was prepared by using FIB to examine a cross-section without artifacts from mechanical polishing. Figure 13 shows the image of a gap. There was a gap at the interface between the Ti liner of M_1 and the W stud, and the FM was clearly observed inside the space. The Aluminum (Al) grains and Al_3Ti grains appeared normal. From these results, it seemed that the open was traceable to the W CMP process.

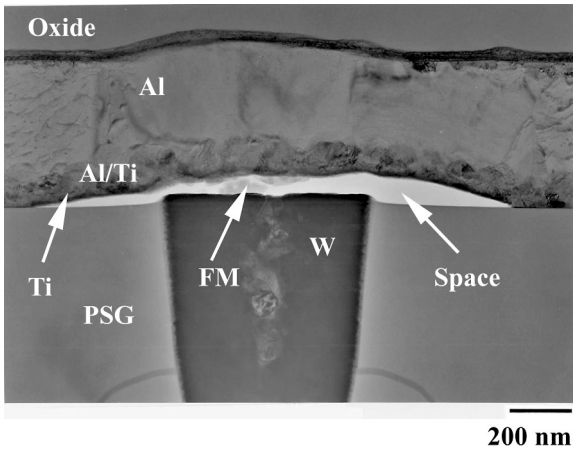

Figure.13 Cross sectional TEM observation

W CMP Process Description

Following are the process steps of the W CMP process. Figure 14 shows a schematic view of each step in W-CMP.

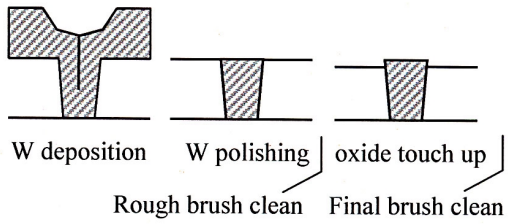

Fig.14 Schematic of cross sectional W-studs explaining W-CMP process

1. W polishing: Polishing W by CMP (Chemical Mechanical Polishing)
2. Rough brush cleaning: Cleaning with an organic brush after W polishing
3. Oxide touch up: Polishing only oxide adhering to W studs
4. Final brush cleaning: Final cleaning with organic brush

FE-AES Analysis of Cross-section Using FIB Preparation

FE-AES analysis was performed with an FIB cross-sectional preparation to clarify the composition of the FM. FE-AES can do elemental analysis and detects changes in chemical composition with high spatial resolution [(x,y,d); (20 nm, 20 nm, 20 Å)]. Another open stud was isolated using the same methods as before. A fresh cross-section of the gap was necessary for accurate chemical analysis. For accuracy, it is also important to detect sufficient numbers of Auger electrons from a sample. Therefore, a large cross-section including the open stud was prepared by FIB milling. The cross-sectional SEM image made using FE-AES is shown in Figure 15. The specimen was tilted at fifty degrees. An Auger survey spectra was obtained from the cross sectional surface of the FM after Ar sputter cleaning. The survey spectrum is shown in Figure 16. Oxygen (O), carbon (C), phosphorus (P), silicon (Si), Al, Ti and W were detected.

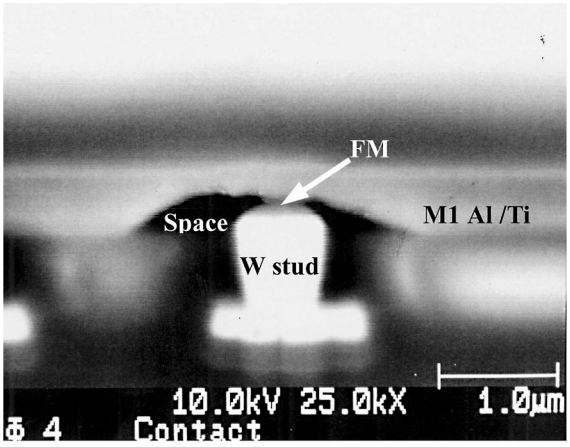

Figure.15 Cross sectional SEM Image of the open stud by FE-AES (tilted at 50 degrees)

Note: A allow indicats the FE-AES analysis point.

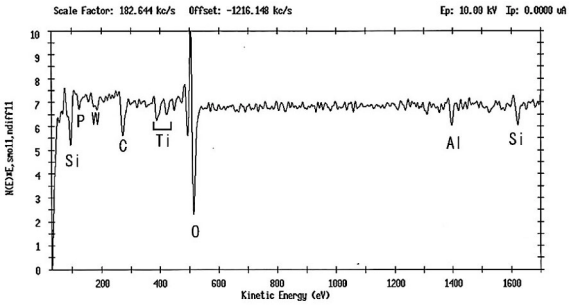

Figure.16 FE-AES survey spectra at the surface of the FM

Considering the high spatial resolution of FE-AES, there was little likelihood of detecting Auger electrons that were generated from elements located far from the analysis point. However, Al, Ti, W can be ignored, because they are the materials of the metal lines themselves. Therefore, O, C, P, and Si were considered to be the elements making up the FM.

FE-AES Analysis at the Interfaces Using FIB flat milling preparation

It was necessary to perform an FE-AES survey analysis at the interfaces to verify the result of the cross sectional FE-AES analysis. Therefore, another open stud was isolated in the same way as before. M_2 was polished off and the surface of the specimen was an interlayer of dielectric film on M_1. If argon (Ar) sputtering with FE-AES is applied for a long time to mill the dielectric film down to the M_1 interface, the sputtered surface becomes rough, and the Auger spectra at the interface loses its clearness and accuracy. In that condition, it is also impossible to analyze very small areas. To avoid these problems, FIB's flat and wide milling technique was used down to the middle of M_1.

Figure 17 shows the SEM image obtained by FE-AES after FIB milling. Stud #1 shows at higher contrast than Stud #2. It seemed that Stud #1 was observed through M_1 and the gap.

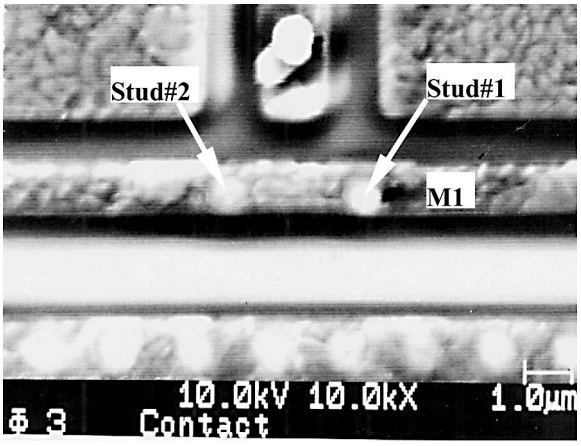

Figure.17 SEM image by FE-AES

Note: Arrows indicate the FE-AES analysis point.

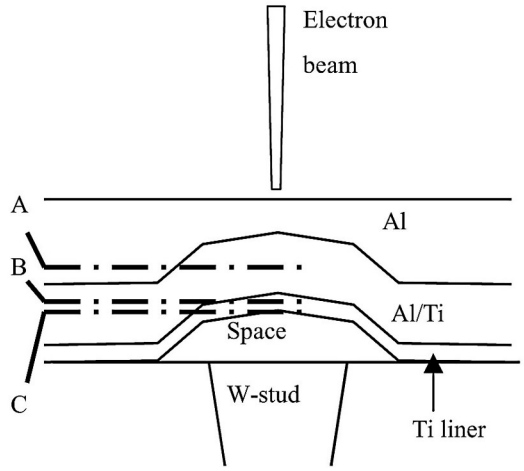

Figure.18 Schematic of cross section at Stud #1

Notes: line A,B,C indicate the analyzed Interfaces.

The analyzed interfaces are shown in Figure 18. Figures 19, 20, and 21 show the Auger survey spectra as each interface was exposed through Ar sputtering. Checking the spectra against structure of the metal line (M_1), it was clear that the Al and Ti peaks were taken from the material of the metal line. When the Ti peak began to decrease, O, C, P, Si, and W peaks began to appear, and in particular the O peak was very strong. These elements must not exist in the interfaces. The Auger chemical analysis also showed a shift of the Al peak at this time. It was clear that Al oxide, O, C, P, and Si surely existed at the interface between the Ti liner and the space above the W stud. This result agreed with the cross-sectional FE-AES analysis result. The FM was composed of organic material, aluminum oxide, phosphorus compound, and Silicon compounds. These materials seemed to be traceable to the slurry and brushes used in the W CMP process.

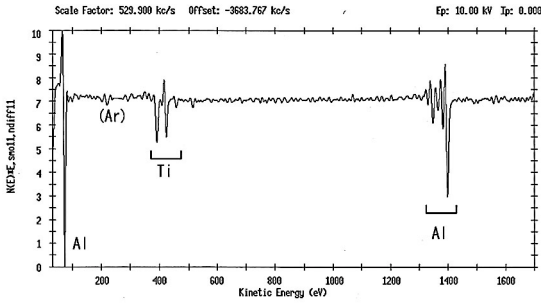

Figure.19 Auger survey spectra at interface A

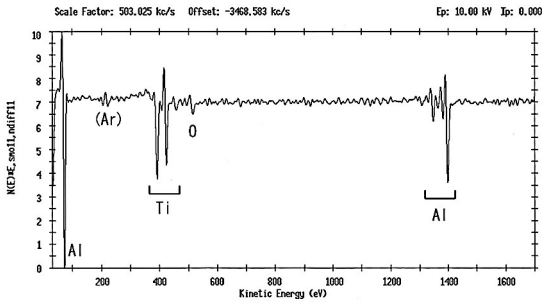

Figure.20 Auger survey spectra at interface B

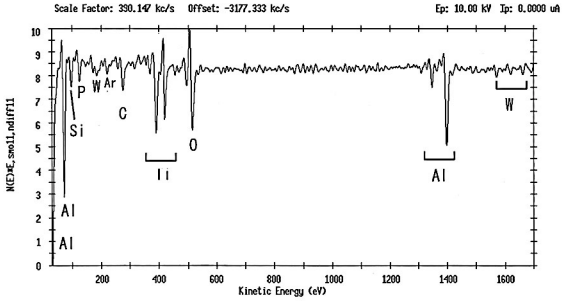

Fig.21 Auger survey spectra at interface C

Reproduction experiments on W-CMP process

Problem reproduction experiments and inspections were performed on the W CMP process in the manufacturing line after the failure analysis results had been fed back into the process. It was determined that the unexpected chemical reactants were adhered to the raised edge between the W studs and PSG during the oxide touch up process. It was also found that when the oxide touch up step took more time, more reactants were stuck to the wafer. An SEM image of the excess reactant chemical is shown in Figure 22. An FE-AES spectrum of the reactant is shown in Figure 23. Although the electrical charge-up process disturbed the obtained Auger spectra, O and C were certainly detected from the surface of the reactant. This confirmed that the reactant consisted of organic materials, in agreement with the earlier failure analysis results.

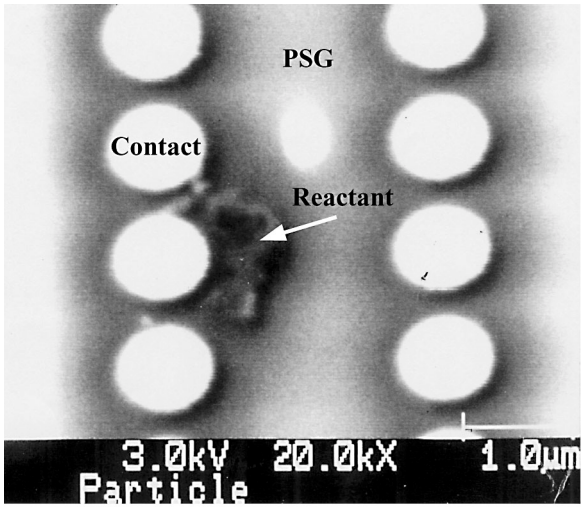

Figure.22 SEM image of the reactant

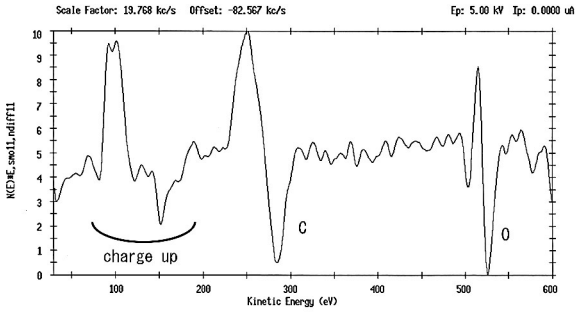

Fig.23 FE-AES spectra at the surface of the reactant

Summary

The I/O leakage failures were caused by floating gates, specifically by open W studs. Cross-sectional SEM and TEM observations showed gaps between the M_1 Ti liner and the W studs. FM was found inside the gap. The FIB process was used for sample preparation, so that cross-sectional and planar FE-AES analyses could be used to identify the elements of the FM. Problem reproduction and inspection in the W-CMP process confirmed that chemical reactants containing organic matters were stuck around contacts during the oxide touch up process.

These results revealed that the W-stud open faults were traceable to the chemical reactants that stuck to uneven edge between the W studs and the PSG film during the oxide touch up process. The composition of the reactants was identified to be slurry, PSG debris, and organic materials such as brush fibers. The root cause of the stud open failures had been identified.

The mechanism producing the open W studs was to postulated to be as follows: Leftover reactants remained on the uneven edge between the W stud and the PSG during the W CMP process. Gas was generated from condensation and degeneration of the reactants during subsequent thermal processes. The M_1 layer was pushed up by the gas, forming the gaps that caused the stud to be disconnected.

The analysis results were fed back into the W CMP sector. As a result ,the material of the cleaning brushes was changed from nylon to PVA (polyvinyl acetate), and the oxide removal quantity was reduced. The process yield had been improved by these actions, showing that the open stud defects were the main cause of the low yield.

Conclusion

I/O leakage analysis using various analytical instruments was able to reveal the root cause of yield problems, which turned out to be in the W CMP process for this component. The failure mechanism was discovered using of FE-AES on samples prepared using FIB to achieve high accuracy of elemental analysis in microscopic areas.

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