Integrated Circuit SNR improvement using Dielectric Altering Compound, Laser Trim, and FIB system.

B.J. Dutt, J.J. Kroutch, Jr., K.N. Hooghan, R.J. Jenkins, M.J. Toth
Lucent Technologies, Allentown, Pennsylvania, U.S.A.

Abstract

Communication Signal Processors (CSP) did not have the Signal-to-noise ratio (SNR) performance expected. Significant differences were noticed between SNR values at wafer level and package testing.

The analog section of the chip was suspected to be the culprit as the problem existed at the analog to digital conversion level. A Dielectric Altering Compound (DiAC) was chosen to simulate the packaged environment in decapsulated parts[1]. The DiAC was applied in and around the analog section, after application in other areas did not show the SNR degradation.

The sampling capacitors in the A to D Converter section (ADC) were selectively coated with DiAC and laser trimmed to identify the offending circuit element. A signal trace running adjacent to the sampling caps, was isolated and suspected of coupling noise to the sampling caps.

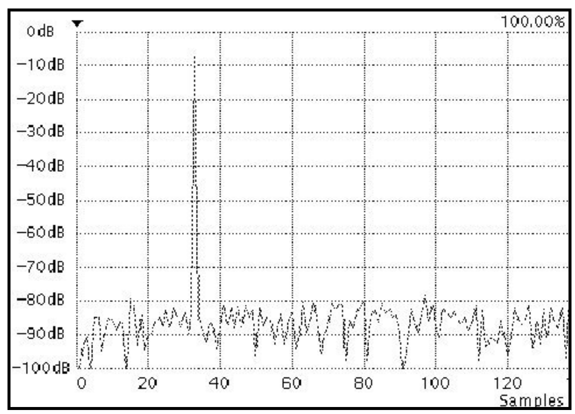
A FIB system was used to deposit a grounded metal shield that covered the suspect runner on a packaged part - subsequent testing showed no degradation.

The above procedure was successful in isolating, verifying, and rectifying the SNR degradation. The SNR degradation was found on more than one code. The same procedure was used repeatedly on subsequent errant codes. Finally, a mask level fix on silicon achieved the desired SNR performance for all the codes.

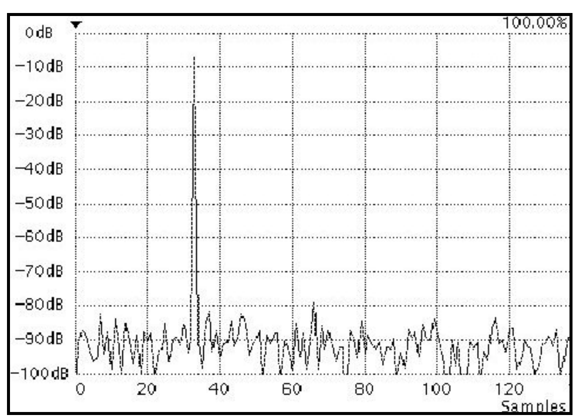
Introduction

A mixed signal, Communication Signal Processor (CSP), was not exhibiting the expected SNR in the Analog to Digital Converter (ADC) section. The 13 bit ADC has a theoretical SNR of approximately 80dB. Significant differences (about 6dB) were observed between SNR values at the wafer level and package part tests.

An experiment was planned to identify the source of degradation. The plan was to take some packaged devices, test their noise performance, decapsulate them and retest again to compare differences. The 6dB difference (typical) between packaged and decapped parts were evident on all tested parts. In addition, significant differences in total harmonic distortion (THD) and noise floor in general were also observed (refer to Graphs 1 and 2 below and Table 1 summary). The 6dB SNR difference was further verified by bench testing. This proved that the package material was causing the noise degradation by altering the dielectric constant in the vicinity of some sensitive circuits. Therefore, isolating the sensitive areas became the next diagnostic step.



Graph 1 - Packaged device showing degraded SNR and noise floor.



Graph 2 - Decapped device showing expected SNR and noise floor.

Table 1: Test results

Parameter	Packaged Parts or with DiAC	Decapped parts without DiAC
SNR	58.911 dB	66.419 dB
THD	67.834 dB	74.727 dB
Noise Floor	70.462 dB	77.357 dB

Isolation

Based on previous experience, we decided to use a Dielectric Altering Compound (DiAC) and apply it systematically to sections of the chip in order to isolate which part of the circuit was sensitive to packaging[1]. The Dielectric constant of the packaging material was 3.7. In order to simulate the effects of plastic packaging, a DiAC with a dielectric constant greater than 3.7 would have to be used. The DiAC used was a common heat sink grease, with a dielectric constant of 4. This compound has been used previously to simulate plastic package encapsulation by adding parasitic capacitance to the underlying circuitry[1].

To start diagnostics, the entire chip was initially covered with DiAC to see if its SNR would degrade. A 6dB degradation was observed with this treatment. Next, since the ADC SNR was degraded, the DiAC was applied to only half of the chip where the analog circuitry was located (Fig. 1). Again, SNR degradation was observed. The digital section of the chip was then coated with the same DiAC and this time, no degradation was observed. This confirmed our speculation that the analog section of the chip was the one that suffered from the packaging degradation effect. Using one strand of a fine artist brush, the DiAC was applied to smaller and smaller areas, (Fig. 2, 3) eventually concentrating around the sampling capacitors of the ADC circuitry. Initially, it was thought that there was noise coupling between some digital control circuitry and the sampling capacitors of the ADC section. Applications of DiAC to these areas however, failed to show SNR degradation. The evidence, however, continued to indicate that the sampling caps and their surrounding areas were the sources of the SNR degradation problem. Pinning down the exact offending circuit element, however, became more of a challenge. An innovative approach was required to precisely apply and trim the DiAC to the ADC elements and their surrounding section(s).

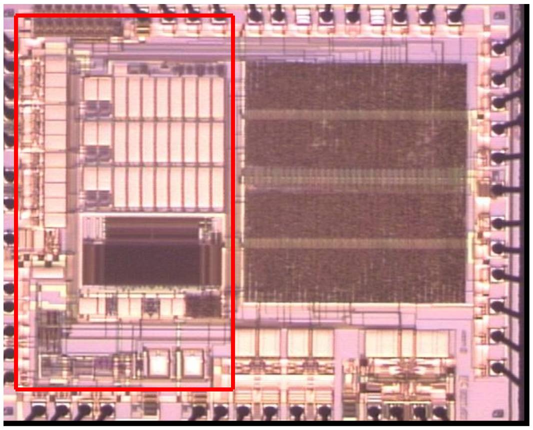


Figure 1 - Analog section covered

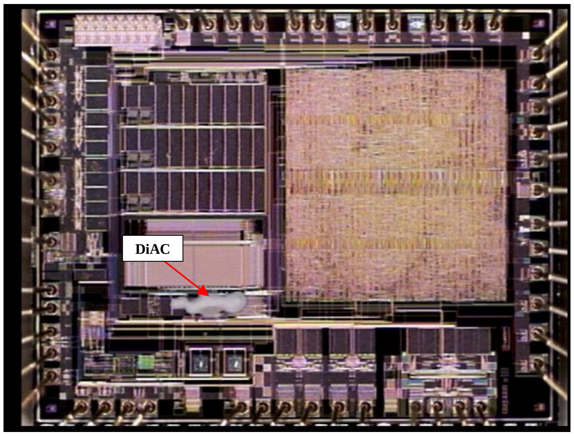


Figure 2 - Example of DiAC application

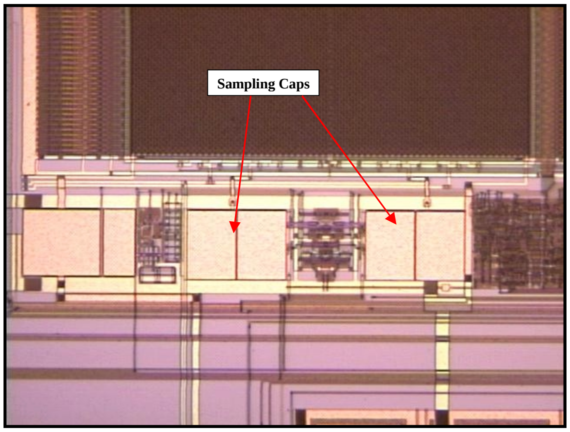


Figure 3 – Higher magnification image of the sampling caps in the DAC section.

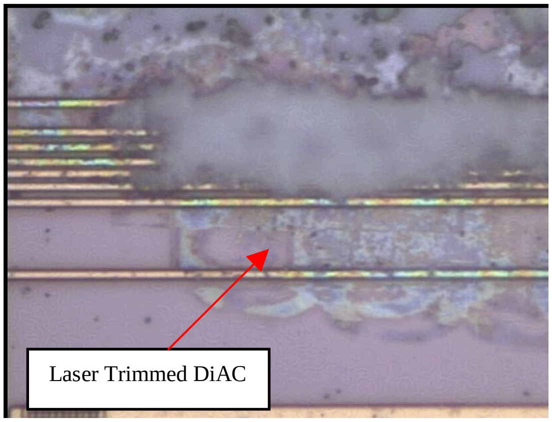


Figure 4 - Example of Laser Trimming

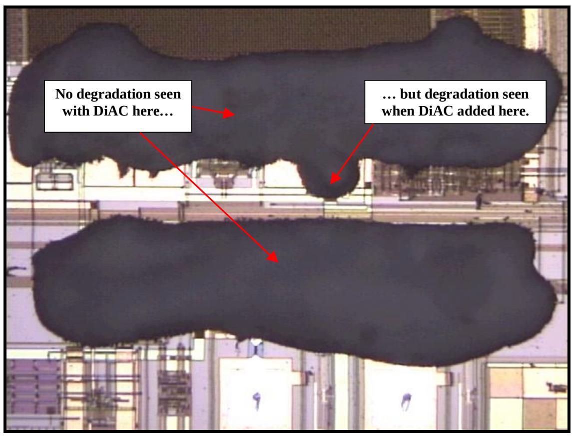


Figure 5 - Final Isolation DiAC cover

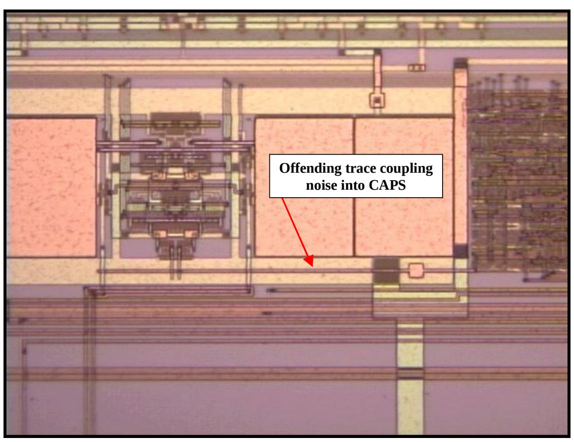


Figure 6 - Suspect Trace

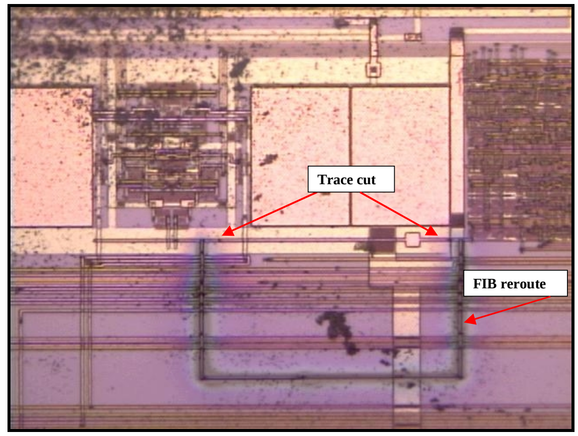


Figure 7 - Unsuccessful FIB re-route

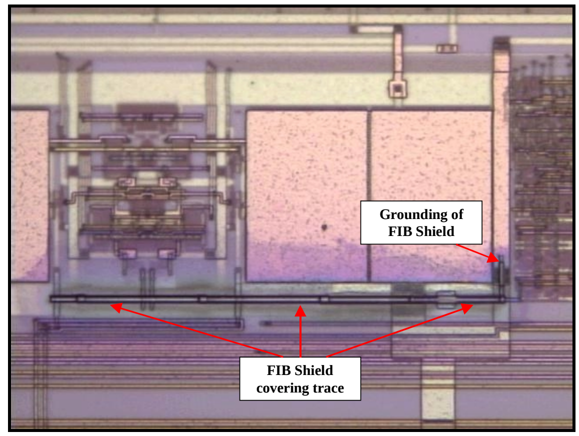


Figure 8 - Successful FIB Shield

A method of applying the DiAC in the general troubled area and laser trimming the DiAC away was suggested, discussed, and implemented. A New Wave laser, model LCSIII Tri-Lite, was used in the UV mode (355nm) to trim away the DiAC. With this wavelength, it was possible to remove the selected DiAC (Fig. 4) without damaging any underlying circuitry. DiAC was applied, device tested, DiAC laser trimmed, and device re-tested. Using this method, we were able to more accurately pinpoint the offending circuit elements.

Several techniques were used to apply the DiAC compound. The best results were obtained by dipping a mechanical probe in the compound and then apply it using a low power microscope. With practice, a section of circuitry could be covered and spread over the targeted area. Laser trimming accomplished further isolation on specific circuit elements.

After application of the DiAC, devices were re-tested and characterized. Additional DiAC application or trimming was done after testing or, at times, the device was cleaned in acetone and a fresh application was applied in a new area. This process was repeated until there was confidence that the sensitive area was identified. One final application of DiAC surrounding the suspect area (Fig. 5) showed no degradation until after the isolated circuitry was covered. A metal three line, which ran adjacent to the ADC sampling caps, appeared to be the point at which noise was coupled into the ADC section (Fig. 6). The last step was to verify the finding.

Verification and Fixes

Discussion with the design and layout engineers, led to a suggestion to disconnect the offending line and reroute it[2]. A FEI FIB Model 200 was used to disconnect and reroute the offending runner (Fig 7). This however degraded the performance further even without the presence of any DiAC, perhaps because of the higher resistance of the rerouted line.

Further discussions led to the idea of using a grounded metal shield over the offending circuit element[3]. Again, using a FIB system, a metal shield was placed over the offending runner and tied to ground (Fig 8). DiAC was then applied to the suspected area. This time the noise degradation phenomenon was gone.

Knowing the offending trace, a metal mask fix was now proposed. The runner was routed away from the sampling capacitors and moved to an underlying metal level. This mask solution was successful and was then applied to circuits associated with two other codes that had used the same codec design.

Summary

Communication Signal Processors (CSP) did not have the Signal-to-noise ratio (SNR) performance expected in packaged form. A Dielectric Altering Compound (DiAC) was chosen to simulate the packaged configuration in decapsulated parts. The DiAC was selectively and iteratively applied to the chip in order to simulate the package caused noise degradation. Laser trimming of the DiAC helped to isolate the exact offending circuit elements that had contributed to the SNR degradation.

Next, a FIB system was used to verify that a metal trace was coupling noise to the adjacent sampling capacitors in the ADC section. This was verified by putting a ground shield over the offending metal line and resulted in recovery of the SNR performance.

Thus, by using a combination of DiAC, laser trimming (of DiAC), and FIB modification, we were able to isolate, verify, and rectify a SNR degradation problem. With this technique, we have come up with a permanent solution of using just one mask change and effectively recovered all of the packaging induced SNR loss in a communication IC.

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[1] Lucent Technologies, Technical Memorandum # 52211-860912-01M, “Capacitive effects on circuits due to passivation and packaging materials on the chip surface”, Davar, V, Lucent Technologies Proprietary (1986)
[2] Discussions with G. Gross, Scott Smith, and Tseng-Nan Tsai, Design and Layout Engineers, Lucent Technologies
[3] K.N. Hooghan, K.S.Wills, P.A. Rodriguez, S. O’Connell, “IC Device Repair using FIB System, Tips, Tricks, and Strategies”, proceedings of ISTFA 1999, pp 247-254