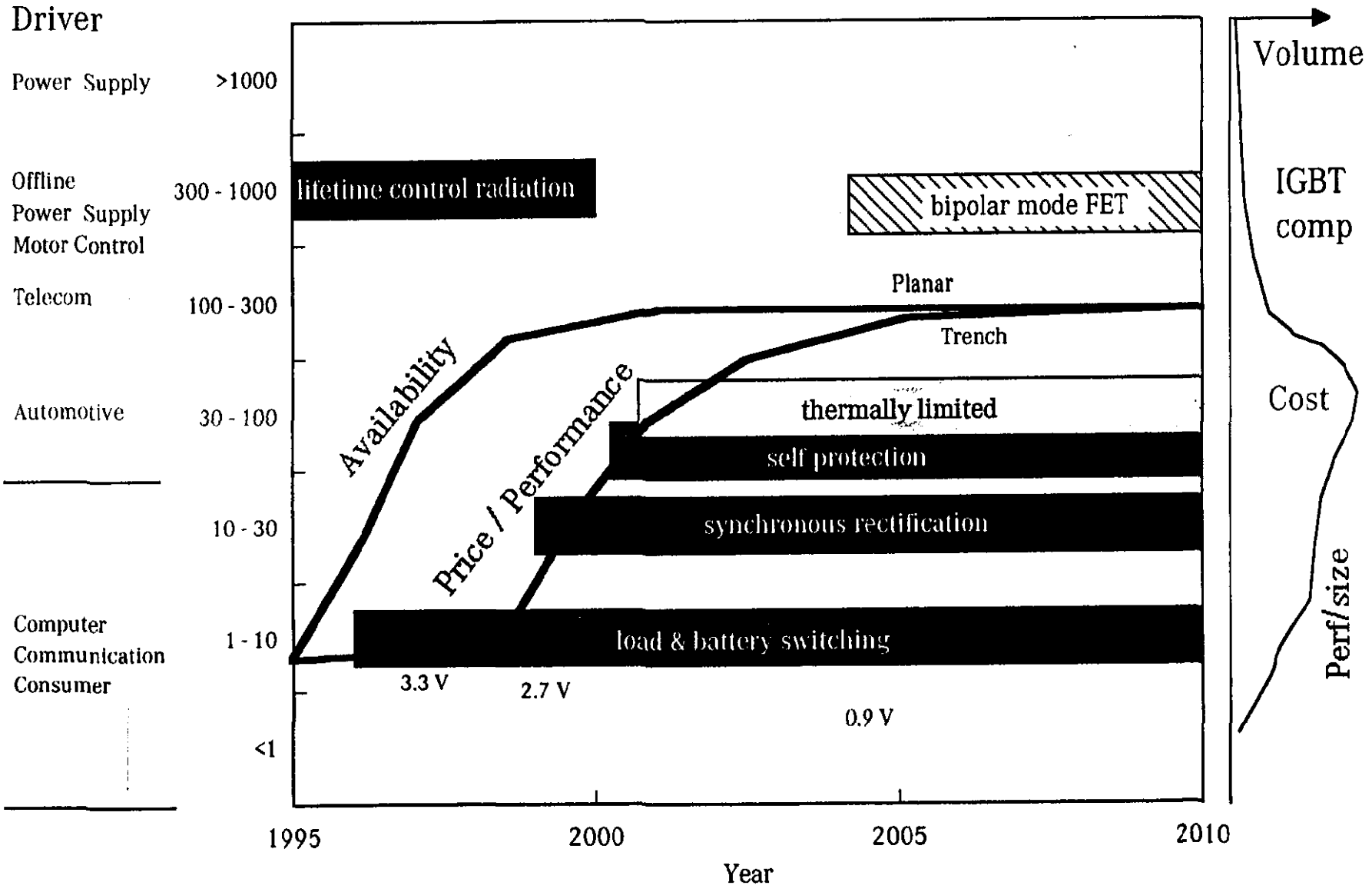
Technology Roadmap for Power Semiconductors

ISPSD'96 Maui, Hawaii

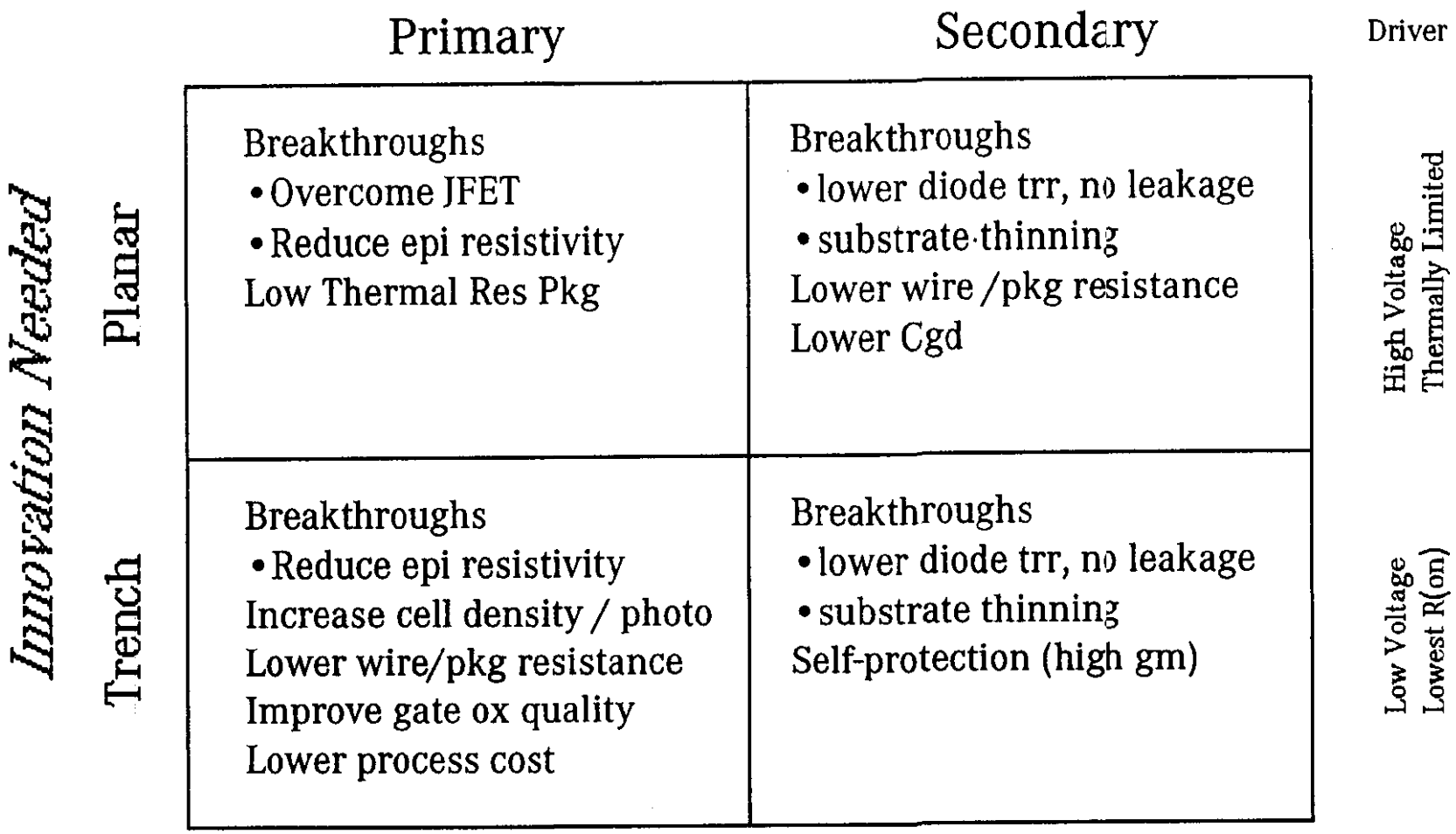
- Attached is a preliminary edition of the first Technology Roadmap for Power Semiconductor Devices
- At this time, some pages have been converted into computer graphics, others are still hand sketched
- A corrected version will be mailed to you this summer
- Special thanks to our workshop facilitators
  - ► Phil Hower, Unitrode, workshop chairman
  - ► Dan Kinzer, International Rectifier, discretes group
  - ► Leo Lorenz, Siemens, high power group
  - ► Aymen Shibib, Lucent Bell Labs, power & high voltage ICs
- Thanks for participating

Richard K. Williams, Siliconix / Temic
General Chairman ISPSD'96

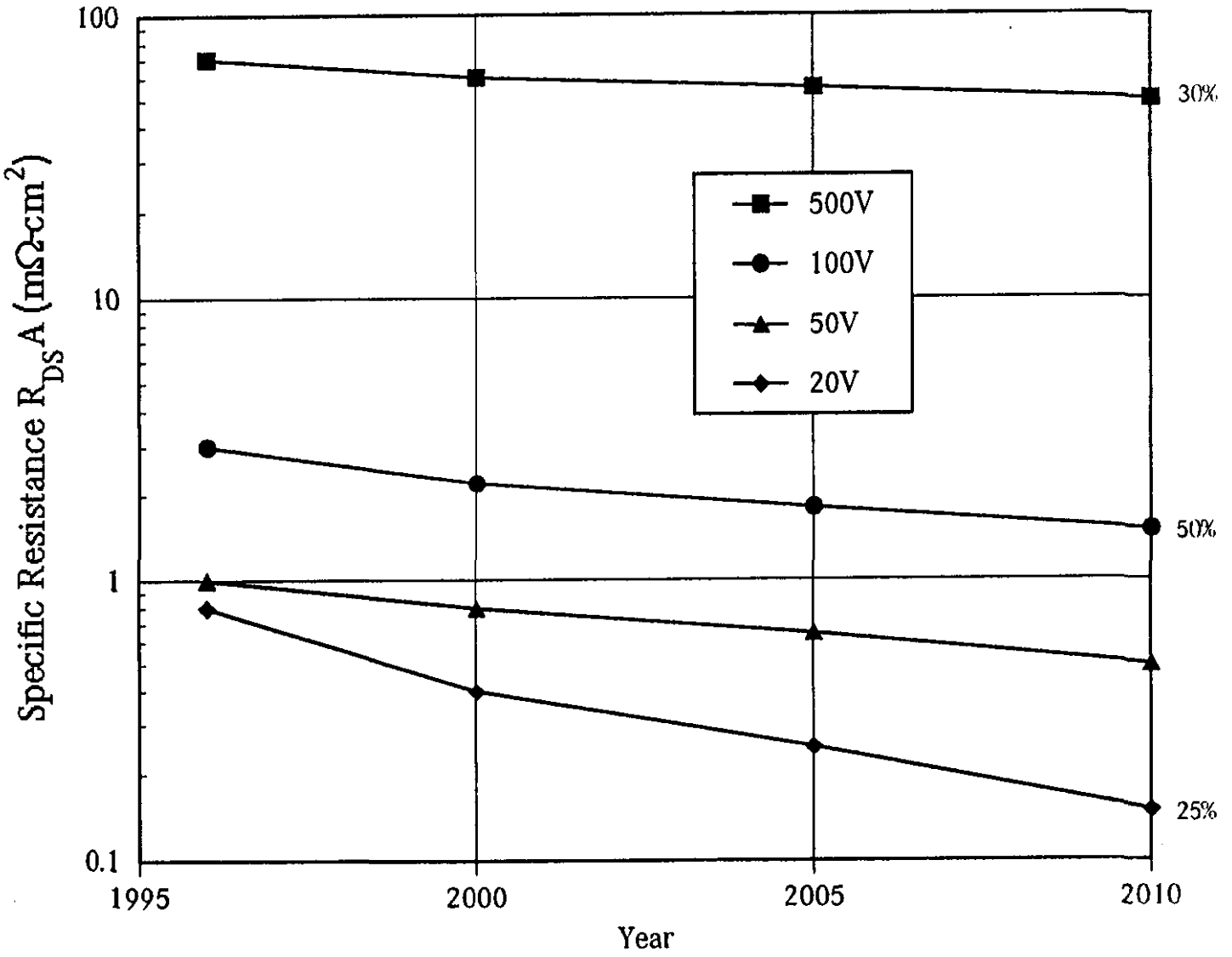
Trench & Planar FET Application Areas



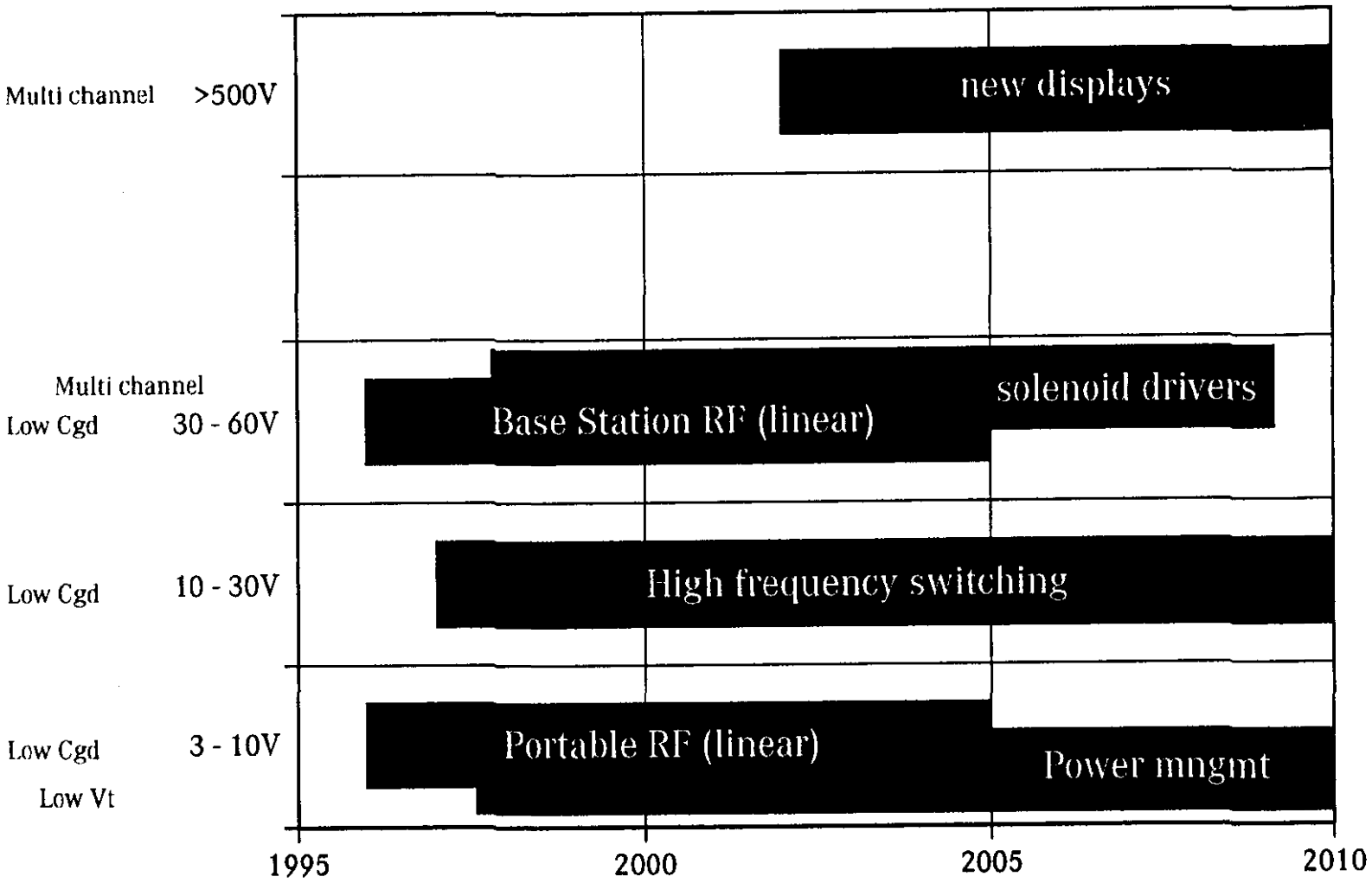
Challenges in MOSFETs



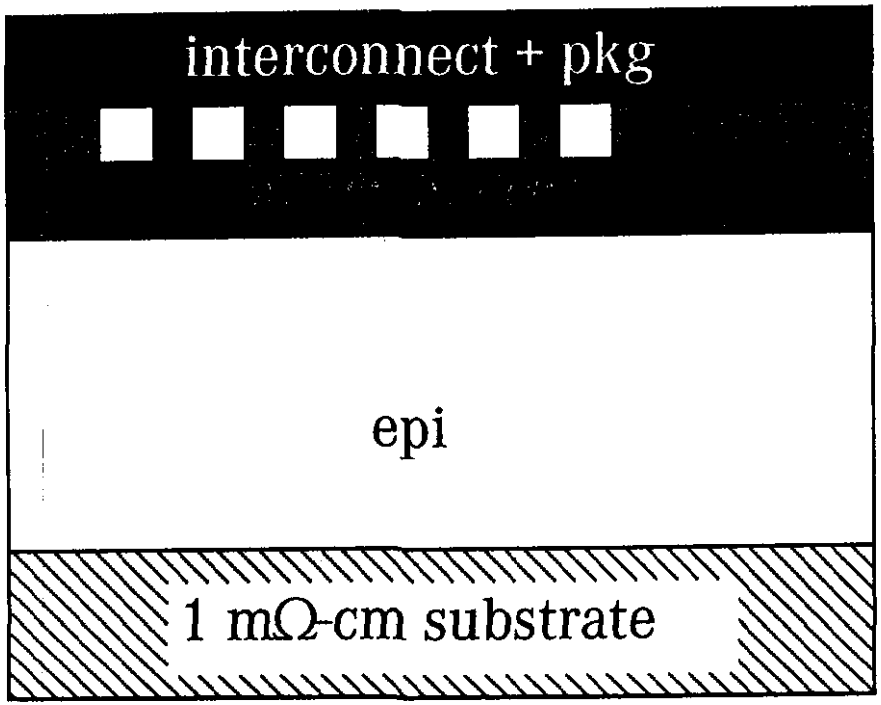
Trend in MOSFET $R_{DS}(on) \bullet A$



Lateral MOSFET Applications



Discrete Breakthrough Opportunities



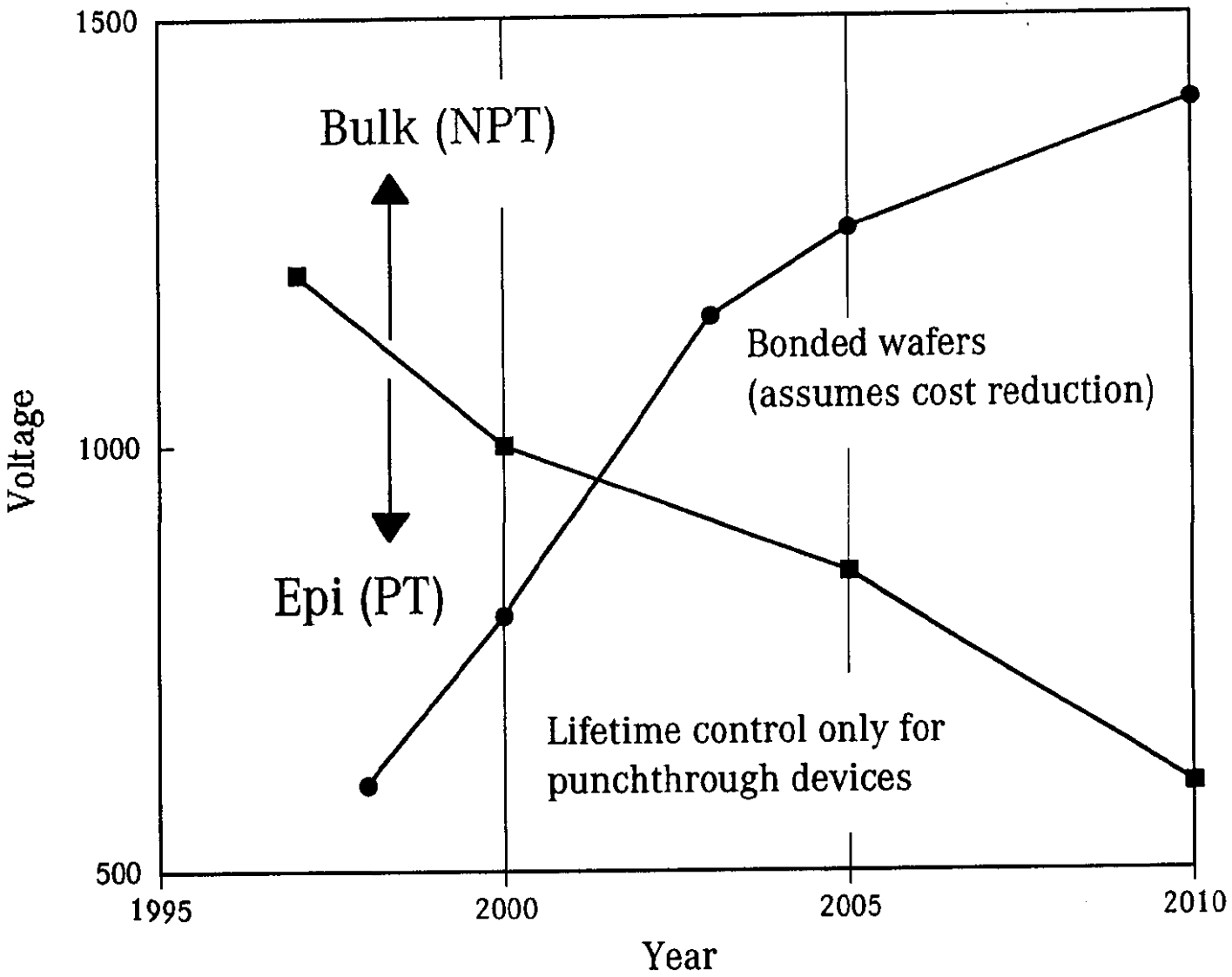
no wire / pkg resistance

silicon technology:
density, cost

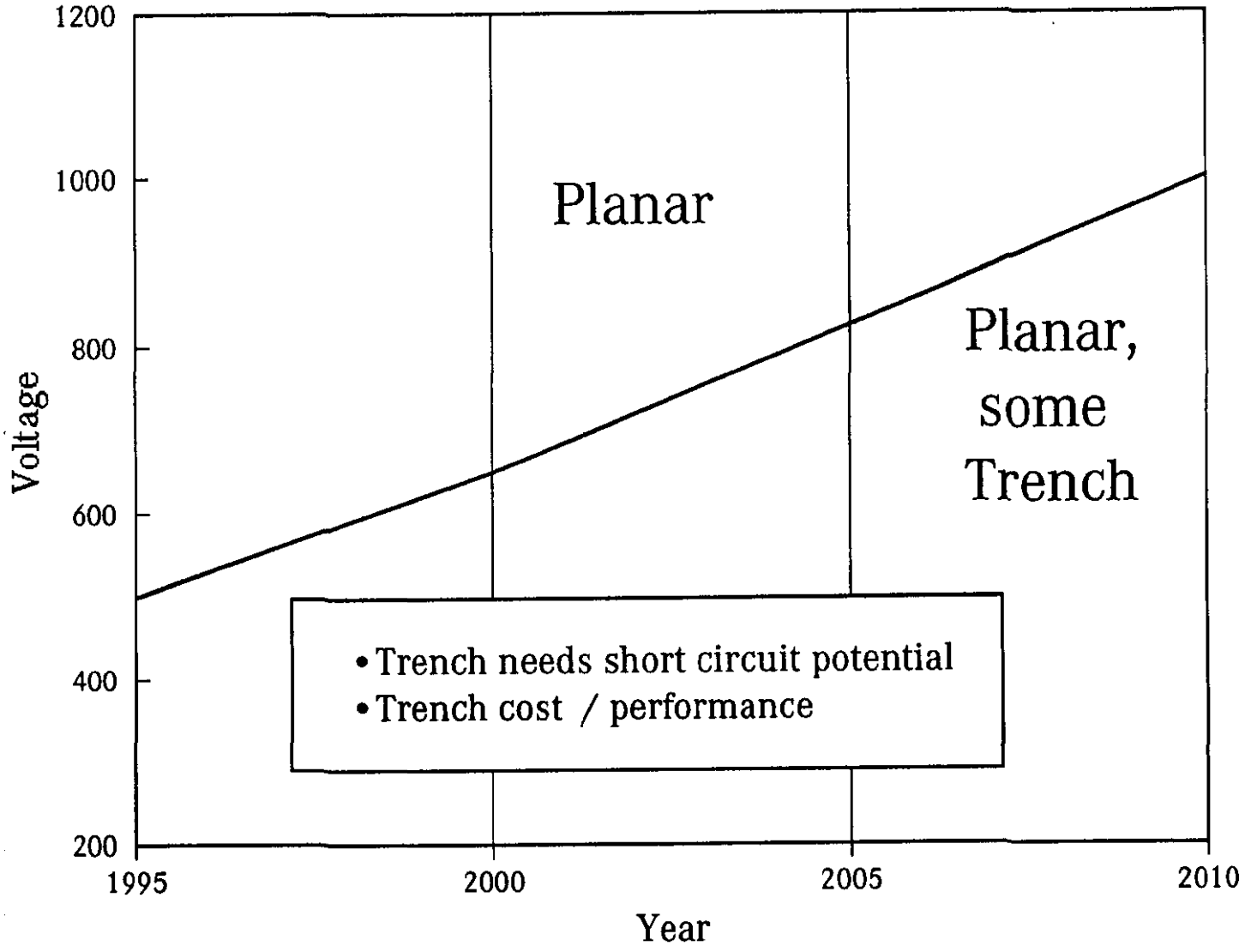
new materials:
$RA = \rho \bullet x_{epi}$

wafer / die thinning:
no breakage

IGBT Processes



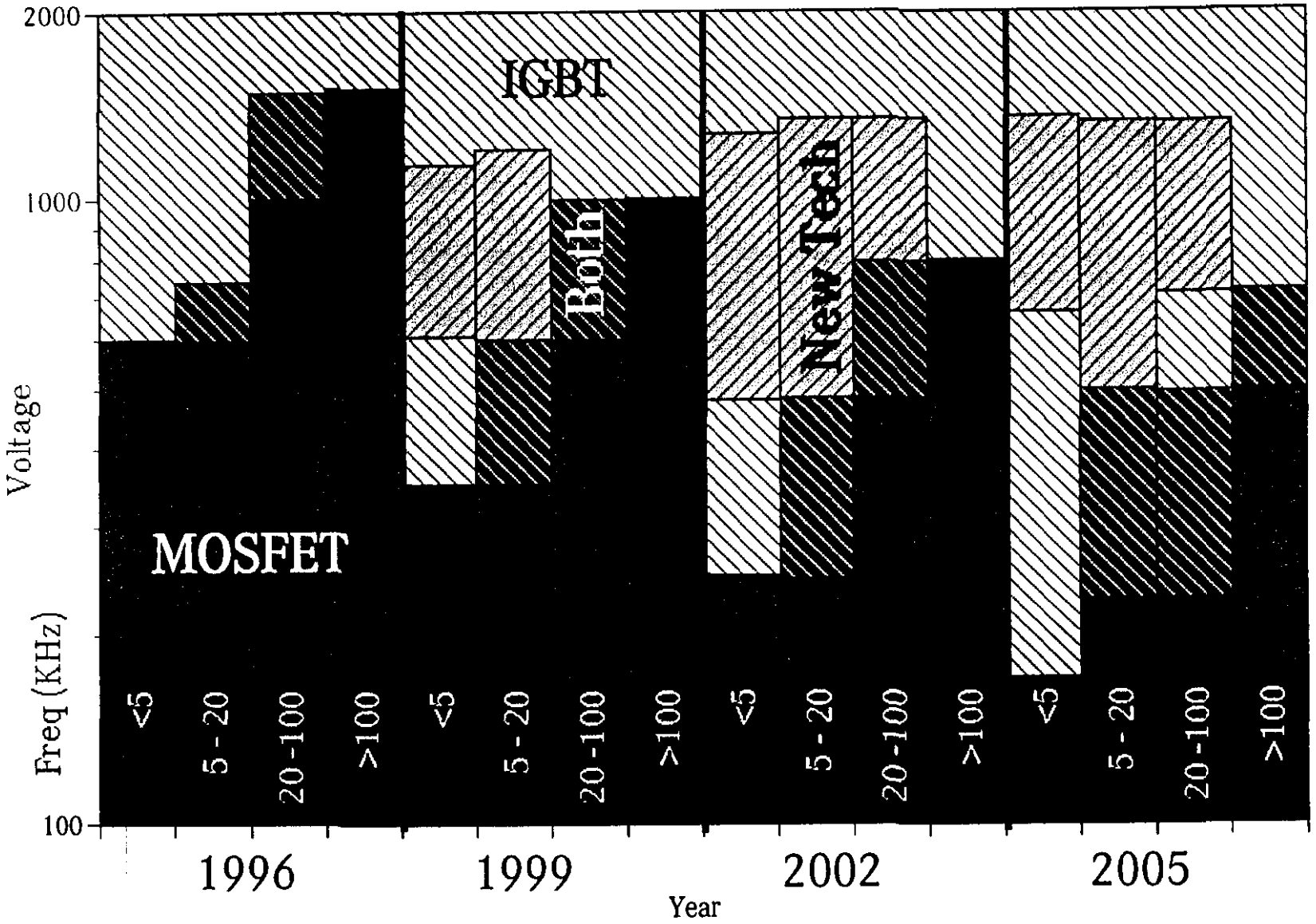
Voltage Range of Planar & Trench IGBTs



IGBT Innovations

Innovation Needed	Primary	Secondary	Driver
	In fab lifetime control • Au, Pt implants • e^- or H^+ Built-in diode	VLSI technology • self-aligned • photolithography • metallization • sidewall spacers *Lateral IGBT = not likely*	Better speed vs on-state drop
	On-chip control circuits Reliability • at high temperatures • metals/materials • packaging • design	Thin wafer processing • 100 μm • backing wafer Lower voltage	Improved thermal performance

Device Selection by Frequency & Voltage

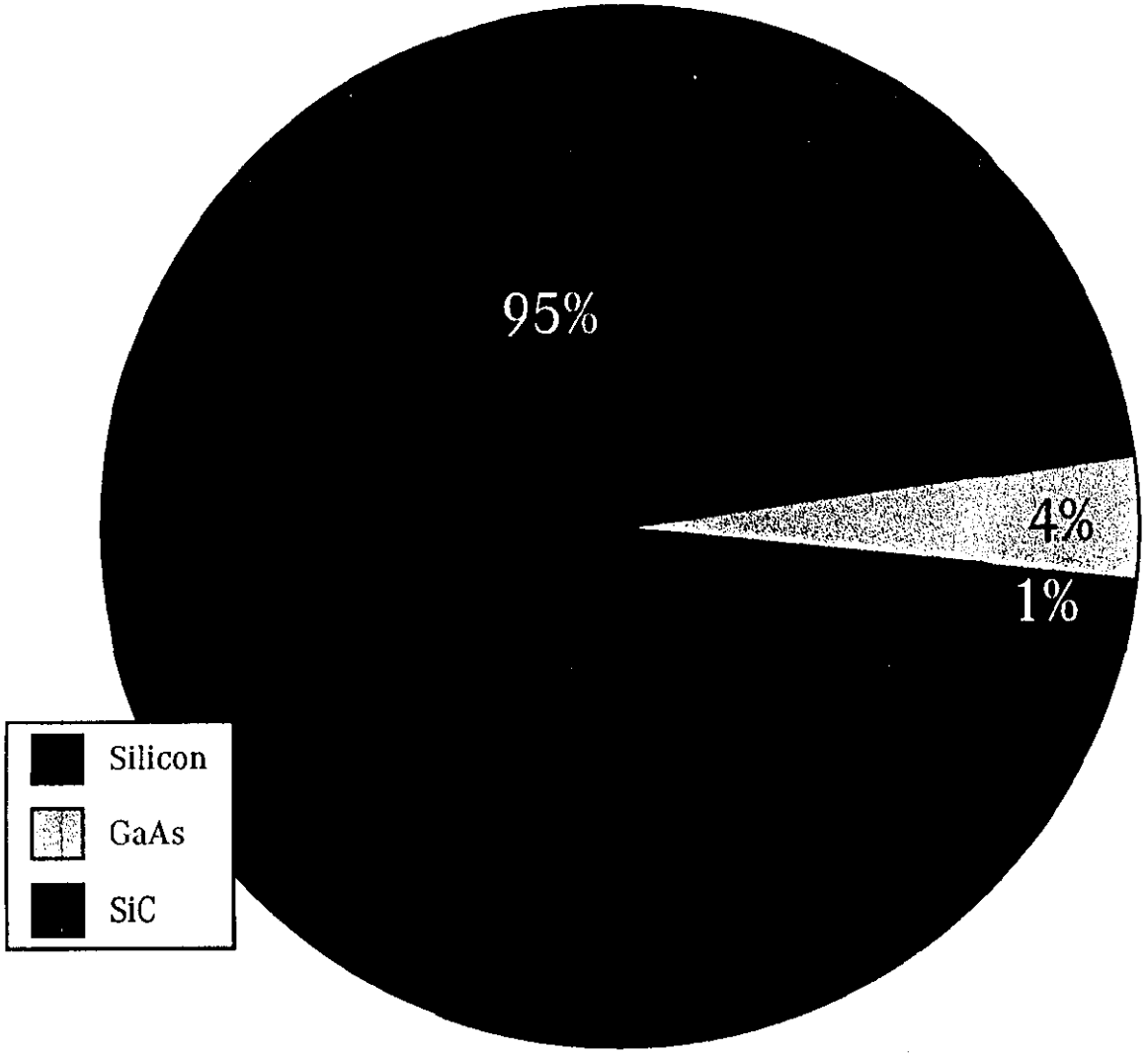


Silicon Rectifiers

Innovation Needed

	Primary	Secondary	Driver
Breakthrough	Metal/ Semi Schottky: Reduction in Vf at V<50V • 250 mV at 300 A/cm2 Low leakage • Tj = 125°C, Jr=150nA/cm^2	1600V Rectifiers: Epi • expensive, poor availability Non-epi • cheaper but higher losses • thin wafers • FZ 200 mm	Portables (LV) Offline (HV)
Improvement	Cost pressure • today's diodes 525 mV at 300 A/cm2 • synchronous rectifier	600V Rectifiers: Optimize Vf vs trr • trr = 28 nsec Vf = 2.5V • new lifetime killers • P+ • GaAs PIN	Logic Supply (LV) Offline (HV)

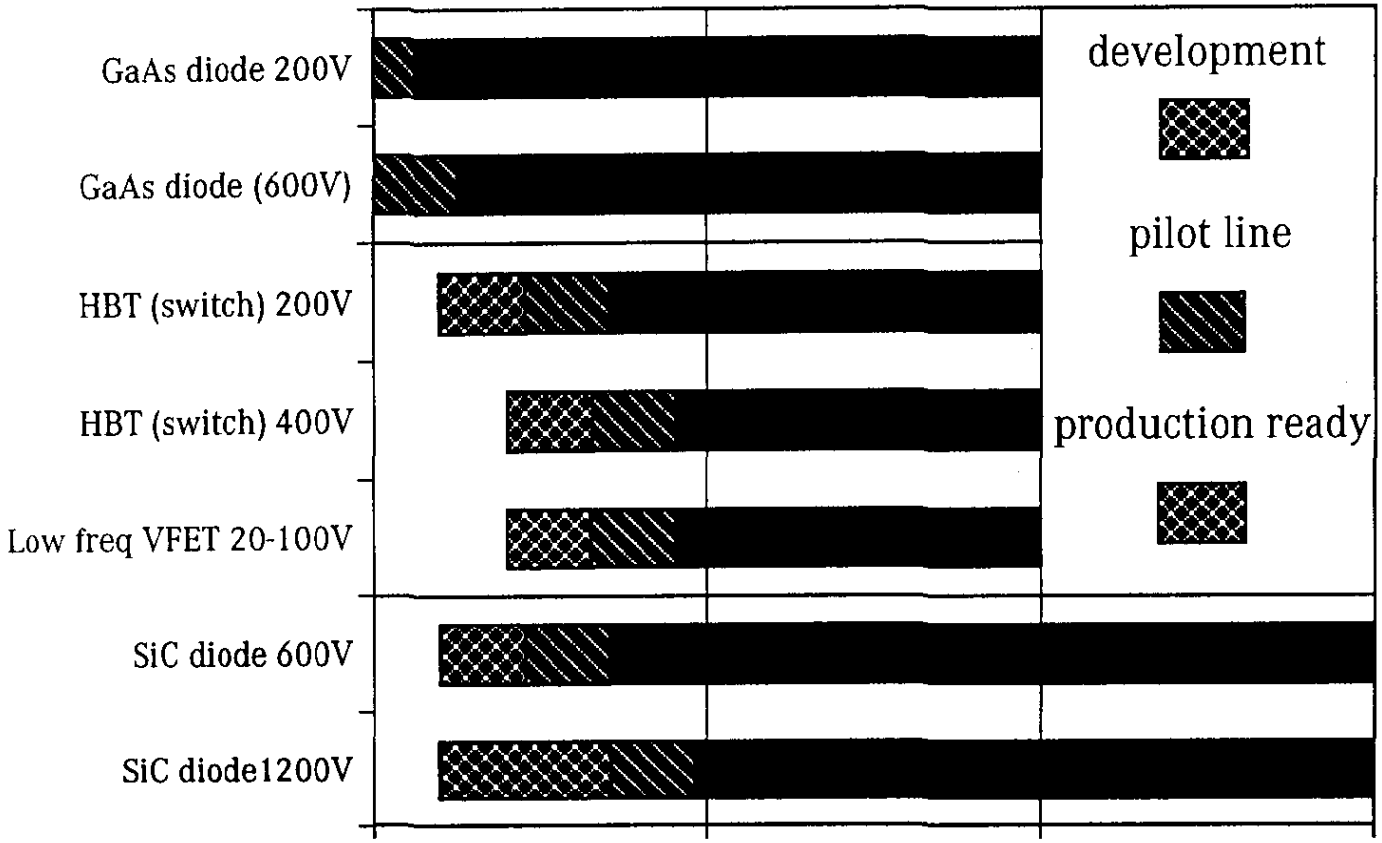
Rectifier Materials



High temp, speed niche

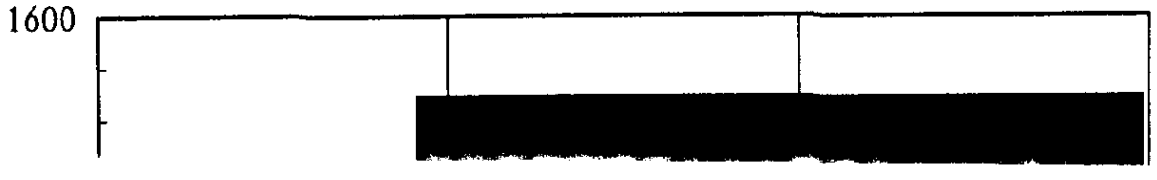
Too expensive, needs new pkg for high temp

Power Devices of New Materials



Production ready indicates technology, not economic performance or production viability

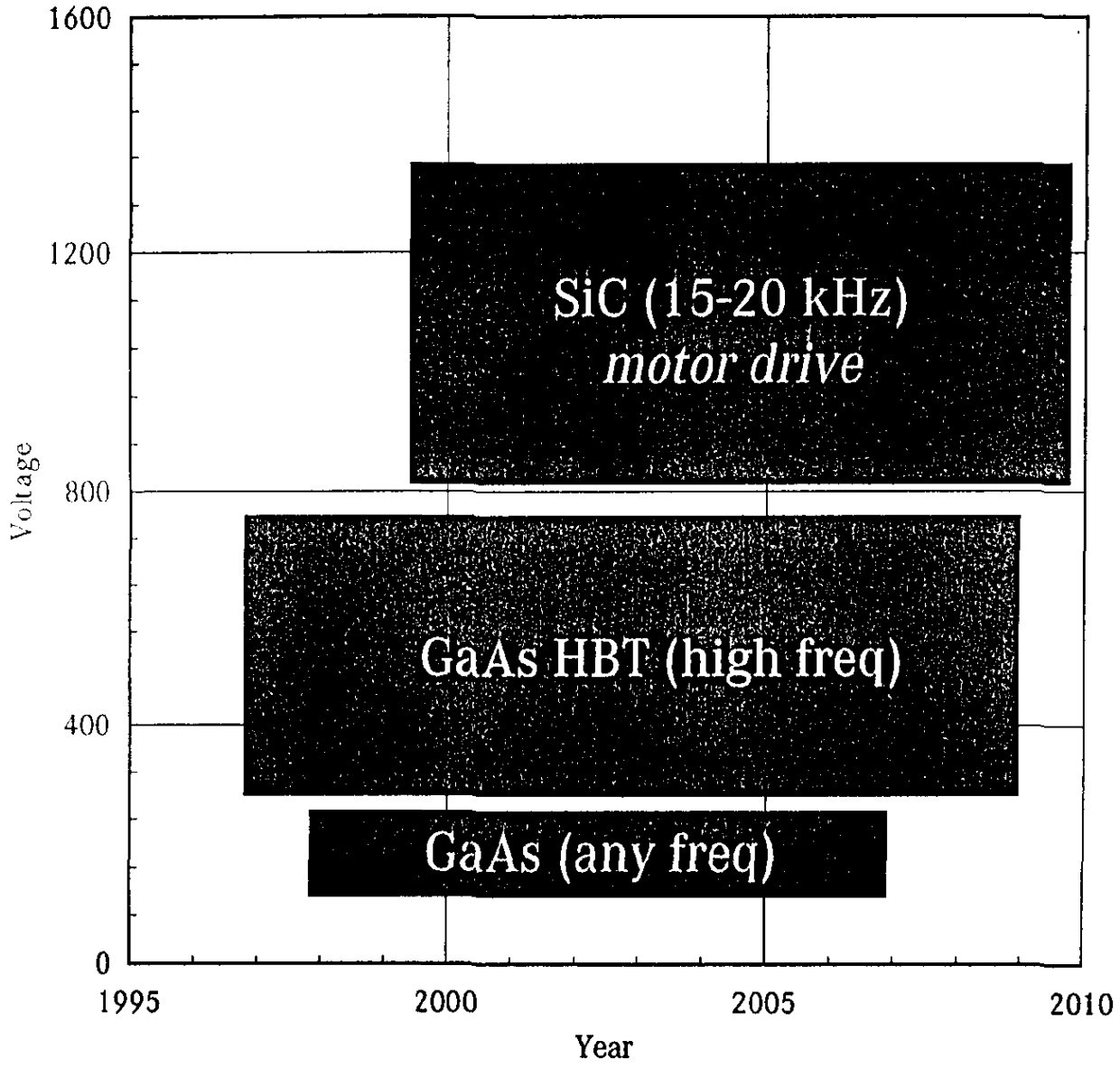
Preferred Diode Material (ignoring cost)



New Materials for Rectifiers & Switches

Innovation Needed	Primary	Secondary	Driver
Breakthrough	GaAs: Dielectric Wafer size, quality, defects SiC: Novel structures Niche application Packaging	SiC: Fab	speed & temperature
Improvement	GaAs: VFET scaling up vs. Si UMOS Packaging, VPE vs MOCVD 1 supplier exists SiC: Wafer quality & size (μpipes) Process optimization/fab	GaAs: 2" vpe 10 μm epi $250, 50 μm $350, 4" 5 μm $1100 MOCVD SiC: Numerical modeling Less vendores than GaAs	Material supply

Preferred Switch Material (ignoring cost)



Driver

$

Package Improvements

Innovation Needed

	Primary	Secondary	Driver
Breakthrough	Zero resistance and inductance Wafer level encapsulation Better TCE matching Chip on bopard, bump tech	Higher Tg plastics Robust die attach, better cycling Improved dicing technology	Surface mount, automotive
Improvement	Reduce pkg / chip footprint Multiwire configurations for pwr Exposed heatsink design SMP Better voltage isolation	High reliability wire bonding Improved mold lock compounds High purity low stress compnds	Surface mount

Power Semiconductor Technology Roadmap Workshop

Schedule for High Voltage and Power IC Session

1:30 Introduction to Workshops

1:45 High Voltage and Power IC Session Begins

1:45-1:50 Introduction - Ayman Shibib, Session Chair
1:50-1:55 Terishima - Junction Isolation
1:55-2:00 Fujishima - Self Isolation
2:00-2:05 Nakagawa- Silicon-on-Insulator (SOI)
2:05-2:10 Korec - Future Technologies
2:10-2:15 Morelli - System Integration

2:15-3:30 Group Discussion

3:30-3:45 Summary

3:45-4:15 Break

4:15-5:15 Workshop Presentations

M.A.Shibib

ISPDS'96 WORKSHOP

HIGH VOLTAGE & POWER IC's

Moderator: Ayman Shibib, Lucent Technologies - Bell Laboratories

INDUSTRY	UNIVERSITIES
Allegro	
AMKOR Electronics	
BCO Technologies	Stanford University
Boeing	
C.P. Clare	
Cherry	
Daewood Electronics	
Daimler - Benz	
EPISIL Techologies	
Ford	
Hitachi	
LAAS-CNRS	
Lucent Techologies (Formerly AT&T Microelectronics)	University of Toronto
Micrel	
Mitsubishi	
Motorola	
National Semiconductors	FHG - IMS
NTT	
Oki	Hong Kong University of S & T
Philips Research	Swiss Fed Inst Integrated Systems Lab
Power Integration	University of Liverpool
Rockwell	
SGS - Thomson	
Siemens	
Siliconix	
Supertex	University of New South Wales
Texas Instrument	
Toshiba	
Unitrode	

Registered Session Participants.

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JI HVIC

Vertical + Cntl logic

Lateral + " "

JI is the dominant technology in High Voltage & Power ICs.

PROCESS

60 V 1 μm logic Proc. Comp ↑ Cost ↑

600V 2-3 μm

MATERIAL

1996 2000

Resurf → Resistive overcoat

organic insulator

SELF ISOLATION

- SINGLE RESURF
- DOUBLE RESURF improves (RxA) vs BV

TRADE-OFF

ISSUES

Accuracy of Dose/Diff
Complexity of Process (more masks)
3 dim design
Multiple Epitaxy
Contact / Metal

SOI Technology

TREND : 500 V → 60 V

High Temp Applications

HV UPS / DC-AC SOLAR CELLS

LV Auto (ABS, Airbag, ECU) 85 mΩ mm²

Obsteacles : Wafer Cost
LIGBT
HV Interconnect
Reliability

Solns : Simple device
Smaller output device
— No Buried Layers
60 LDMOS on SOI ≈ 85 mΩ mm²
— Trench Gate

Future
> 2000 V MUST USE SIPOS @ BOX
> 10 A
200°C

Future Technologies

Power Module Features

Volume / Weight ↓

200C

High Reliability

Costs ↓ ⇒ More Import.

Electronics in Autos (Content)

14 % → 25 % in auto

8 % → 17 % popular cars

Largest Vol = 200°C

Niche ≥ 800°C

Integration ⇒ smart discretes

- High Temp growth - Auto

SOI 18 %
WBS 55 % (SiC } Growth Rate

- Chip / Pkg / Substr. integration
- KNown good die, hermeticity, cost

HIGH VOLTAGE AND POWER ICs
Technology Trends

Substrate
- Standard
- Epi
- SOI

Process
- Bipolar
- DMOS
- CMOS
- BiCMOS
- Measure of Process Complexity vs. Cost

Device Structure
- Vertical
- Quasi-vertical
- Lateral

Compare PIC Technologies vs. VLSI
- Design Rules
- Multi-level Metals
- Special Processing Requirements

Status of Silicon Alternatives

CAD Tools/Requirements

Hybrids vs. Monolithic
- Where is the boundary?
- Moving toward more integration?

Power Packaging
- Current Status
- Techniques borrowed from non PIC?
- Future power handling?
- Future pin counts

Reliability of PICs
- What improvements needed
- Is evolutionary improvement

M. A. Shibib

HIGH VOLTAGE AND POWER IC s

What is the Technology Driver for High Voltage and Power IC s ?

- Cost

MAINLY : - Primarily

. System cost reduction - For chip makers working with particular customer

. Chip cost - For catalog or mechanical relay replacement

- Size Reduction (System Integration)

secondary

- Reliability

- Market Application

important factor in determining importance of cost driver.

HIGH VOLTAGE AND POWER IC s

Intelligent PICs
(SMART POWER)

WORLD MARKET SIZE(~~MILLIONS~~) in $Millions.

	1995	*2000*	*2005*
Automotive	300	highest % Computer	
Computer	250	2nd highest → Automotive	
Telecom	150		
Industrial	150	No estimate of size	
Consumer	100		
Military	50		

TOTAL All ↑

computer

Above underestimated
Computer segment (for 95)

~~Multimedia~~
(~~Displays~~)

Important areas
- Multi-media
- Displays (Drivers)

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HIGH VOLTAGE AND POWER ICs

INTEGRATION ROADMAP

General Comments:

- Integration is important only if it represents a significant contribution/cost reduction to the customer, otherwise it is not necessari a strong driver of technology -

(PERFORMANCE)

INTEGRATION

VOLTAGE	Next 5 Years 2000	Next 10 Years 2005	Next 15 Years 2010
< 20	µP NOW		
< 60		Add µP (?) OR MULTICHIP	
< 200		No µP ON CHIP	
< 400		IT IS DIFFICULT TO INTEGRATE µP	
< 1000		? FOR THESE TECHNOLOGIES.	

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HIGH VOLTAGE AND POWER ICs

ROADMAP

General Comments:

Application areas of High Voltage & Power ICs by voltage range is the best way to consider trends and projections for each area.

APPLICATIONS

VOLTAGE	Next 5 Years 2000	Next 10 Years 2005	Next 15 Years 2010
< 20	BATTERY CHG COMPUTER MOTOR CONTROL		
< 60	POWER MANAGEMENT AUTOMOTIVE		
< 200	AEROSPACE TELECOM DISPLAYS		
< 400	LAMP BALLAST		
< 1000	INDUSTRIAL		

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HIGH VOLTAGE AND POWER ICs

ROADMAP

General Comments:

COST TRACK started: 10X ; 3X - INITIAL COST ?

CURRENT ~ 5X

FUTURE ~ 3X

- BIPOLAR TECHNOLOGIES BENEFIT OF SIZE SHRINK BY USING SOI (some by 2.5X).

SUBSTRATE ISOLATION

VOLT	Next 5 Years 2000	Next 10 Years 2005	Next 15 Years 2010
< 20	JI		SOI w/ INTEGRATION IMPORTANT IN CASE OF SYSTEM INTEGRATION
< 60	JI	SOI ? (TEMP) HIGH TEMPERATURE	
< 200	JI		
< 700	DI		SOI w/ DUMETEN INCR.
< 1000	DI		

LOWER COST

SOI will replace Dielectric Isolation for > 5 inch diameter

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HIGH VOLTAGE AND POWER ICs

Existing Power Technologies	NOW	FUTURE
- Junction Isolated Power IC s	5 um Bipolar 1.2-1.5 um BiCMOS	.8 → .5
- Self Isolated Power IC s	3 um CMOS	WILL FOLLOW CMOS PROGRESS WITH FEW YEARS LAG -
- DI Power IC s	3 um BiCMOS	
- SOI Analog/Power IC s	1 - 3 μm	

HIGH VOLTAGE AND POWER ICs

PROCESS ROADMAP

General Comments:

- BIPOLAR TECHNOLOGY → NICHE APPLICATIONS
- CMOS & BICMOS AS MAINSTREAM.
- COMPLEX TECHNOLOGY DEPENDS ON LEVEL OF INTEGRATION NEEDED

BIPOLAR
CMOS
BICMOS

* PROCESS (COMPLEXITY)

	Next 5 Years 2000	Next 10 Years 2005	Next 15 Years 2010
< 20	NEEDS		
< 60	ARE		
< 200	DEPENDENT	UPON ADDITIONAL	
< 700		INTEGRATION (µP)	
< 1000	INTEGRATION	VS. MULTICHIP	

HIGH VOLTAGE AND POWER ICs

METALIZATION & WAFER DIAMETER ROADMAP

General Comments:

METALS

- NEW METAL COMPOSITION NEEDED? (DIFFERENT THAN VLSI)
  NEED PR/ETCH EQUIP FOR METAL
  - DESIGN RULES
  - METALS
- FOLLOW CMOS' ← WAFER DIAMETER

	Next 5 Years 2000	Next 10 Years 2005	Next 15 Years 2010
< 20			
< 60	3 LM THICK TOP METAL COMPOSITION ?		
< 200	2 LM	3 LEVELS OF METAL 3 LM	
< 700			
< 1000		(THICKER METAL) 3 - 7 μm THICK	

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- DIFFICULTY IN PHOTORESIS
- DIFFICULTY IN ETCHING

HIGH VOLTAGE AND POWER ICs

DEVICE TYPE ROADMAP

General Comments:

- VERTICAL HAS BEEN PREDOMINANT
- LATERAL DEVICES CAN PROVIDE VERY LOW ON-RESISTANCE & CURRENT HANDLING CAPABILITY IF MULTI-LEVEL THICK METAL IS USED.

DEVICE TYPE

	Next 5 Years 2000	Next 10 Years 2005	Next 15 Years 2010
< 20			
< 60			
< 100			
< 700	VERTICAL	LATERAL CURRENT IMPROVEMENT	
< 1000			

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HIGH VOLTAGE AND POWER ICs

POWER PACKAGING ROADMAP

General Comments:

- CURRENT PACKAGES ARE ADEQUATE.
- WOULD LIKE TO SEE:
  1- LOWER THERMAL RESISTANCE
  2- LOWER DC & AC PARASITICS.
- BARE CHIP IS ULTIMATE PACKAGE FOR POWER ICs (REDUCED COST).

PACKAGING

	Next 5 Years 2000	Next 10 Years 2005	Next 15 Years 2010
TECHNIQUES FROM NON-PIC	FLIP-CHIP DEVELOPED - DC RESISTANCE	FLIP CHIP (BARE DIE)	
FUTURE POWER HANDLING	- IMPROVED THERM PERF ON SURF. MT.		
FUTURE PIN COUNTS		OK W/ BARE DIE	

CURRENTLY : 600-V FLIP-CHIP ICs IN HIGH RELIABILITY SYSTEMS ARE AVAILABLE

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HIGH VOLTAGE AND POWER ICs

CAD, RELIABILITY & Silicon ALTERNATIVES: ROADMAP

General Comments:

- CAD : NEED 3-D Device Simulation (now ~~Key~~)
  - SPICE-TYPE MODELS ADEQUATE
  - WOULD LIKE TO SEE PROCESS-INDUCED DAMAGE IN SIMULATORS.
- RELIABILITY: HV & PICs community need to learn more about hot carriers effect as sizes ~~is~~ shrink from CMOS-VLS
- Silicon Alternatives: SILICON WILL BE MAINSTREAM FOR NEXT 10 YRS

	Next 5 Years 2000	Next 10 Years 2005	Next 15 Years 2010
CAD OK	3 D COMPONENT IMPROVED CIRCUIT THERMAL	SECTIONS EFFECTS NEED MIXED SIGNAL	
RELIABILITY		HOT CARRIER EFFECTS	
Si ALTER.	Si OK	NICHE for ALTER.	

- GAAS & SiC - Will appear in discrete devices first - will be Niche

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Workshop

High Power Devices and Power Modules

Maui, Hawaii

by
L. Lorenz

❒ Invited Speakers

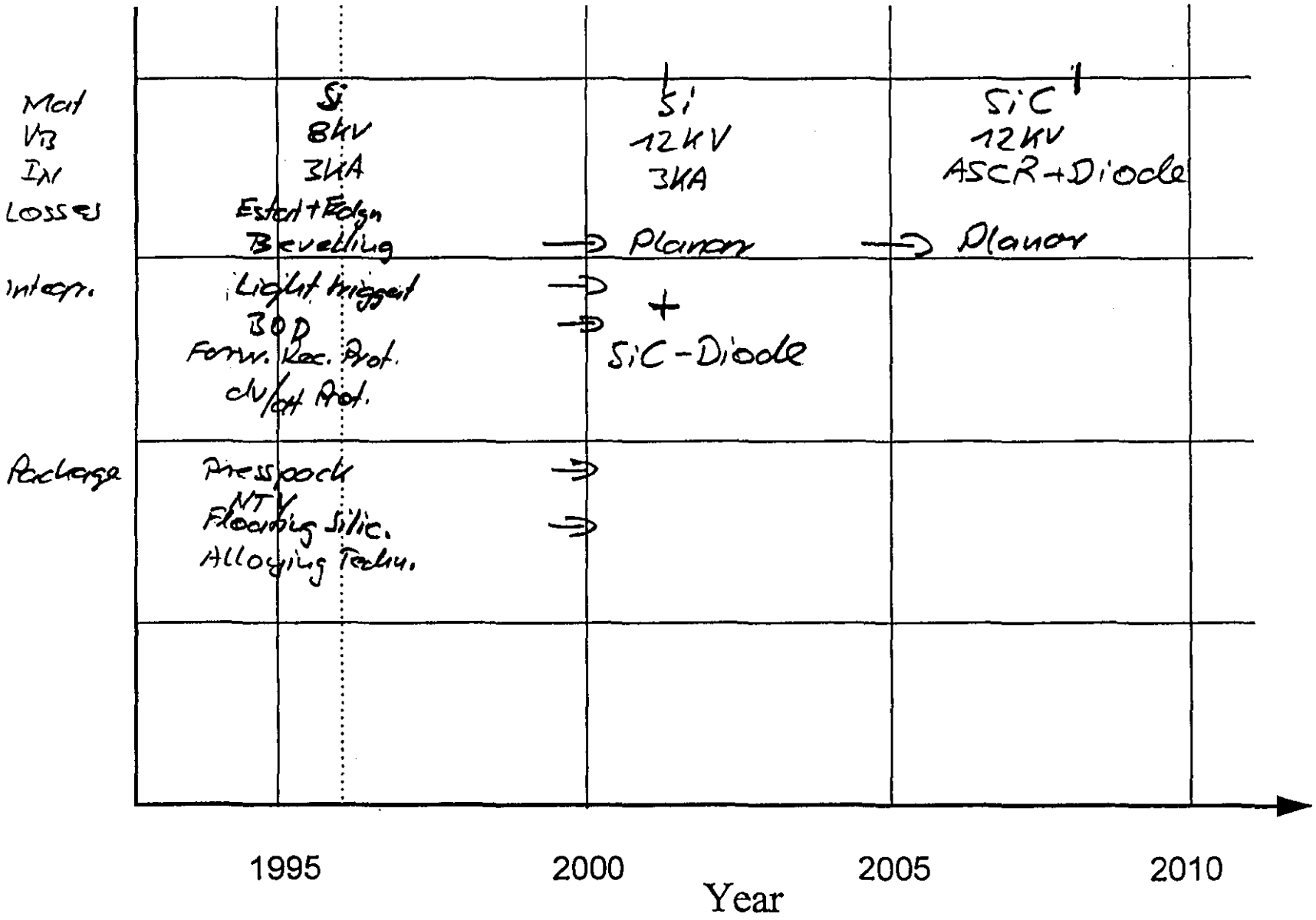
Mr. Robb	Motorola
Mr. Jaecklin	ABB
Mr. Ohashi	Toshiba
Mr. Kobayashi	Hitachi
Mr. Shigekane	Fuji
Mr. Takata	Mitsubishi

❒ Working Group

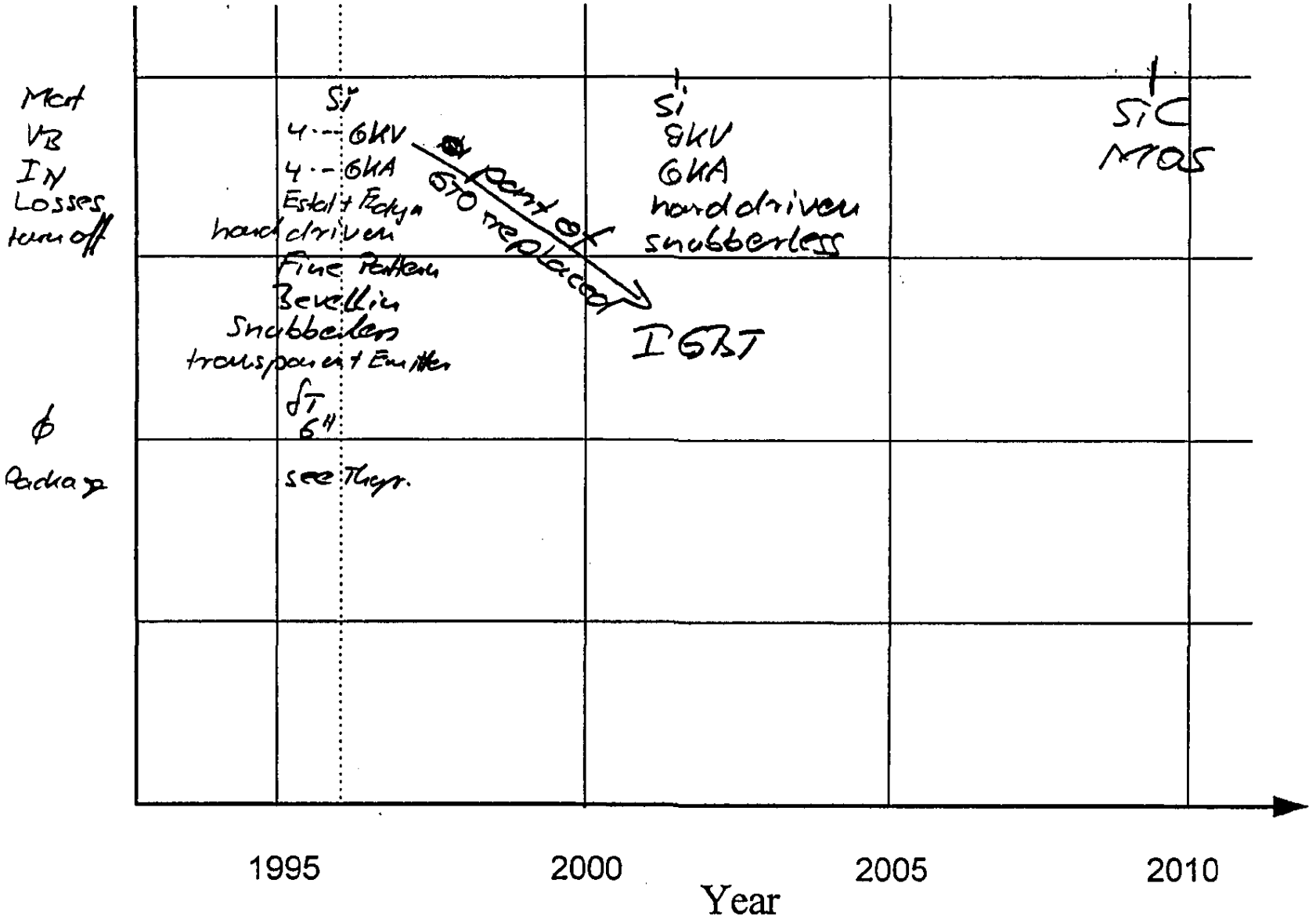
❒ Presentation: Roadmap

High Power Device

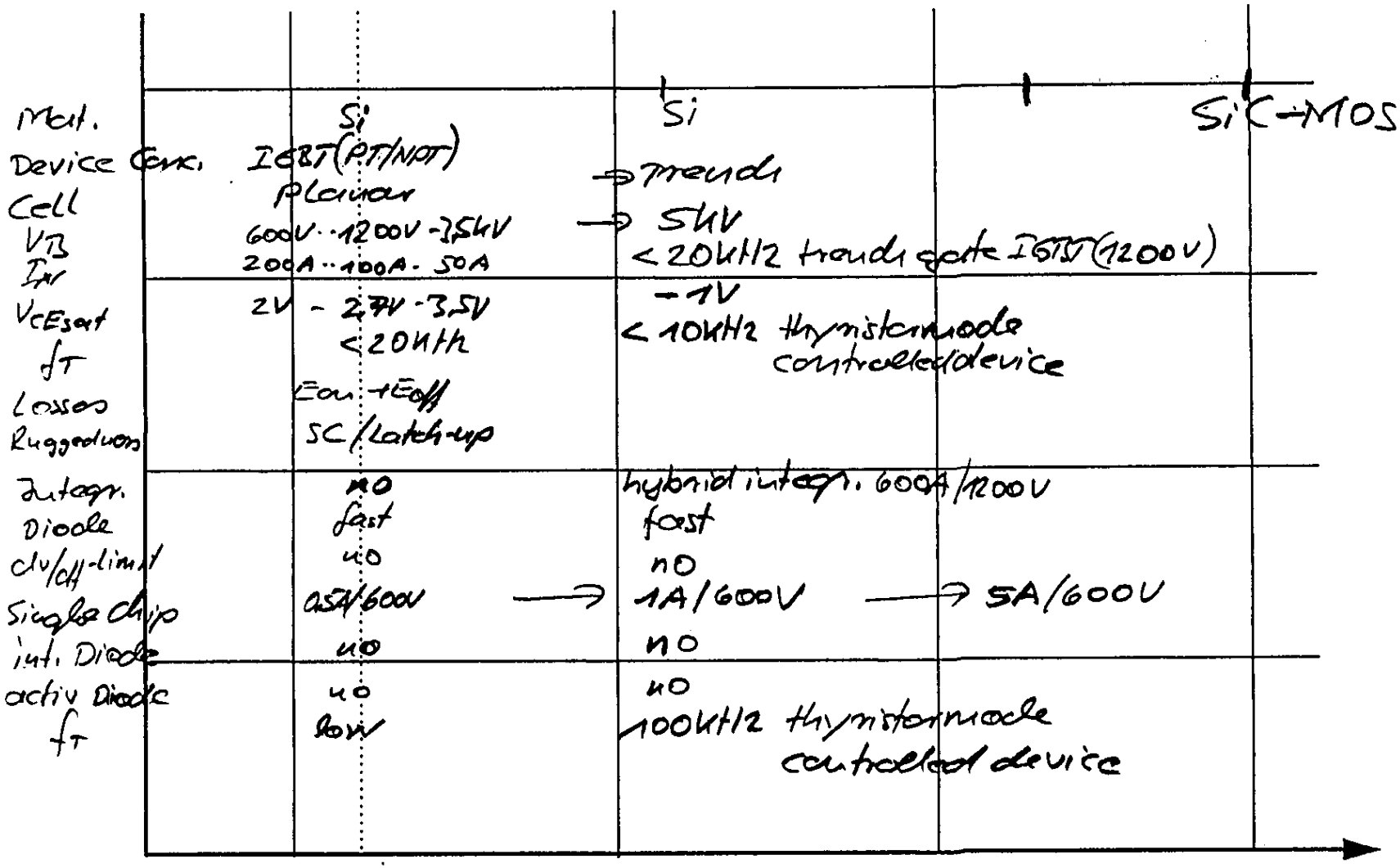
Thyristor Roadmap



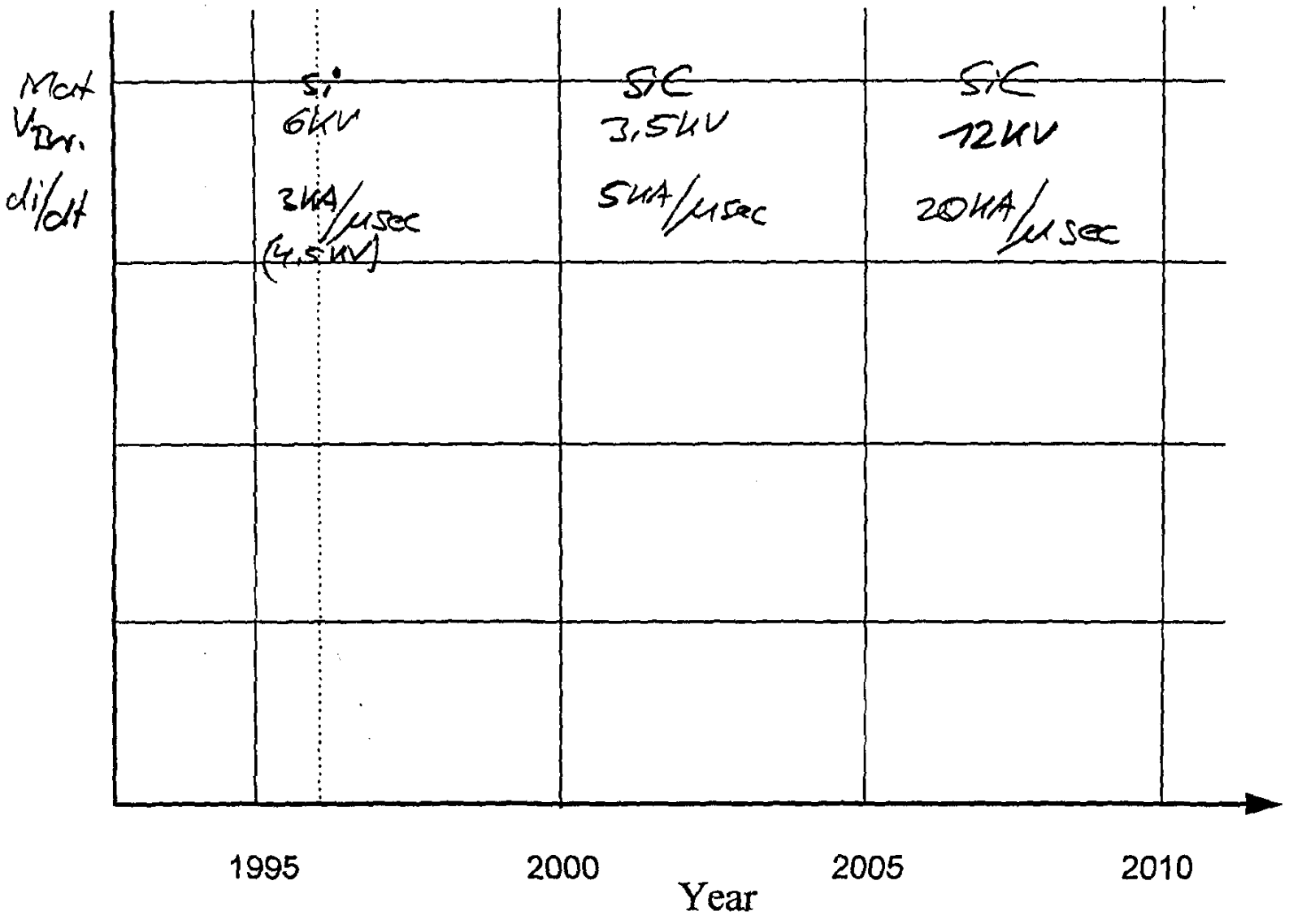
GTO Roadmap


Mat
VB
IN
Losses
turn off
Si
4 - 6kV
4 - 6kA
Esbli + Redya
hard driven
Fine Pattern
Bevelling
Snubbeless
transparent Emitter
ST
6"
Package
see Thyr.
Si
8kV
6kA
hard driven
snubberless
IGBT
SiC
MOS
1995
2000
2005
2010
Year

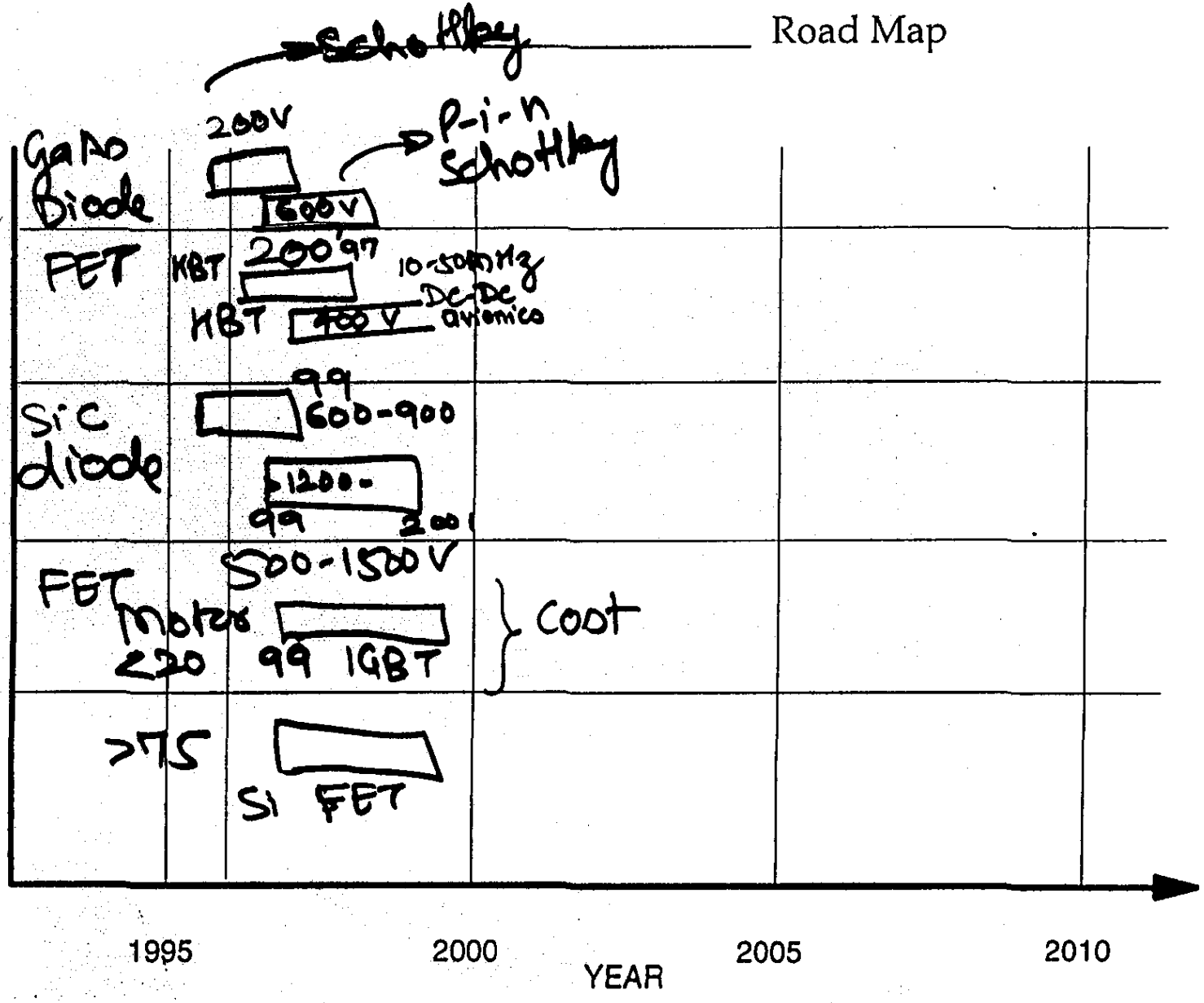
MOS-Controlled Device Roadmap



Diode Roadmap



Road Map


Schottky
GaAs Diode
200V
p-i-n Schottky
1600V
FET
HBT
200
97
10-30 MHz
DC-DC
avionics
HBT
99
SiC diode
600-900
1200-
99
500-1500V
FET
motor
<20
99
IGBT
Cost
>75
Si FET
1995
2000
2005
2010
YEAR