THE 11TH INTERNATIONAL SYMPOSIUM ON
POWER SEMICONDUCTOR DEVICES AND ICs

ISPSD '99

Advance Program

Crowne Plaza
Toronto, Ontario, Canada
May 26-28, 1999

Sponsor: IEEE Electron Devices Society
Co-Sponsor: The Institute of Electrical Engineers of Japan

Page

On behalf of the Conference Committee, I would like to invite you to the 11th International Symposium on Power Semiconductor Devices and IC's (ISPSD99). Following the overwhelming success of last year's meeting in Kyoto, Japan, the Symposium once again returns to North America, specifically to Toronto, Ontario, Canada.

The strong international nature of our industry and the broad range of topics covered by the Symposium are evident in the invited and contributed papers originating from around the world.

The plenary invited talks on Wednesday feature the following presentations.

- From Japan, T. Watanabe will address "Trend of Railway Technologies and Power Semiconductor Devices".

- From Europe, L. Lorenz will discuss "COOLMOS - a New Milestone in High Voltage Power MOS"; as well, P. Leturcq will talk about "Power Semiconductor Device Modeling Dedicated to Circuit Simulation".

- From North America, F. Lee will discuss "'Power Management Issues for Future Generation Microprocessors".

The invited speaker at the Banquet on Thursday is: Dr. Alexander Lidow, President and CEO, International Rectifier Corporation, El Segundo, California.

From 121 submitted abstracts, 36 papers were accepted for oral presentation with another 40 accepted as poster session papers. The global character of ISPSD99 is reflected by submissions originating from 17 countries; 38% of the papers submitted were from North America, 31% from Europe, 18% from Japan and 13% from the rest of the world. Submissions were equally divided between University and Industry. Student papers submitted are eligible for a "Best Student Paper Award".

It is with great pleasure that I thank the ISPSD99 Organizing and Technical Program Committees and specially the Technical Program Committee Chair, Taylor Efland, for their outstanding efforts in planning the Symposium. We are all looking forward to welcoming you in Toronto.

C. Andre T. Salama
General Chair, ISPSD99

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Symposium Date & Site

Dates: May 26-28, 1998

Location: Crowne Plaza Toronto Centre
325 Front St. W.
Toronto, Ontario, Canada
M5V 2X3
Phone: 416-597-1400
Fax: 416-597-8128

Sponsorship

ISPSD99 is sponsored by the Electron Device Society (EDS) of the Institute of Electrical and Electronic Engineers (IEEE). It is co-sponsored by the Institute of Electrical Engineers of Japan (IEEJ). The IEEE holds the copyright of the ISPSD99 proceedings.

Official Language

The official language of the ISPSD is English. There will be no facilities for simultaneous translation.

Web Site

For further information on the conference, please visit the website at: www.utoronto.ca/ispsd99/

Advance Registration

Your booklet contains a mailer for

- ISPSD99 Conference registration
- Hotel reservation
- HV and Power IC Design Short Course registration

Please fax the information as soon as possible. ISPSD participants are encouraged to stay on location at the Crowne Plaza. Competitive hotel room rates have been arranged especially for ISPSD99 participants and their guests. Since the number of available rooms is limited, early hotel registration is encouraged.

Conference Registration

Your ISPSD99 conference registration includes your program proceedings, one ticket to the conference reception, and one ticket to the banquet dinner. The conference registration includes admission to the plenary session, all of the regular technical sessions and the poster session. Enrolment in the short course preceding ISPSD is additional.

Extra tickets to the reception and the dinner and additional copies of the proceedings may be ordered on the attached registration form or may be obtained at the on-site registration desk. Attendees are encouraged to bring families and friends to the evening reception and dinner. We would appreciate early purchase of the evening event tickets to better assist us in planning these functions.

Registrations forms should be faxed directly to:

ISPSD99 Registration
c/o Micronet
University of Toronto
10 King's College Road
Toronto, Ontario, Canada M5S 3G4
Fax: 416-978-4516

and must be received **prior to April 1, 1999**.

To simplify registration, only one form needs to be faxed to register for the Conference, to reserve rooms at the Hotel and to register for the short course.

Registration Fees

To simplify financial transactions all payments must be made by credit card (American Express, Mastercard, or Visa only). Please make sure to include credit card expiration date and signature on the registration form in addition to card type and card number. Registration forms must be faxed to ISPSD99 Registration at 416-978-4516.

If you have difficulties using credit card payments, please contact the Conference General Chair C.A.T. Salama at: Fax 416-978-4516 or email: salama@vrg.utoronto.ca

The schedule of fees in Canadian dollars* is as follows:

Registration	Before April 1	After April 1
IEEE/IEEJ member	$700	$800
Non IEEE/IEEJ member	$800	$900
IEEE/IEEJ student	$350	$400
Non IEEE/IEEJ student	$400	$450
Extra Reception tickets	$60	$60
Extra Dinner tickets	$100	$100
Extra Proceedings	$75	$75

Members of the press receive complementary conference registration. All other attendees including speakers and session chairs please use the above fees table. Students will be required to show evidence of their status at the registration desk.

* Canadian dollar approximate exchange rates:
$1 Can = $0.65 (US Dollar)
$1 Can = ¥ 75 (Japanese Yen)
$1 Can = € 0.55 (Euro)

Hotel Reservations

Reservations for the Crowne Plaza Hotel (Toronto, Canada) must be made by fax using the attached reservation form. For other hotel related information, please call the Hotel directly at 416-597-1400. Room rates vary by category as follows:

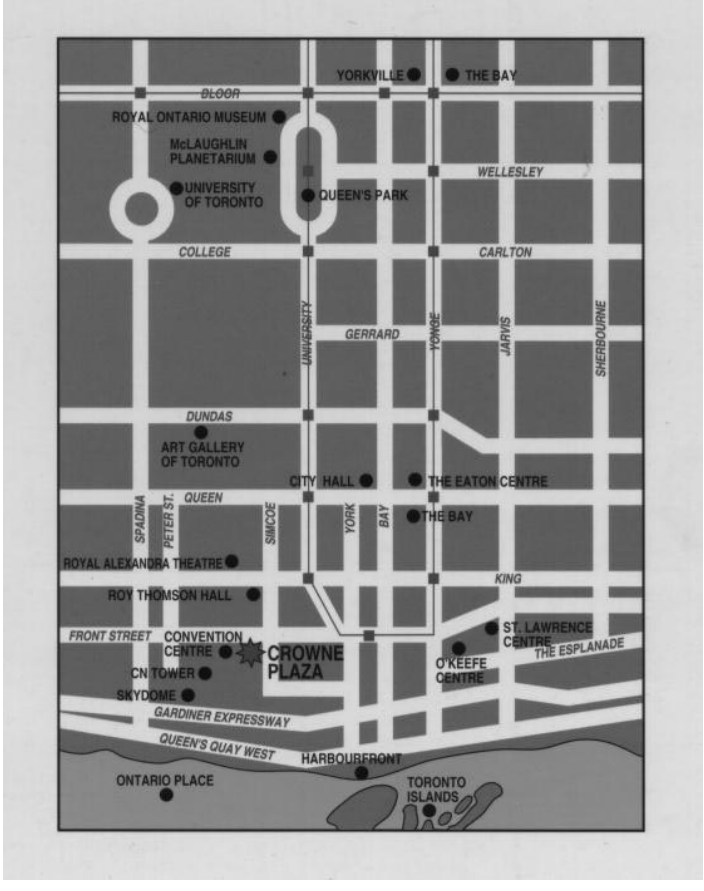
ROOM CATEGORY	RATE IN CAN $
Standard	$209
Deluxe	$219

All rates are based on single or double occupancy and are subject to applicable taxes.

Quoted ISPSD99 rates are in effect from May 24 to May 29, 1999. Reservations or extensions outside these dates will be confirmed at published rack rates. Reservations must be guaranteed by a one (1) night deposit accompanying the reservation request form. The deposit must be made by credit card. **Deadline for reservations is April 1, 1999.**

Guests may check into the hotel after 3:00 PM on the arrival date and check-out no later then 12:00 noon on the departure date. Early arrivals will be checked-in based on room availability. Late check-out requests should inquire at the front desk.

Location of the Hotel



Registration Desk

The ISPSD99 conference will be held in the Ballroom meeting facility of the Crowne Plaza located on the lower level of the hotel. The registration desk on the lower level will be open on the evening prior to the conference and during the duration of the symposium. Information, additional proceedings and extra event tickets will be available at this desk. Desk hours will be as follows:

Tuesday, May 25, 1999	5:00 PM to 8:00 PM
Wednesday, May 26, 1999	7:30 AM to 5:00 PM
Thursday, May 27, 1999	7:30 AM to 5:00 PM
Friday, May 28, 1999	7:30 AM to 12:00 NOON

Presentations

All oral presentations will use overhead projection viewgraphs.

Meeting Facilities

All the papers will be presented in the Ballroom meeting facilities on the lower level of the Hotel.

Speaker's Preparation Room

A speaker's preparation room, located in the Simcoe room directly adjacent to the Ballroom, will be open for the duration of the conference.

Air Transportation

Over 20 major airlines offer regularly scheduled flights in and out of Toronto Lester B. Pearson International Airport. The Airport is located approximately 25 km (15 miles) from downtown Toronto (45 minutes car ride). Information booths are located throughout the terminals and baggage claim areas.

Transportation to and from the Airport

Airport Express provides frequent bus service from all terminals of the Lester B. Pearson Airport to downtown Toronto. At the arrivals level of the airport, travellers can purchase tickets (rates are approximately $12 one way, $20 return) for a bus which stops at all major downtown hotels, including the Crowne Plaza.

Taxis are also available from the arrivals level of the airport. Follow signs on that level for a taxi or limousine. Rates are approximately $35.00 for a taxi or $40.00 for a limousine from the airport to the Crowne Plaza.

Car Rental

Car rentals are available at the airport or at the hotel from a number of suppliers such as Hertz (800-620-9620), Avis (800-879-2847), National (800-387-4747) and Budget (800-622-1000). Make reservations in advance.

Weather

May is mild during the day and cool at night. Medium weight clothing is your best bet. The average daily minimum/maximum temperatures in Toronto vary between 10°C and 20°C.

Toronto

Toronto, as the venue of the conference, is one of North America's fastest growing cities and is a vibrant and exciting cosmopolitan city with a multitude of sights to see and places to go. The name Toronto, from a Huron word meaning "place of meeting", is just as appropriate today for this bustling metropolis as it was hundreds of years ago when Native Canadians would gather here while travelling between the Upper and Lower Lakes. The city is full of contrasts -

The soaring glass and concrete towers of the commercial and financial heart of Canada mingle with parks, gardens and village style ethnic neighborhoods that are microcosms of the lands recent immigrants to the city left behind. The city offers an excellent choice of restaurants and shopping amenities and is the home of two major league teams the baseball Toronto Blue Jays and the basketball Toronto Raptors. The rich texture of Toronto's demographics is reflected in its active arts community. After New York and London, Toronto has more theatres than any other city in the world, and it has many outstanding museums and art galleries. In addition, it is one of the safest cities of its size - nearly 3 million people.

Crowne Plaza Toronto Centre

The Crowne Plaza (Toronto Centre) Hotel, where the conference will be held, is located in downtown Toronto, and features 587 guest rooms and suites. The Hotel is in the heart of the business, shopping and theatre districts and offers excellent dining facilities, room service, valet parking, a complete recreation club with a heated indoor pool and outstanding conference facilities. In addition, the hotel is located within a block of the magnificent SkyDome sports and entertainment complex. As a point of interest, the Crowne Plaza Centre is also located steps from the CN Tower, the world's tallest freestanding structure with the world's highest observation galleries. The CN Tower offers a variety of activities for the whole family. Close to the Hotel are many other popular local attractions including Harbourfront, the Hockey Hall of Fame, the O'Keefe Centre, Roy Thomson Hall, the Princess of Wales and Royal Alexandra Theatres, the Fashion District and over 100 clubs and restaurants.

Sightseeing

Information on various tours of Toronto and the surrounding areas including Niagara Falls and Niagara on the Lake and the wine country of southern Ontario is available from the concierge in the main lobby of the Hotel. **For the most complete and up-to-date information on Toronto, visit the website: www.tourism-toronto.com.**

High Voltage and Power IC Design Short Course

A one day short course on "High Voltage and Power IC Design" will be held prior to the Symposium on Tuesday May 25, 1999, from 8:00 a.m. to 5:00 p.m. in the Kingsway Room.

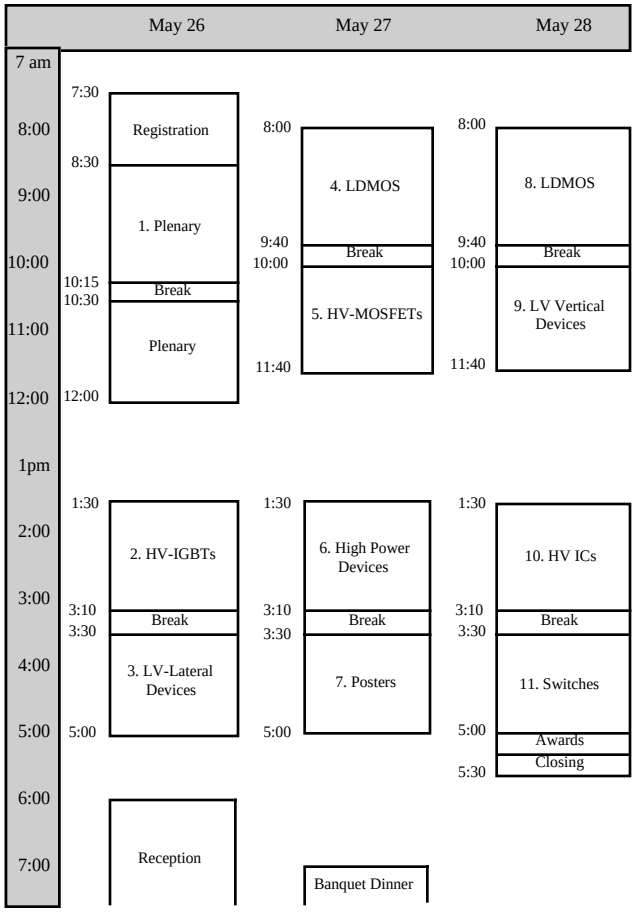
Course Outline

The course is intended for students, engineers, scientists, and managers working on the design of high voltage and power ICs.

- **Process Technology Options**
  - Lecturer: C. Andre T. Salama, University of Toronto
  - Introduction, isolation, resurf, integrable power devices, IC technology options, device cross talk, future trends.
- **Device and Layout Design Issues**
  - Lecturer: Taylor Efland, Texas Instruments
  - Categories and types of modern BiCMOS power devices, interconnect effects, large transistor systems, integrated protection.
- **Motor Drive Building Block Design**
  - Lecturer: David Tam, International Rectifier
  - Motor drive system architectures, controllers, gate drivers, current sensors, inverter power stages, converter power stages, architectures and chipsets for low and high power drives.
- **Automotive Building Block Design**
  - Lecturer: Richard Williams, Analogic
  - Power electronics in automobiles, electrical and thermal environments. High side switches, low side switches, H-bridge drivers. Complex systems: automatic braking, air bags.
- **Telecom Building Block Design**
  - Lecturer: Mehran Aliahmad, Quantum
  - HVICs in present and future local access networks; subscriber line interfaced circuits; choice of technology; building blocks; line drivers, op amps, sense amplifiers, switches and control circuits; protection issues.

Fees: $750 Can for registration received before April 1, 1999; $800 after April 1, 1999. Fees include course material, luncheon, and beverage breaks.

Registration: Please complete attached registration form, and fax to 416-978-4516. Enrolment will be limited to the first 30 applicants.



PLENARY

8:30 -12:00 noon, Wednesday

Chairs: T. Efland, Texas Instruments
S. Benes, Schneider

FORMAL OPENING OF CONFERENCE (8:30)

OPENING REMARKS

C.A.T. Salama, University of Toronto
General Chair, ISPSD99

INVITED PAPERS

1.1 8:45 - 9:30

COOLMOS™ - A New Milestone in High Voltage Power MOS

L. Lorenz, G. Deboy, A. Knapp, M. März
Siemens AG, Semiconductor Division, Germany

The COOLMOS™ technology – developed for the production of charge compensated devices – is presented. Due to its novel internal structure the device offers a dramatic reduction of the on-resistance with a completely altered voltage dependence of the device capacitances. The ruggedness aspects such as avalanche and short circuit behavior are excellent and reach the limit of active zener clamped devices. The above mentioned electrical features recommend the device for a broad application range. The paper will also discuss device physics based selection criteria for fast IGBTs and COOLMOS.

1.2 9:30 - 10:45

Trend of Railway Technologies and Power Semiconductor Devices

T.Watanabe
Railway Technical Research Institute, Japan

Transportation has a big share in energy consumption especially in case of automobiles. Transportation volume will rapidly increase in the coming twenty first century. On the other hand environmental issues become imminent and methods to cut carbon dioxide dissipation of concern. Railways save energy in the field of mass freight transportation, commuter services and high speed passenger transportation. Shifting transportation from roads and automobiles to railways is important to settle future energy and environmental issue.

Inverters have made a great progress due to power semiconductor development. The smaller power converter offers the more passenger space in passenger vehicle and the more productivity.

If 10-40kV power semiconductors are made, we can have a prospect to realize transformerless railway vehicles for 25kV a.c. system by adding the role of a main transformer of traction circuit to converters.

In addition, electric vehicles with accumulator, hybrid vehicles using both engine and accumulator and cars with fuel cells are discussed for future environment friendly automobiles. Electric traction seems unavoidable for future automobiles which means huge markets for power converters and power semiconductor devices in 21st century.

BREAK **10:15 - 10:30**

1.3 10:30 - 11:15

Power Semiconductor Device Modeling Dedicated to Circuit Simulation

P. Leturcq
Laboratoire d'Analyse et d'Architecture des Systèmes du C.N.R.S, Toulouse, France

Until recently, power semiconductor device models drawn up for circuit simulation were mainly of the behavioral type. The main worries of power electronics specialists were the improvement of the power conditioning circuit topologies and control strategies, hardware problems being preferably solved at the prototyping stage by way of cut and try approaches.

The present needs for smaller, lighter, cheaper and more efficient equipment, imply an increase in operating frequency and in functional complexity, and now call for new design methodologies avoiding prototyping, at least partly. Thus, a priori evaluations by means of simulation for dI/dt and dV/dt, current or voltage overshoots and power dissipation become of special concern when designing power circuits. However, existing semiconductor models and simulation softwares, have a number of difficulties : - long simulation time; - convergence problems; - inaccuracy of results

As a matter of fact, most power semiconductor models currently available either are derived from the field of microelectronics (and are unable to predict the transient characteristics of high voltage devices, specially in the case of bipolar devices, due to the weakness of quasi-static approximations frequently involved in the model derivation), or are based on finite elements descriptions (and are cumbersome to handle, owing to their extreme physical and numerical complexity)

The aim of the paper is to recall the problematic of circuit simulation in the field of power electronics and to critically review the recent approaches to semiconductor device modeling for that purpose.

1.4 11:15 - 12:00

Power Management Issues for Future Generation Microprocessors

F. C. Lee and X. Zhou
Virginia Polytechnic Institute and State University
Blacksburg, VA , USA

In order to meet ever increasing demands of speed and efficiency of dataprocessing system, modern microprocessors are being designed with lower logic voltage 1.1V~1.8V, higher load 50A~100A and significantly higher operating frequencies, above 1GHz. These future generation microprocessors need aggressive power management, employing voltage regulator module (VRMs) to provide well regulated voltage with higher current capability and much faster transient responses.

As the speed of the processor increases, the demand for higher current slew rate at VRM output posses a major technical challenge. These higher current slew rates are encountered when the system is transition from the sleep mode to the active mode and vice versa. With the higher current slew rate, the interconnect parasitic impedance and the ESR and ESL of capacitors have dramatic effects on the VRM voltage regulation under dynamic load transients. Most of today's VRMs use the conventional buck or synchronous rectifier buck topology. In future microprocessor applications, these conventional VRM topologies can no longer meet the challenges. VRM with significantly high efficiency, higher power-density and faster transient must be developed. To achieve this target, a number of critical issues have to be addressed. Besides device technology, innovative power system architectures should be developed, which can meet the new performance envelop and in the meantime offers a cost effective solution. Advanced VRM topologies for fast transient response and low ripple voltage together with advanced packaging technologies for improving power density and thermal management are among those important issues to be addressed.

HV – IGBTs

1:35 – 3:15 PM, Wednesday

Chairs: Leo Lorenz, Siemens
Steve Robb, Motorola

This session will center on characterization and new developments in a variety of IGBTs.

2.1 1:35 – 2:00

Static and Dynamic Thermal Characteristics of IGBT Power Modules
C. Yun*, P. Regli*, J. Waldmeyer**, and W. Fichtner*
*ETH, Switzerland
**ABB, Switzerland

2.2 2:00 – 2:25

High performance Wide Trench IGBTs for motor control applications
A.Bhalla, J. Gladish, A. Polny, P. Sargeant, and G. Dolny
Harris Semiconductor, USA

2.3 2:25 – 2:50

Fabrication of a Double-sided IGBT by Very Low Temperature Wafer Bonding
K. D. Hobart*, F.J. Kub*, G. Dolny**, M. Zafrani**, J.M.Neilson**, J. Gladish**, and C. McLachlan**
*Naval Research Laboratory, USA
**Harris Semiconductor, USA

2.4 2:50 – 3:15

Large Reverse Biased Safe Operating Area for a Low Loss HiGT
Y. Uchino, H. Kobayashi, M. Mori, and R. Saito
Hitachi, Japan

BREAK **3:15- 3:30**

SESSION 3
Ballroom

LV – ENERGY CONSIDERATIONS FOR LATERAL DEVICES

3:30 – 5:10 PM, Wednesday

Chairs: Akio Nakagawa, Toshiba
Claudio Contiero, ST Microelectronics

Problematic current flow along with device styles are discussed with respect to lateral DMOS safe operation. Additionally copper is looked at with respect to energy considerations and application to power devices.

3.1 3:30 - 3:55
SOA Considerations in LDMOS Transistors
P. Hower, J.Lin, S. Haynie, S. Paiva, R.Shaw, and N. Hepfinger
Unitrode, USA

3.2 3:55 – 4:20
20 V LDMOS Optimized for High Drain Current Condition Which is better, n-epi or p-epi?
K. Kinoshita, Y. Kawaguchi, T. Sano, and A. Nakagawa
Toshiba, Japan

3.3 4:20 – 4:45
Cu Layer Approach for Enhancement of Power Device Energy Capability
Y.S. Chung, T. Willett, V. Macary, S. Merchant, and A. Baird
Motorola, USA

3.4 4:45 – 5:10
Efficiency of Power Devices using Full Cu Metallization Technologies
E. Kobori, N. Izumi, N. Kumamoto, Y. Hamazawa, M. Matsumoto, K. Yamamoto, and A. Kamisawa
Rohm, Japan

EVENING RECEPTION Wednesday, 6:00 PM

LV – ADVANCES IN LDMOS

8:00 – 9:40 AM, Thursday

Chairs: Rainer Constaple, Daimler Benz
Jack L Glen, Delco

This session will present advances in lateral DMOS devices, both from the point of view of new device design and design optimization.

4.1 8:00 - 8:25
A New Concept for the Lateral DMOS Transistor for Smart Power IC's
M. Zitouni*, F. Morancho*, P. Rossel*, J. Buxo**, I. Pages***
*LAAS-CNRS, France
**Motorola, USA
***Motorola, France

4.2 8:25 – 8:50
0.35mm, 68mWcm2 Power MOSFET to Power Future Microprocessor
N.X. Sun, A.Q. Huang, and F.C. Lee
Virginia Power Electronics Center, USA

4.3 8:50 – 9:15
Self-aligned and Shielded-Resurf LDMOS for dense 20V Power IC's
A.W. Ludikhuize
Philips Research Laboratories, The Netherlands

4.4 9:15 – 9:40
Split Gate MOSFETs in BiCMOS Power Technology for Logic Level Gate Voltage Application
A. Tsai, T. Efland, and S. Pendharkar
Texas Instruments, USA

BREAK 9:40- 10:00

SESSION 5
Ballroom

HV – MOSFETS

10:00 – 11:40 AM, Thursday

Chairs: Yoshitaka Sugawara, Kansai Electric
Wolfgang Fichtner, ETH

This session is about new methods of MOSFET realization. CoolMOS, RESURF and SiC are discussed.

5.1 10:00 - 10:25
Properties of COOLMOS between 420 K and 80 K — the Ideal device for Cryogenic Applications
A. Schlogl*, G. Deboy*, U. Linnert*, H.W. Lorenzen**, H.J. Schulze*, and J.P. Stengl*
*Siemens, Germany
**Technical University of Munich, Germany

5.2 10:25 – 10:50
Predicted Electrical Characteristics of 4500V Super Multi-Resurf MOSFETs
Y. Kawaguchi, K. Nakamura, and A. Nakagawa
Toshiba, Japan

5.3 10:50 – 11:15
Analysis of the Effect of Charge Imbalance on the Static and Dynamic Characteristics of the Super Junction MOSFET
P. M. Shenoy, A. Bhalla, and G.M. Dolny
Harris Semiconductor, USA

5.4 11:15 – 11:40
Electrical Performance of Triple Implanted Vertical Silicon Carbide MOSFETs with Low On-Resistance
D. Peters, P. Friedrichs, R. Schorner, H. Metlehner, B. Weis, and D. Stephani
Siemens, Germany

SESSION 6
Ontario - Niagara Room

HV – HI POWER DEVICES

1:35 – 3:15 PM, Thursday

Chairs: Phil Hower, Unitrode
Shin-ichi Shinohara, Origin

The reliability of high power IGBT modules is discussed along with higher power diodes.

6.1 1:35 – 2:00
Advanced High Current, High Reliable IGBT Module with Improved Multi-Chip Structure
R. Saito, Y. Koike, A. Tanaka, T. Kushima, H. Shimizu, S. Nonoyama
Hitachi, Japan

6.2 2:00 – 2:25
Application of High Resolution Strain and Temperature Mapping on the Reliability of Wirebonds in IGBT-Based Power Modules
V. Mehrotra, J. He, M .S. Dadkhah, R. C. Addison, K. Rugg, M. C. Shaw
Rockwell, USA

6.3 2:25 – 2:50
A Planarized High Voltage Silicon Trench Sidewall Oxide-Merged PIN/Schottky (TSOX-MPS) Rectifier
R. N. Gupta*#, W.G. Min*, T. P. Chow*, H. R. Chang#, C. Winterhalter#
*Rensselaer Polytechnic Institute, USA
#Rockwell, USA

6.4 2:50 – 3:15
4.5 kV-Fast-Diodes with Expanded SOA Using a Multi-Energy Proton Lifetime Control Technique
O. Humbel**, N. Gaister*, F. Bauer*, W. Fichtner**
*ABB, Switzerland,
**ETH, Switzerland

BREAK **3:15- 3:30**

POSTER SESSION

3:30 – 5:10 PM, Thursday

Chairs: Yearn-Ik Choi, Ajou University
Duncan Grant, Bristol University

7.1 Analysis on the Self-Clamp Phenomena of IGBTs
M. Takei, T. Fujihira
Fuji, Japan

7.2 Explosion Tests on IGBT High Voltage Modules
S. Gekenidis, E. Ramezani, H. Zeller
ABB, Switzerland

7.3 A New Trench Bipolar Junction Diode (TBJD)
B. You*, A.Q. Huang*, J.K.O. Sin**
*Virginia Tech, USA
**HK Univ. Sci. & Tech., P.R. China

7.4 Static and Dynamic Characteristics of a 1100V Double P-Type Implanted, Planar 4H-SiC PiN Rectifier
V. Khemka, R. Patel, N. Ramuguul, T. P. Chow, and R.J. Gutmann
Rensselaer Polytechnic Institute, USA

7.5 1.2KV, 25 A, PT and NPT Trench IGBTs with Optimum Forward Characteristics
S.S.M. Chan*, F. Udrea**, P. R. Waind*, T. Trajkovic**, J. Thomson*, M. Rahimo*, S. Huang**, G.A.J. Amaratunga**, A. E. Crees*
*Mitel Semiconductor, U.K.
**Cambridge University, U.K.

7.6 Ultra-High Resolution Temperature Measurement and Thermal Management of GHz Power Devices using Heat Pipes
J. He, V. Mehrotra, M. C. Shaw
Rockwell, USA

7.7 The Recessed-gate IGBT Structure
M. Nemoto**, B.J. Baliga*
*North Carolina State University, USA
**Fuji, Japan

POSTER SESSION

7.8 A Comparative Study of High Voltage (4kV) Power Rectifiers P+iN/MPS/SSD/SPEED
S. Sawant, B.J. Baliga
North Carolina State University, USA

7.9 A New High Voltage Integrated Switch: The Thyristor Dual”
J.-L. Sanchez, M. Breil, P. Austin, J. P. Laur, J. Jalade, B. Rousset, H. Foch
LAAS, France

7.10 High Voltage Ni/4H-SiC Schottky Rectifiers
R.K. Chilukuri, B.J. Baliga
North Carolina State University, USA

7.11 A Fully Planarized 4H-SiC Trench MOS Barrier Schottky (TMBS) Rectifier
V. Ananthan, V. Khemka, and T. P. Chow
Rensselaer Polytechnic Institute, USA

7.12 A Physics-Based Model for the Avalanche Ruggedness of Power Diodes
G.A.M. Hurks, and N.Koper
Philips Semiconductor, The Netherlands

7.13 A New Wide SOA DC-EST Structure with Diode Diverter
S. Sawant, B.J. Baliga
North Carolina State University, USA

7.14 A Novel IGBT Chip Design Concept of High Turn-off Current Capability and High Short Circuit Capability for 2.5kV Power Pack IGBT
K. Yoshikawa, T. Koga, T. Fujii, T. Katoh, Y. Takahashi, and Y. Seki
Fuji, Japan

POSTER SESSION

7.15 MOS Bipolar Gate IGBT Operation
M.D. Bobde, T. Minato, N. Thaper, B.J. Baliga
North Carolina State University, USA

7.16 Characterization of Silicon Direct Bonding Methodology for High Performance IGBT
C.M. Yun, T.H. Kim, S.S. Kim, Y.D. Kwon, and H.W. Jang
Samsung, Korea

7.17 The Effect of Charge in Junction Termination Extension Passivation Dielectrics
J.R. Trost, S.Arthur, R.S. Rodley, Sr.
H. Evans, M.K. Khan, and T. Grebs
Harris Corporation, USA

7.18 A New Differential Backside Laserprobing Technique for the Investigation of the Lateral Temperature Distribution in Power Devices
C. Furbock*, R. Thalhammer**, M. Litzenberger*, N. Seliger,***G. Wachutka**, and E. Gornik*
*Institute for Solid State Electronics, Austria
**Technical University of Munich, Germany
***Siemens, Germany

7.19 Reliability Problems due to Ionic Conductivity of IC Encapsulation Materials under High Voltage Conditions
R.T.H. Rongen*, H.J. Bruggers*, C.P. Meeuwsen*, A.W. Ludikhuize**,
* Philips Semiconductors, The Netherlands
**Philips Research, The Netherlands

7.20 Low On-Resistance Lateral U-Gate MOSFET with DSS Pattern Layout
Y. Shimoida, Y. Hayami, K. Ohta, M. Hoshi, T. Shinohara
Nissan, Japan

7.21 An Improved power VDMOSFET Using a Split Well Structure
J. Zedng , C.F. Wheatley
Harris, USA

SESSION 7
Ballroom
ISPSD 99

POSTER SESSION

7.22 2.5 V-Driven N channel 3rd Generation Trench Gate MOSFET
A. Osawa, Y. Kanemaru, N. Matsuda, T. Yoneda, H. Matsuki, Y. Usui, and Y. Baba
Toshiba, Japan

7.23 The Lateral Dual Channel Emitter Switched Thyristor Employing The Segmented P-Base
D.S. Byeon*, J.K. Oh*, Y.S. Lee*, M.K. Han*, Y.I. Choi**
*Seoul Nat'l Univ, Korea
**Ajou Univ., Korea

7.24 A New Model for Dopant Redistribution in a Power SOI Structure
T. Ishiyama*, S. Matsumoto*, T. Yachi*, W. Fichtner**
*NTT, Japan
**NTT, Switzerland

7.25 RF LDMOSFET with Graded Gate Structure
S. Xu, P.D. Foo
Institute of Microelectronics, Singapore

7.26 High-Performance 13-65V Rated LDMOS Transistors in an Advances Smart Power Technology
S. Merchant, R. Baird, S. Chang, P. Hui, G. Neaves, and V. Macary
Motorola, USA

7.27 The Maximum Controllable Current of The Base Resistance Controlled Thyristor Employing Self-Aligned Corrugated P-Base
D. S. Byeon*, Y. S. Lee*, J. K. Oh*, M. K. Han*, Y. I. Choi**
*Seoul Nat'l University, Korea
**Ajou University, Korea

7.28 Electro-Thermal instability in low voltage Power MOS: Experimental characterization
A.Breglio, F. Frisina, A. Magri, P. Spirito
University of Naples, Italy

POSTER SESSION

7.29 Industrial Relevance of Deep Junction Produced by Rapid Thermal Processing for Power Integrated Circuits
J-M. Dilhac*, L. Cornibert**, S. Roux*, C. Ganibal*
*LAAS-CNRS, France
**SGS-Thomson, France

7.30 Integrated Design Environment for DC/DC Converter FET Optimization
R. Sodhi, S. Brown Sr., D. Kinzer, R. Martinez, M. Wiener
International Rectifier, USA

7.31 Comparison of RF Performance of VDMOS and LDMOS
M. Trivedi, K. Shenai
University of Illinois, USA

7.32 High Performance Extended Drain MOSFETs (EDMOSFETs) with Metal Field Plate
M. Lee, and O. Kwon
Hanyang University, Korea

7.33 The Behavior of Digital Circuits under Substrate Noise in a Mixed Signal Smart Power Environment
R. M. Secareanu*, I. S. Kourtev*, J. Becerra**, T. E. Watrobski**, C. Morton**, W. Staub**, T. Tellier, E. G. Friedman**
*University of Rochester, USA
**Xerox Corporation, USA

7.34 Thermal Simulation During Transient Operation of Power Devices with Cu Layer
Y.S. Chung
Motorola, USA

7.35 A Novel Dual Gated lateral MOS-Bipolar Power Device
S. Hardikar*, E.M.S. Narayanan*, M.M. De Souza*, A.Q. Huang**, G. Amaratunga***
*De Montfort University, U.K.
**Virginia Polytechnic Institute, USA
***University of Liverpool, U.K.

POSTER SESSION

7.36 Forward Drop-Leakage Current Tradeoff Analysis of a Junction Barrier Schottky (JBS) Rectifier
Z. Hossain, D. Cartmell, G. Dashney
Motorola, USA

7.37 A Simple Mobility Model for electrons and Holes
I.Takata
Mitsubishi, Japan

7.38 Current Redistribution in IGBTs During Turn-Off
J.C. Joyce. P.R. Palmer
Cambridge University, UK

7.39 A First Approach on Parallel-Monitor Integration Circuit for Energy-Capacitor-System (ECS)
Y. Yamamoto*, M. Horii*, M. Mitome**, S. Fujimoto**, M. Yamagish***, M. Shinotsuka***, M. Okamura****
*Tamagawa University, Japan
**Nihon Inter, Japan
***Power Systems, Japan
****Okamura, Japan

7.40 A New Current Measuring Principle for Power Electronic Applications
N. Karrer, P. Hofer-Noser
ETH, Switzerland

BANQUET DINNER Thursday, 7:00 PM
BALLROOM

ISPSD 99 General Chairman: C.A.T. Salama
Guest Invited Speaker - Dr. Alexander Lidow, President and CEO, International Rectifier Corporation, El Segundo, California

LV – ADVANCES IN LDMOS

8:00 – 9:40 AM, Friday

Chairs: Adrian W. Ludikhuize, Philips Research
Steven L Merchant, Motorola

The first two papers discuss power ICs for plasma display panels . The last two papers propose a HV high frequency bipolar transistor and a submicron silicon carbide CMOS for smart power applications.

8.1 8:00 - 8:25
SOI High Voltage Integrated Circuit Technology for Plasma Display Panel Drivers
S.S. Lee**, M.R. Lee*, I.H. Lee**, I.S. Yang**, J.H. Paek**, L.Y. Hwang**, J.I.Ju**, B.H. Lee**, C. Lee**, and O. Kwon*
*Hanyang University, Korea
**LG Semicon, Korea

8.2 8:25 – 8:50
A Power IC Technology with Excellent Trench Isolation and P-LDMOS Through Tapered TEOS Field Oxides
S. Kim, J. Kim, J. Koo, D.Y. Kim
Electronics & Telecommunications Research Institute, Korea

8.3 8:50 – 9:15
High Voltage High Frequency Silicon Bipolar Transistors
D. Gradinaru, W.T. Ng, C.A.T. Salama
University of Toronto, Canada

8.4 9:15 – 9:40
Submicron Silicon Carbide CMOS for SmartPower Applications
K.T. Kornegay
Cornell University, USA

BREAK **9:40- 10:00**

LV – LOW VOLTAGE VERTICAL DEVICES

10:00 – 11:40 AM, Friday

Chairs: Mike A. Briere, Cherry Semiconductor
Paolo Spirito, University of Napoli

This session is about low voltage vertical power MOSFETs with low on resistance. The first papers talk about advances in trench devices, while the last talks about a circuit breaker power IC.

9.1 10:00 - 10:25
Ultra-Low Rdson 12 Volt P-channel Trench MOSFET
R. Carta, D. Asselanis, D. Kinzer
International Rectifier, USA

9.2 10:25 – 10:50
High-Density Ultra-low Rdson 30 Volt N-Channel Trench FETs for DC/DC Converter Applications
R. Sodhi, R. Malik, D. Asselainis, D. Kinzer
International Rectifier, USA

9.3 10:50 – 11:15
Expanding the Operating Voltage Range of Trench-Gated Vertical DMOS
R.K. Williams, W. Grabowski
Analogic, USA

9.4 11:15 – 11:40
A New Circuit-Breaker Integrated Device for Protection Applications
J-P Laur, J. L. Sanchez, M. Marmouget, P. Austin, J. Jalade, M. Breil, M. Roy
ST Microelectronics, France

SESSION 10
Ballroom

HV – HVICs

1:35 – 3:15 PM, Friday

Chairs: Roland Sittig, Technical U. Braunschweig
Ikunori Takata, Mitsubishi

High voltage integrated circuits and integration techniques are discussed.

10.1 1:35 – 2:00
Improvement in Lateral IGBT Design for 500V 3A One Chip Inverter ICs
A.Nakagawa, H. Funaki, Y. Yamaguchi, F. Suzuki
Toshiba, Japan

10.2 2:00 – 2:25
600V Power Conversion System-on-a-Chip Based on Thin Layer Silicon-on-Insulator
T. Letavic, M. Simpson, E. Arnold, E. Peters, R. Aquino, J. Curico, S. Herko, S. Mukherjee
Philips Electronics, USA

10.3 2:25 – 2:50
A New High Energy Implantation Based Technology for Power Integrated Circuit Devices
D. Patti
ST Microelectronics, Italy

10.4 2:50 – 3:15
New High Voltage Integrated Circuits Using Self-Shielding Technique
T. Yamazaki, N. Kumagai, K. Oyabe,
A.Tada, H. Takeda, Y. Seki, K. Sakurai
Fuji, Japan

BREAK 3:15- 3:30

SESSION 11
Ballroom

HV – CONTROLLED SWITCHES

3:30 – 5:10 PM, Friday

Chairs: T. Paul Chow, Rensselaer Poly. Institute
Hans Rudolf Zeller, ABB Semiconductors

Various new three terminal high voltage switch types are discussed.

11.1 3:30 - 3:55
Dynamic characteristics of high voltage 4H-SiC JFETs
H. Mitlehnerh, W. Bartsch, K.O. Dohnke,
P. Friedrichs, R. Kaltschmidt, U. Weinert, A.Weis, and D. Stephani
Siemens, Germany

11.2 3:55 – 4:20
Experimental Demonstration of 600V MICCT
T. Iwaana, N. Iwamuro, Y. Harada, and Y. Seki
Fuji, Japan

11.3 4:20 – 4:45
A Monolithically Integrated Device Consisting of a GAT and a MPS Diode with Improved Switching Speed
C. Xu*, K.B. Wei*, J. Sin**,W. Zhe*, and L.G.Zhong*
*Beijing Polytechnic University, P.R. China
**H.K. University of Sci. & Tech., P.R. China

11.4 4:45 – 5:10
New Design Approach for Ultra High Power GCT Thyristor
K. Satoh*, K. Morishita**, M. Yamamoto*, K. Kurachi**, N. Nakanishi*, A. Kawakami*
*Mitsubishi, Japan
**Fukuryou, Japan

5:10 - 5:30 PM

BEST STUDENT PAPER AWARD	**T. Efland**
ISPSD2000	**G. Charitat**
CLOSING REMARKS	**A. Salama**

ISPSD2000

First Announcement
The 12th International Symposium on
Power Semiconductor Devices and ICs
ISPSD2000
Toulouse, France, May 22-25, 2000

The 12th International Symposium on Power Semiconductor Devices & ICs (ISPSD2000) provides a forum for technical discussion in all areas of power semiconductor devices and power IC's and their applications. Areas of interest include, but are not restricted to the following:

- **Materials and Processes**
- **CAD/Simulation**
- **Devices**
- **Monolithic and Hybrid Power Integrations**
- **Packaging**
- **Applications**

General Chair
Dr. Charitat Georges
LAAS-CNRS
Groupe CIP
7, Avenue du Colonel Roche
31077 Toulouse Cedex 4 - France
Phone: +33-5 61 33 64 57 (or 63 59)
FAX: +33-5 61 33 62 08
Email: charitat@laas.fr

For further details about ISPSD'2000, contact the General Chair or visit the website @ http://www.laas.fr/ISPSD2000.