

Projet 8 - ISOL_MOS / Commande isolée pour transistor MOSFET.

Projet : LMP1
Info : [DATA098]
Révision : 10 mars 1999

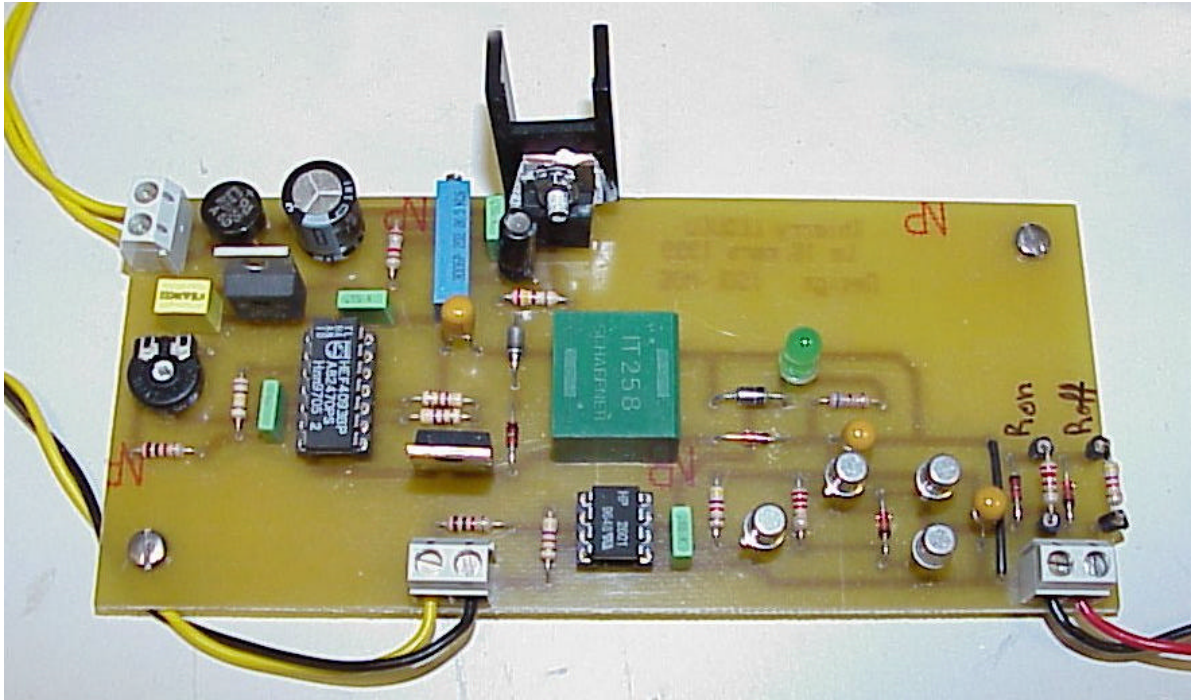


Figure 8.1. Commande isolée pour MOSFET (images-maquettes\cde-mosfet1.jpg).

8.1 Liste des plans

- Calcul du régulateur LM 217.
- Liste des composants.
- Allure des principaux composants.
- Schéma électronique.
- Circuit imprimé.
- Documentations des composants.

8.2 Calcul du régulateur LM 217

La figure 8.2 donne le schéma de montage des régulateurs ajustables LM 117/217/317.

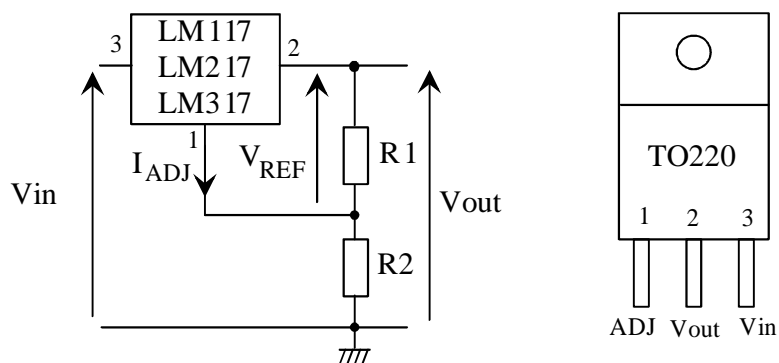


Figure 8.2. Schéma de montage du régulateur (orcad\lmp1\regul1.drw).

La valeur de V_{REF} est constante et vaut $V_{REF} = 1,25 \text{ V}$. Le courant de polarisation du régulateur I_{ADJ} est donné à $I_{ADJ} = 50 \mu\text{A}$. On prendra une chute de tension minimal $V_{IN} - V_{OUT}$ de 3V.

Les courant dans R1 et R2 sont donnés par :

$$I_1 = \frac{V_{REF}}{R1} \text{ et } I_2 = I_1 + I_{ADJ} = \frac{V_{REF}}{R1} + I_{ADJ} = \frac{V_{OUT} - V_{REF}}{R2} \quad (8.1)$$

On en déduit alors l'expression de la tension de sortie V_{OUT} :

$$V_{OUT} = R2 \cdot (I_1 + I_{ADJ}) + V_{REF} = \left(\frac{R2}{R1} + 1 \right) \cdot V_{REF} + R2 \cdot I_{ADJ} \quad (8.2)$$

On peut également exprimer la valeur de la résistance R2 en fonction de V_{OUT} :

$$R2 = \frac{V_{OUT} - V_{REF}}{(I_1 + I_{ADJ})} = \frac{V_{OUT} - V_{REF}}{\left(\frac{V_{REF}}{R1} + I_{ADJ} \right)} \quad (8.3)$$

Dans les notes d'applications, on trouve deux valeurs de résistances R1 :

$$R1 = 120 \Omega \text{ et } R1 = 240 \Omega$$

Le tableau donne la plage de variation de la résistance R2, pour $R1 = 240 \Omega$ en fonction de la tension de sortie désirée V_{OUT} , ainsi que la valeur du condensateur de filtrage.

Tableau 8.1. Calcul des régulateurs LM 117/217/317 (orcad\lmp1\regulateurs.xls).

Vout (en V)	5	9	12	15	18	20	24
R2 (en ohms)	713	1474	2044	2615	3185	3566	4326
Vin mini (en V)	8	12	15	18	21	23	27
V2AC eff (en V)	9	12	15	18	22	24	24
Vc maxi (en V)	12,0	16,3	20,5	24,8	30,4	33,2	33,2
Iout maxi (en A)	1	1	1	1	1	1	1
C mini (en uF)	2483	2342	1814	1480	1062	976	1602

8.3 Liste des composants

Tableau 8.2. Liste de composants (projets-lmp1.xls / ISOL_MOS).

No	Quantité	Référence	Désignation	Empreinte
1	3	C1,C9,C10	100nF	
2	1	C2	1uF	
3	2	C4,C3	4.7uF	
4	1	C5	1nF	
5	1	C6	330uF	
6	1	C7	330nF	
7	1	C8	10uF	
8	5	D1,D2,D3,D6,D7	BAT48	
9	1	D4	5.1V	
10	1	D5	3mm	
11	1	D8	DIODE BRIDGE	REDROND
12	1	D9	24V	
13	1	JP1	SORTIE	
14	1	JP2	ENTREE	
15	1	JP3	ALIM	
16	3	Q1,Q2,Q4	2N2222	
17	1	Q3	2N2907	
18	1	Q5	IRF520N	
19	1	R1	2.2K	
20	1	R2	4.7K	
21	1	R3	750	
22	1	R4	100K	
23	2	R5,R9	1K	
24	3	R6,R8,R10	470	
25	1	R7	10K	
26	1	R11	R_ON	
27	1	R12	R_OFF	
28	1	R13	2K	
29	1	R14	1.8K	
30	1	R15	240	
31	1	T1	IT258	
32	1	U1	CD4093	
33	1	U2	LM217	
34	1	U3	7815	
35	1	U4	HCPL2601	

8.4 Allure des principaux composants

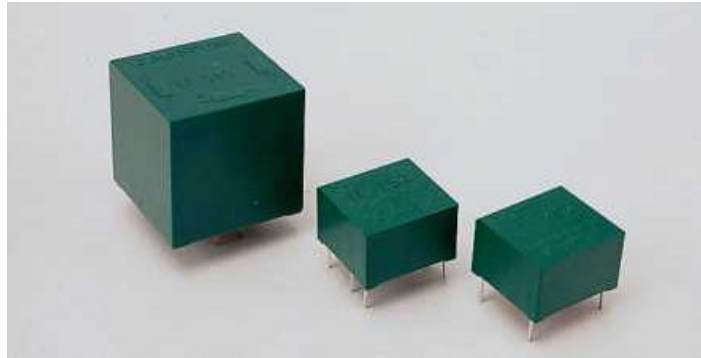


Figure 8.3. Transformateurs d'impulsions (images-composants\ti1.jpg).

Type de boîtier:

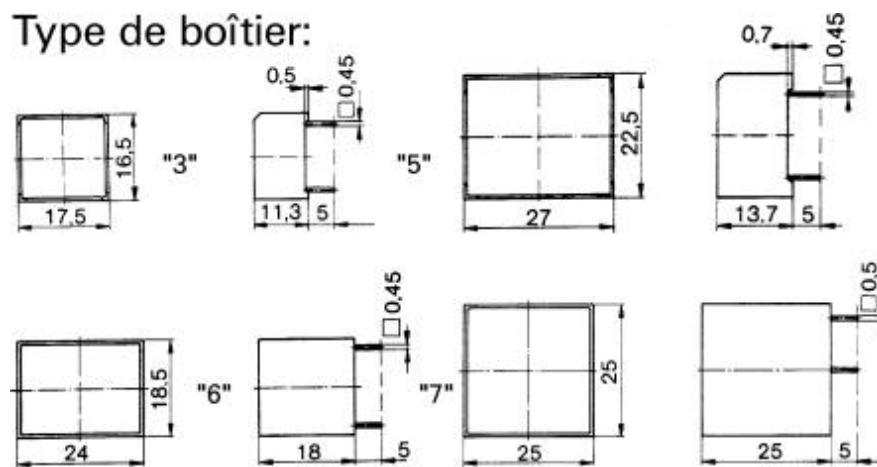


Figure 8.4. Transformateurs d'impulsions (images-composants\ti2.gif).

Connexions

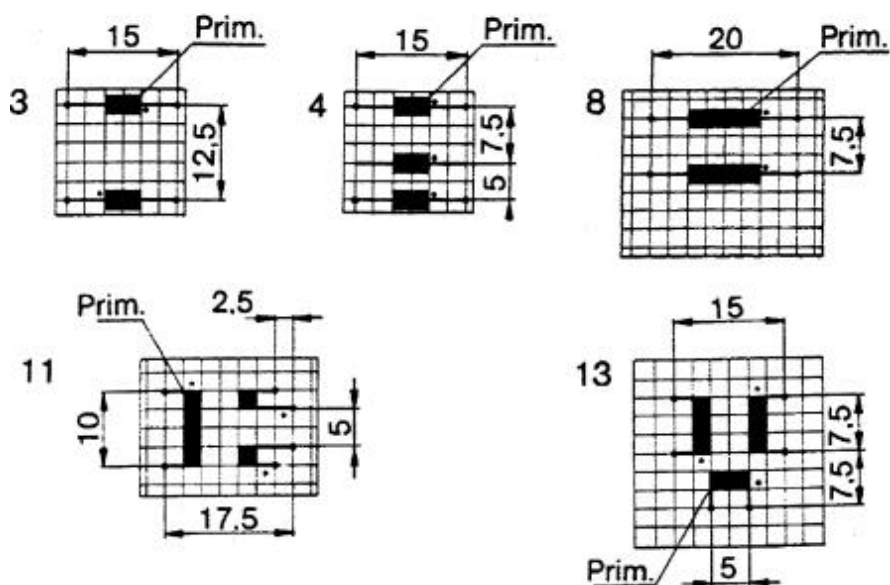


Figure 8.5. Transformateurs d'impulsions (images-composants\ti3.gif).

8.5 Circuit imprimé de la version 2 du 16 mars 1999

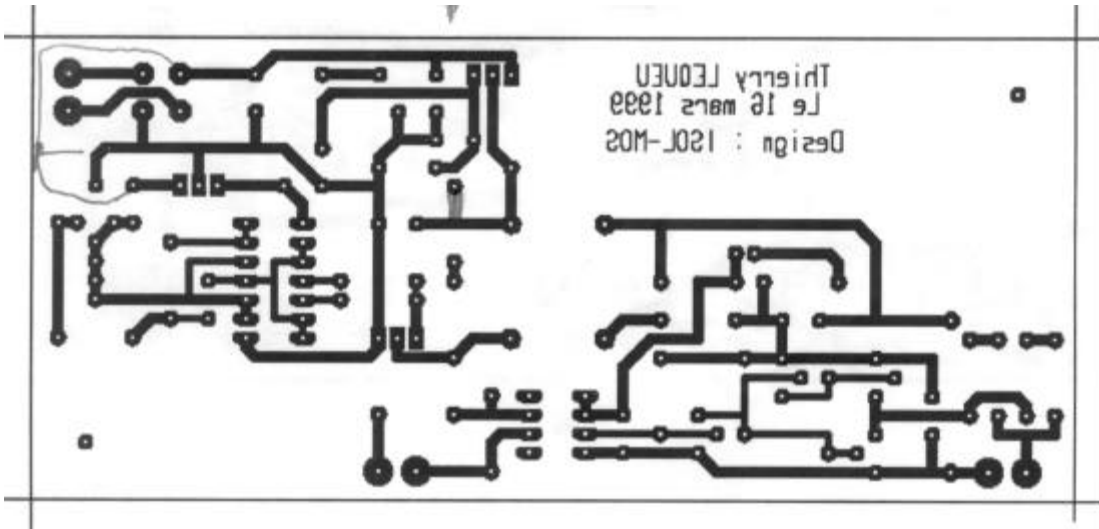


Fig. 8.6. Circuit imprimé coté cuivre (images-maquettes\isol_mos11.jpg).

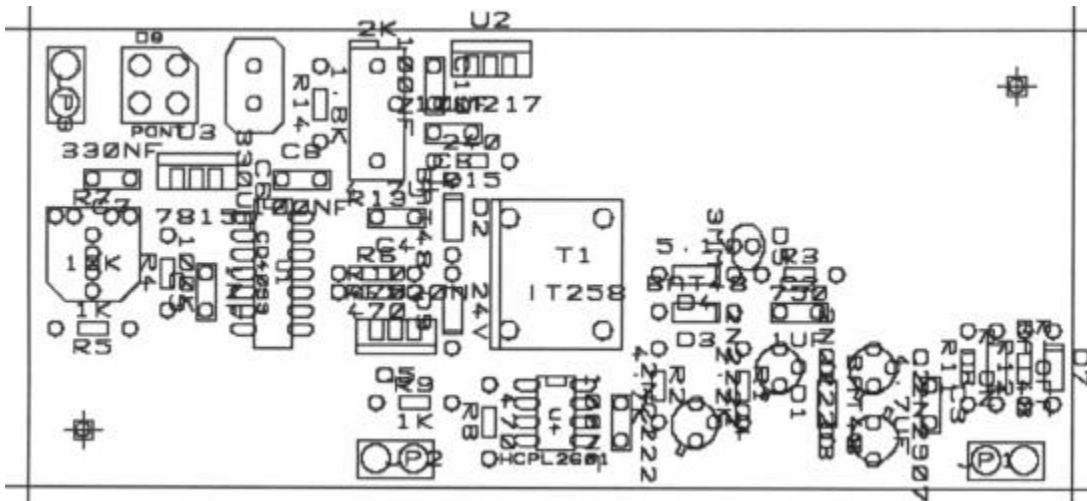


Fig. 8.7. Circuit imprimé coté composants (images- maquettes\isol_mos21.jpg).

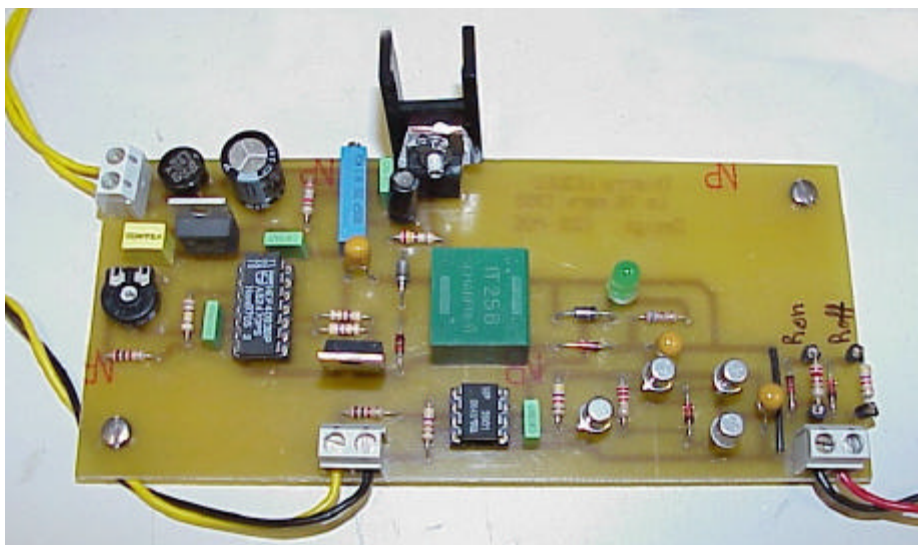
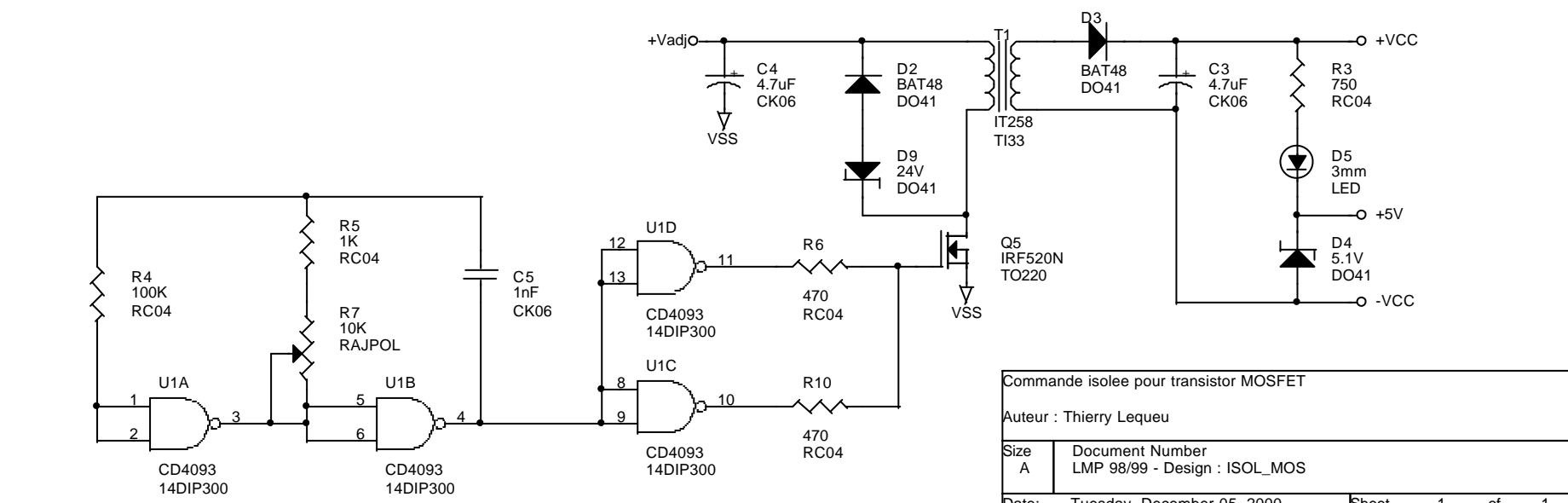
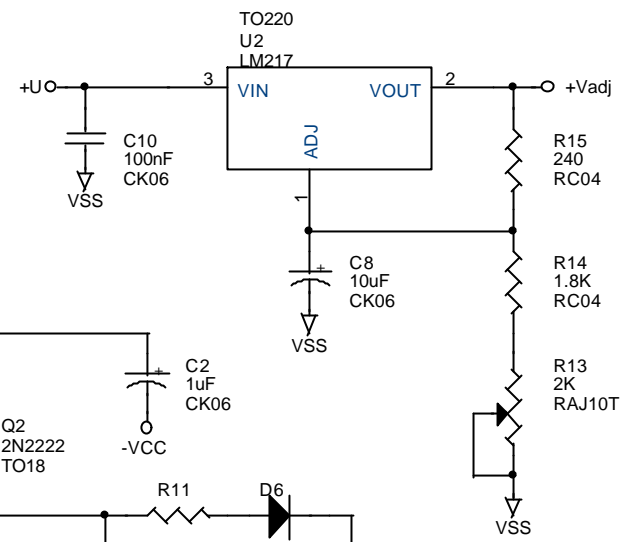
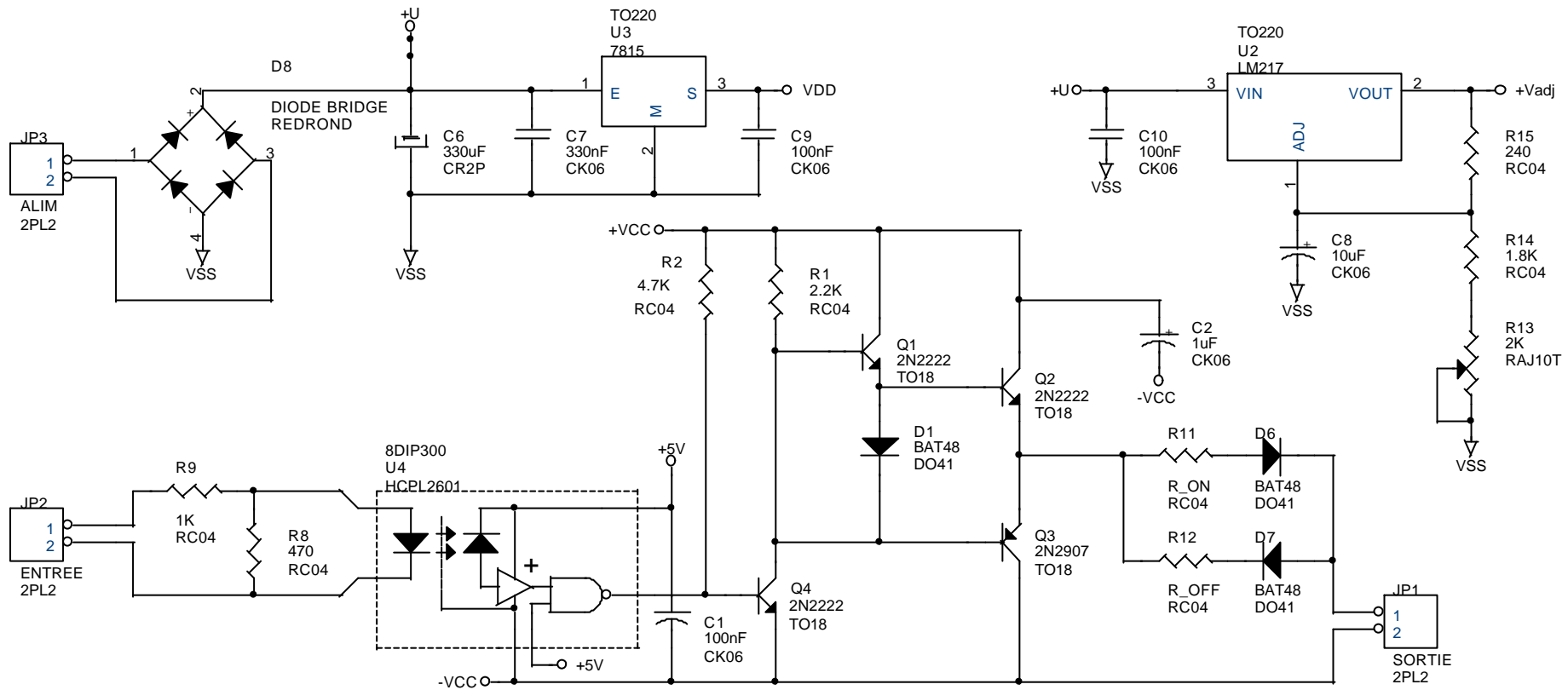


Fig. 8.8. Commande isolée pour MOSFET (images-maquettes\cde-mosfet1.jpg).

Réf.	Désignation	Qu.	Fournisseur	Date	Page	Code Cde	U.d.V.	Prix U.H.T.	Prix T.H.T.
C1,C6	100 nF100V Polyester	1	Radiospares	décembre-00		166-5973	10	16,09 F	1,61 F
C2	1uF 25V tantale	1	Radiospares	décembre-00		180-1668	10	10,00 F	1,00 F
C3,C4	4.7uF 25V tantale	2	Radiospares	décembre-00		180-1696	10	3,50 F	0,70 F
C5	1nF 100V polypropylène	1	Radiospares	décembre-00		115-691	5	9,92 F	1,98 F
D1,D2,D3,D8,D9	BAT48	5	Radiospares	décembre-00		251-3053	10	22,20 F	11,10 F
D4	zener 5.1V	1	Radiospares	décembre-00		283-019	3	3,90 F	1,30 F
D5	LED 3mm verte	1	Radiospares	décembre-00		113-4463	5	6,15 F	1,23 F
D6	zener 24V	1	Radiospares	décembre-00		112-7825	3	3,90 F	1,30 F
D7	1N4007	1	Radiospares	décembre-00		261-980	10	6,50 F	0,65 F
JP1 - SORTIE	Connecteur, bloc de jonction, circuit imprimé, pas 5mm, 2 points, Camdem,	1	Radiospares	décembre-00		131-8920	10	16,65 F	1,67 F
JP2 - ENTRÉE	Connecteur, bloc de jonction, circuit imprimé, pas 5mm, 2 points, Camdem,	1	Radiospares	décembre-00		131-8920	10	16,65 F	1,67 F
JP3 - ALIM	Connecteur, bloc de jonction, circuit imprimé, pas 5mm, 2 points, Camdem,	1	Radiospares	décembre-00		131-8920	10	16,65 F	1,67 F
OPTO1	HCPL2601	1	Radiospares	décembre-00		303-129	1	27,40 F	27,40 F
Q1,Q2,Q4	2N2222	3	Radiospares	décembre-00		295-028	1	3,53 F	10,59 F
Q3	2N2907	1	Radiospares	décembre-00		349-9043	5	24,00 F	4,80 F
Q5	IRF520N	1	Radiospares	décembre-00		295-371	1	9,79 F	9,79 F
R1	2.2K	1	Radioson				1	0,15 F	0,15 F
R2	4.7K	1	Radioson				1	0,15 F	0,15 F
R3	750	1	Radioson				1	0,15 F	0,15 F
R4	100K	1	Radioson				1	0,15 F	0,15 F
R5,R9	1K	2	Radioson				1	0,15 F	0,30 F
R6,R8,R10	470	3	Radioson				1	0,15 F	0,45 F
R7	10K	1	Radioson				1	0,15 F	0,15 F
R11	R_ON	1	Radioson				1	0,15 F	0,15 F
R12	R_OFF	1	Radioson				1	0,15 F	0,15 F
T1	IT258	1	Radiospare	décembre-00		173-6423	1	53,20 F	53,20 F
U1	CD4093	1	Radiospare	décembre-00		345-5712	1	1,97 F	1,97 F
Divers	Circuit imprimé S.F. 150x80 mm	120	IUT GEII				1	0,15 F	18,00 F

TOTAL H.T. :	153,42 F
dont TVA : 19,60%	30,07 F
TOTAL T.T.C. :	183,49 F



Commande isolee pour transistor MOSFET

Auteur : Thierry Lequeu

Size A	Document Number LMP 98/99 - Design : ISOL_MOS	Rev 2
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Date: Tuesday, December 05, 2000 Sheet 1 of 1

High CMR, High Speed TTL Compatible Optocouplers

Technical Data

6N137	
HCNW137	HCPL-0631
HCNW2601	HCPL-0661
HCNW2611	HCPL-2601
HCPL-0600	HCPL-2611
HCPL-0601	HCPL-2630
HCPL-0611	HCPL-2631
HCPL-0630	HCPL-4661

Features

- **5 kV/μs Minimum Common Mode Rejection (CMR) at $V_{CM} = 50$ V for HCPL-X601/X631, HCNW2601 and 10 kV/μs Minimum CMR at $V_{CM} = 1000$ V for HCPL-X611/X661, HCNW2611**
- **High Speed: 10 MBd Typical**
- **LSTTL/TTL Compatible**
- **Low Input Current Capability: 5 mA**
- **Guaranteed ac and dc Performance over Temperature: -40°C to +85°C**
- **Available in 8-Pin DIP, SOIC-8, Widebody Packages**
- **Stroable Output (Single Channel Products Only)**
- **Safety Approval**
UL Recognized - 2500 V rms for 1 minute and 5000 V rms* for 1 minute per UL1577
CSA Approved
VDE 0884 Approved with $V_{IORM} = 630$ V peak for HCPL-2611 Option 060 and $V_{IORM} = 1414$ V peak for HCNW137/26X1
BSI Certified (HCNW137/26X1 Only)
- **MIL-STD-1772 Version Available (HCPL-56XX/66XX)**

Applications

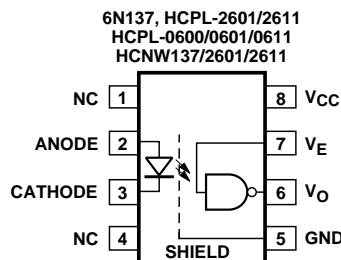
- **Isolated Line Receiver**
- **Computer-Peripheral Interfaces**
- **Microprocessor System Interfaces**
- **Digital Isolation for A/D, D/A Conversion**
- **Switching Power Supply**
- **Instrument Input/Output Isolation**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**

- **Power Transistor Isolation in Motor Drives**
- **Isolation of High Speed Logic Systems**

Description

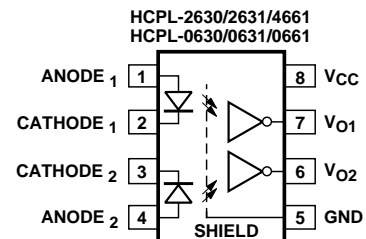
The 6N137, HCPL-26XX/06XX/4661, HCNW137/26X1 are optically coupled gates that combine a GaAsP light emitting diode and an integrated high gain photo detector. An enable input allows the detector to be strobed. The output of the detector IC is

Functional Diagram



TRUTH TABLE
(POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H
ON	NC	L
OFF	NC	H



TRUTH TABLE
(POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

*5000 V rms/1 Minute rating is for HCNW137/26X1 and Option 020 (6N137, HCPL-2601/11/30/31, HCPL-4661) products only.

A 0.1 μF bypass capacitor must be connected between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

9.2A, 100V, 0.270 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA09594.

Ordering Information

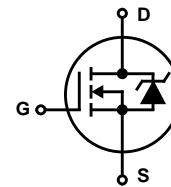
PART NUMBER	PACKAGE	BRAND
IRF520	TO-220AB	IRF520

NOTE: When ordering, use the entire part number.

Features

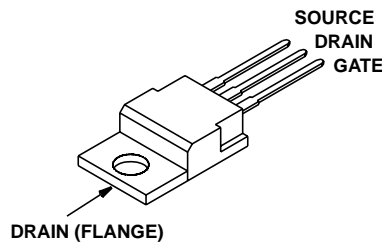
- 9.2A, 100V
- $r_{DS(ON)} = 0.270\Omega$
- SOA is Power Dissipation Limited
- Single Pulse Avalanche Energy Rated
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC TO-220AB



1.2V TO 37V VOLTAGE REGULATOR

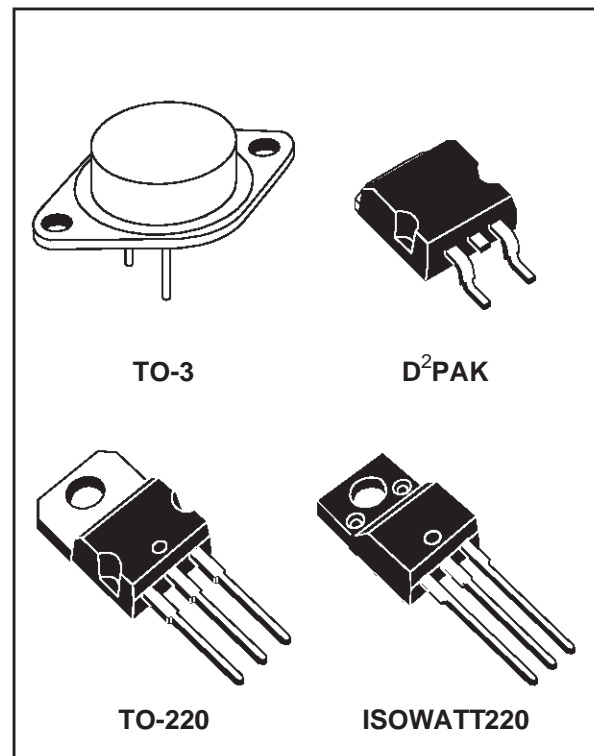
- OUTPUT VOLTAGE RANGE : 1.2 TO 37V
- OUTPUT CURRENT IN EXCESS OF 1.5A
- 0.1% LINE AND LOAD REGULATION
- FLOATING OPERATION FOR HIGH VOLTAGES
- COMPLETE SERIES OF PROTECTIONS : CURRENT LIMITING, THERMAL SHUTDOWN AND SOA CONTROL

DESCRIPTION

The LM117/LM217/LM317 are monolithic integrated circuit in TO-220, ISOWATT220, TO-3 and D²PAK packages intended for use as positive adjustable voltage regulators.

They are designed to supply more than 1.5A of load current with an output voltage adjustable over a 1.2 to 37V range.

The nominal output voltage is selected by means of only a resistive divider, making the device exceptionally easy to use and eliminating the stocking of many fixed regulators.



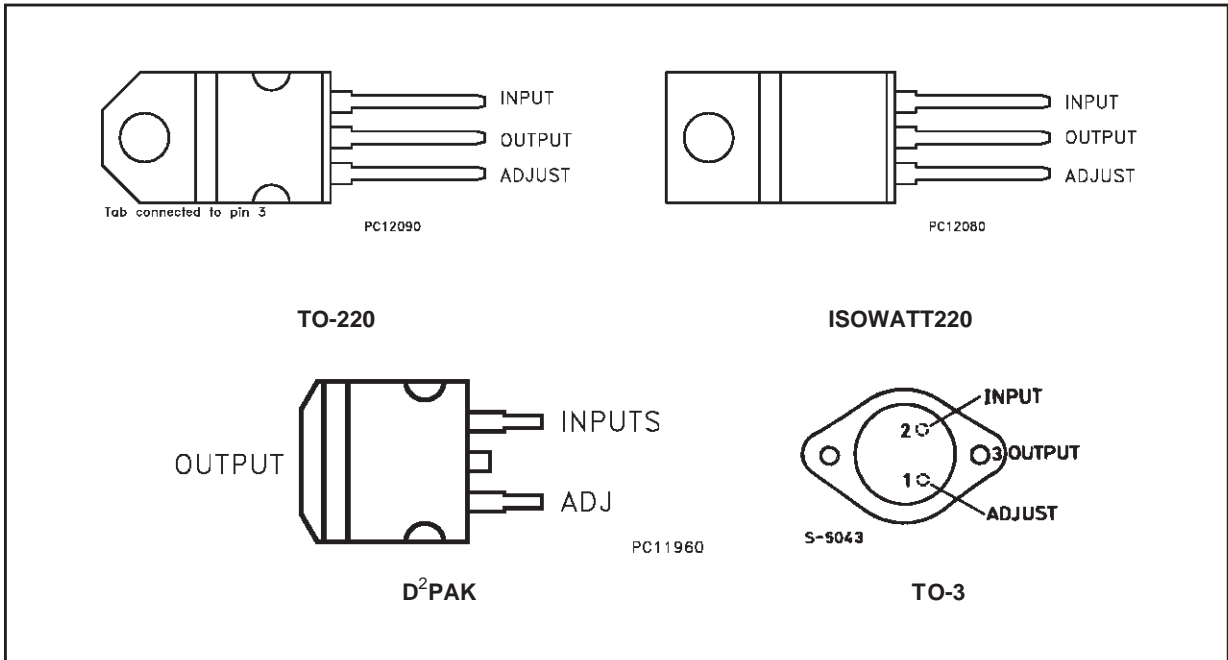
ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{i-o}	Input-output Differential Voltage	40	V
I_o	Output Current	Internally Limited	
T_{op}	Operating Junction Temperature for: LM117 LM217 LM317	-55 to 150 -25 to 150 0 to 125	°C °C °C
P_{tot}	Power Dissipation	Internally Limited	
T_{stg}	Storage Temperature	- 65 to 150	°C

THERMAL DATA

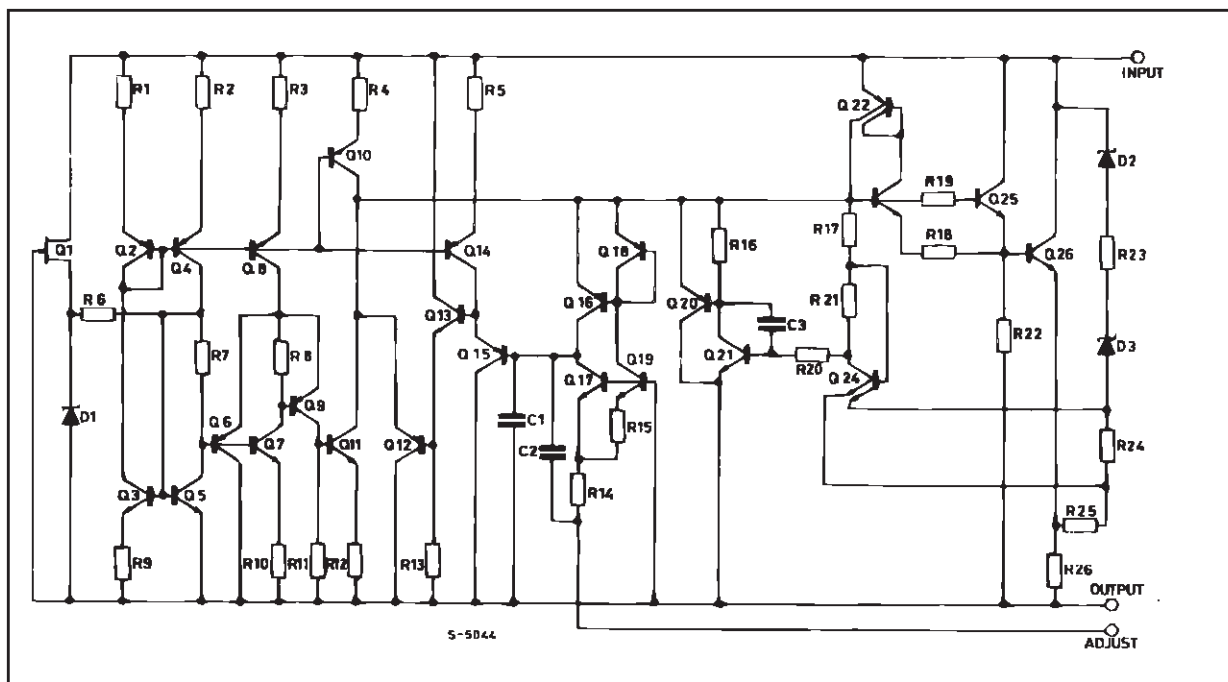
Symbol	Parameter	TO-3	TO-220	ISOWATT220	D ² PAK	Unit
$R_{thj-case}$	Thermal Resistance Junction-case	4	3	4	3	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient	35	50	60	62.5	°C/W

CONNECTION DIAGRAM AND ORDERING NUMBERS (top view)



Type	TO-3	TO-220	ISOWATT220	D ² PAK
LM117	LM117K			
LM217	LM217K	LM217T		LM217D2T
LM317	LM317K	LM317T	LM317P	LM317D2T

SCHEMATIC DIAGRAM

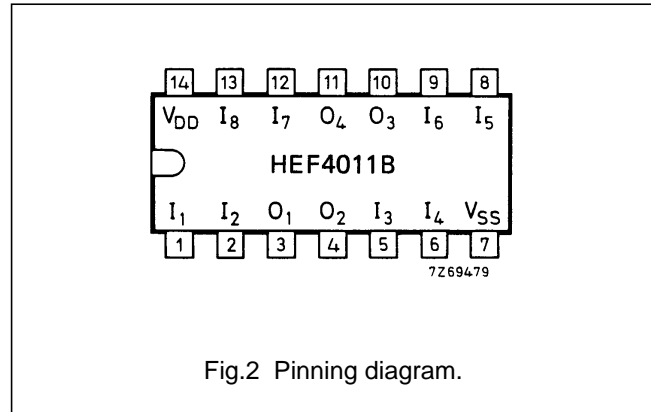
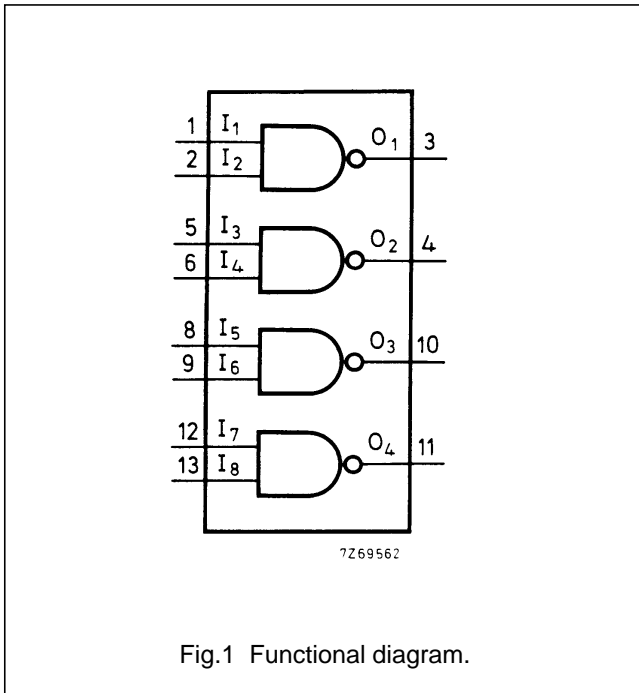


Quadruple 2-input NAND gate

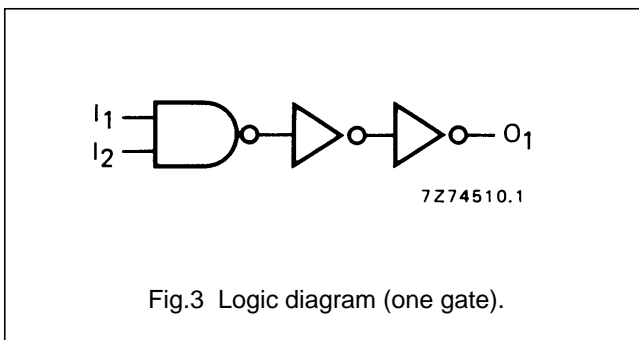
HEF4011B
gates

DESCRIPTION

The HEF4011B provides the positive quadruple 2-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.



- HEF4011BP(N): 14-lead DIL; plastic (SOT27-1)
 - HEF4011BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
 - HEF4011BT(D): 14-lead SO; plastic (SOT108-1)
- (): Package Designator North America



FAMILY DATA, I_{DD} LIMITS category GATES

See Family Specifications