What is a SIG?

A Special Interest Group is a collection of people who meet to pursue and share knowledge and information on a specific topic.

Who makes up a SIG?

A SIG is composed of individuals that may represent a wide range of backgrounds and interests.

The effectiveness of the SIG depends on the shared affiliation with others in an area of common interest.

For Example: Circuit Designers, Process Engineers, Device Engineers, Reliability Engineers, Quality Assurance Engineers, ...

What does a SIG do?

The purpose of SIGs is to provide a means for members of several companies to engage in a collaborative pursuit of knowledge and understanding of topics of mutual concern and benefit.

Why SIGs?

There is perceived need to develop intercompany, collaborative efforts in the reliability arena. This need is validated by the on-going support for various SIG-like activities:

- Fine Line Task Force
- Building In Reliability Task Force
- JEDEC 14.2 WLR Working Groups

Why SIGs? (cont.)

We believe that broader participation can be achieved through the formation of SIGs that would coalesce around a commonly held problem area and work to develop potential solutions or solution methodologies

What are the benefits?

No one company can know all of the solutions to the problems that lie ahead in the field of reliability. SIGs may provide a resource-effective means of closing the knowledge gap by capitalizing on the synergy that can occur in small working groups for task forces.

What are the benefits? (cont.)

SIGs may provide a viable outlet or opportunity for non-JEDEC or non-CCI member companies to participate in intercompany activities.

INTEGRATED RELIABILITY WORKSHOP SPECIAL INTEREST GROUPS (SIG)

COMMON ELEMENTS OF A SUCCESSFUL SIG

- At least one "Champion"
- Each participant is dedicated, with a specific & crucial role to play
- Objectives are clear and specific
- Interaction is frequent, often each week
- Specific "Outputs" are clearly stated
- Membership tends to be small (usually under 5)
- Direct or indirect funding exist
- At least some tie-in with company work

INTEGRATED RELIABILITY WORKSHOP SPECIAL INTEREST GROUPS (SIG)

OFFICIAL "SIG" GROUPS:

- "CHARM" Ion Implant monitor
  - Chair..Wes Lukaszek (Stanford)
  - Mentor.......................................Cleston Messick (NSC)
- HAST Users
  - Chair...Brian Walker (Digital)
  - Mentor..Kris Mohan (NSC)
- Test Chips for Package Reliability
  - Chair...James Sweet (Sandia)
  - Mentor...Kris Mohan (NSC)
- Thin Oxides
  - Chair..Cleston Messick (NSC)
  - Mentor...John Suehle (NIST)
- SWEAT / Isothermal / Conventional E.M.
  - Chair...Marty Johnson (NSC)
  - Co-Chair.......................................Raif Hijab (AMD)
  - Mentor..Paul Marcoux (HP)
- Wafer / Die Level Burn-In
  - Chair...David Kirchner (Sharp Mic.)
  - Mentor..Kris Mohan (NSC)
- WLR Implementation
  - Chair...Gordon Claudius (Rockwell)
  - Mentor..Pat Kennedy

CHARM SPECIAL INTEREST GROUP (CHARM SIG)

Definition:
The CHARM Special Interest Group (CHARM SIG) has been formed to further the development and application of EEPROM-transistor-based surface charging monitor wafers in IC process development, manufacturing, and reliability assurance.

Mission:
- Make available a complete, proven CHARM tool, comprised of CHARM 2.1 wafers, test, and data analysis software.
- Provide assistance in the application of the CHARM tools.
- Use the CHARM tools to develop improved understanding of wafer charging mechanisms in ion implantation and plasma-based processes.
- Develop wafer charging models and oxide damage prediction methods using the CHARM tools.

Roadmap:
- Process and make available sample quantity of 150 mm CHARM 2.1 wafers.
- Provide proven CHARM 2.1 test and data interpretation support.
- Conduct a thorough CHARM 2.1 evaluation on a high-volume IC manufacturing line.
- Summarize key observations related to CHARM applications, and disseminate them to members of CHARM SIG.

TIME-FRAME:
The above should be completed by the end of the year. Another roadmap will be developed next year for follow-on activities.

EXPECTED ACTIVITIES:
- Run CHARM 2.1 experiments in a variety of ion and plasma-based process equipment.
- Analysis data and develop charging and oxide damage models.
- Communicate on a regular basis (at least once a month).
- Publish results.

RESOURCES/FUNDING:
All resources come from SIG members. (CHARM tools will be commercially available.) Contributors to the SIG will determine extent of distribution of details.

MEMBERSHIP:
Membership is open to anyone able to actively contribute to the SIG. (Financial support of basic research in this field at Stanford University will qualify as active participation).

ACTIVE MEMBER ROSTER:
Michael Current, Applied Materials
Larry Larson, SEMATECH
Wes Lukaszek, Stanford University
Cleston Messick, National Semiconductor
Joseph Reedholm, Reedholm Instruments
Jay Shideler, National Semiconductor

CHARTER FOR HAST USERS SPECIAL INTEREST GROUP

DEFINITION OF THE SIG:
The HAST Users SIG provides a forum for both experienced and novice HAST users to share and discuss HAST test procedures and data. The forum will promote the use of HAST as a means of advancing the reliability of plastic package.

MISSION:
The HAST SIG exists to promote the use of HAST as a reliability assessment tool for non-hermetic semiconductor devices. Promotion of HAST will include encouragement of standard test procedures and parameters. The HAST SIG will also support information exchange on solving HAST test equipment related problems, new semiconductor/IC packaging failure mechanisms induced by HAST and HAST based failure mechanism models and acceleration factors.

ROADMAP:

1. Gather and maintain a list of individuals responsible or active with HAST testing that are interesting in participating in the HAST users SIG.
2. Sense the varying needs of the SIG participants and match individuals with common interests together, to work on HAST specific issues (i.e. HAST development, HAST acceleration factor calculation, modeling).
3. Share test experience and data to enhance future HAST development and plastic packaging reliability. Encourage the presentation of findings in recognized conferences.

TIME FRAME:

SHORT TERM (6-12 months):

- Develop HAST database with contact list of names and phone numbers as well as a compilation of responses to HAST questionnaire.
- Group the interest categories of HAST SIG participants.
- List of failure mechanisms accelerated by HAST for packaging, die/wafer coat, passivation etc. Discuss HAST failure mechanism modeling.
- Discuss HAST test procedure standards and consensus on endorsing existing standards.
- Provide regular forum for discussion of HAST equipment limitations.

LONG TERM (> 12 months):

- Endorse test procedure
- Develop minimum HAST equipment specifications/capabilities
- Develop HAST based reliability evaluation tools such as:
  - HAST based failure mechanism models
  - HAST based acceleration factors
- Share HAST generated test data and encourage joint projects and publications.

EXPECTED ACTIVITIES:

1. Share experiences with HAST testing procedures.
2. Discuss failure mechanisms generated from HAST - develop models.
3. Meet regular1y at IRW and IRPS
4. Hold regular (monthly, bi-monthly) conference calls
5. Present data at conferences or journals

RESOURCES/FUNDING:
All resources are derived from the SIG members. The SIG is not a legally organized group and will not have resources of its own. Contributors to the SIG will determine the extent of distribution of the details. (i.e. It would be possible for a member to provide samples without disclosing outside of the SIG the processing details.)

MEMBERSHIP:

Advisor: Jay Shideler, NSC
Mentor: Kris Mohan, NSC

Membership is open to anyone able to actively contribute to the SIG.

Name	Company	Phone/FAX	EMAIL
Ken Bowers	Micro Instruments	619-746-2010/0433	
Charles Hong	Intel Corporation	503-642-6744/6652	(chong@aloha6.intel.com)
Jack Honore	AT&T Bell Labs	609-639-3062/2851	
Steve Kidd	Analog Devices	408-562-7592/2654	
Kris Mohan	Nat'l Semiconductor	408-721-3075/2323	
Andy Shia	Cirrus Logic	408-945-8300/263-5682	(andys@cirrus.com)
Glen Shirley	Intel Corporation	503-642-6050/6652	(gshirley@aloha6.intel.com)
Jim Sweet	Sandia Nat. Labs	505-845-8242/844-2991	
Kamilia Tenenbaum	Ericsson Telecom	4608-7199596/46-087198439	
Morris Tsou	VLSI Technology	408-434-7973/7935	
Brian Walker	Digital Equipment	508-568-6940/4681	(walker@bigq.enet.dec.com)

TEST CHIPS FOR PACKAGE RELIABILITY SPECIAL INTEREST GROUP -Draft Charter 10/8/93

DEFINITION OF THE SIG

The Test Chips for Package Reliability SIG provides a mechanism for Members to pool information and share knowledge in the area of test chips and associated methodology for reliability and lifetime evaluation of packaged or assembled integrated circuits.

MISSION:

The principal mission of this SIG is to speed the development of special purpose assembly test ICs (Assembly Test Chips or ATCs) and test methodology for use in evaluating the reliability or packaged ICs. In addition, the SIG will work to make information and ATCs publicly available to users.

ROADMAP:

1. Develop a list and description of packaged part failure modes of interest to SIG members.
2. Develop a list and description of test circuits or structures which could potentially be used to study the failure modes developed in item # 1. Also develop a list of commercial ICs and ATCs which are useful for evaluation of package reliability.
3. Using the information developed in 1 & 2, determine the requirements for potential new activity in package reliability test vehicle development.
4. Determine potential mechanisms for fabricating test chips and making them available to the public.

TIME FRAME:

1. Complete preliminary work on item 1 above by 3/94 and distribute results to SIG members by newsletter.
2. By IRW 94, complete items 1-3 below and present a summary at that IRW.

EXPECTED ACTIVITIES:

1. Conduct a survey of SIG members and others in the packaging/reliability community to define needs or requirements for ATCs and test methodology.
2. Determine the suitability of existing ATCs and commercial ICs for meeting the requirements determined in 1.
3. Write a long newsletter and/or journal paper summarizing the findings of # 1 and # 2 above and describing recent ATC work.

RESOURCES/FUNDING:

All funding for work on this SIG will come from the individual member companies. Similarly, the resources will be those of the member companies.

MEMBERSHIP REQUIREMENTS:

Membership is open to people who are interested in playing an active roll in the SIG. Members should be willing to work on the SIG activities and share their experiences with other members.

ACTIVE MEMBER ROSTER:

Kris Mohan, National Semiconductor Corp.
Jay Shideler, National Semiconductor Corp.
Barbara Vasquez, Motorola Corp.
James Sweet, Sandia National Laboratories
Charles Hong, Intel Corp.
Tim Turner, Turner Engineering Technology

CHARTER FOR THIN OXIDE RELIABILITY MEASUREMENT

Special Interest Group

DEFINITION OF THE SIG:
The thin oxide SIG provides a platform for university, government, and industry individuals to pool resources to make significant advances in the reliability testing of grown silicon dioxide films thinner than 35 nm.

MISSION:
Using data obtained from testing differently processed oxides at a variety of fields and temperatures, develop appropriate models, testing methods, and data analysis procedures. Publish the results in accepted journals and at conferences.

ROADMAP:

1. Distribute similarly processed wafers having well designed MOS capacitors to different facilities for testing over a range electric fields and temperatures.
2. Circulate data.
3. Determine best data analysis techniques.
4. Fit data to existing models & determine variances.
5. Develop new models to explain data.
6. Distribute status and results at IRW and IRPS..

TIME FRAME:
By IRW in 1996, work on 10 to 35 nm thick oxides should be completed. Further activities may develop as needs arise.

EXPECTED ACTIVITIES:

1. Test wafers and/or packages
2. Analyze data and compare to present models
3. Develop model(s)
4. Meet regularly (at IRW and IRPS —other times as possible and/or needed.)
5. Hold monthly teleconference calls (more often if needed)
6. Present results at conferences or in journals.

RESOURCES/FUNDING:
All resources are derived from the SIG members. The SIG is not a legally organized group and will have no resources of its own. Contributors to the SIG will determine the extent of distribution of the details. (i.e. It would be possible for a member to provide samples without disclosing outside of the SIG the processing details.)

MEMBERSHIP:
Membership is open to anyone able to actively contribute to the SIG. However, this is a small working group and those desiring to work with a large group are invited to participate in the JEDEC 14.2 subcommittees.

ACTIVE MEMBER ROSTER:

1. John Suehle, NIST
2. Cleston Messick, National Semiconductor
3. Bill Miller, Sandia
4. Ken Boyko, AT&T

ELECTROMIGRATION SPECIAL INTEREST GROUP

DEFINITION OF THE SIG
The EM SIG provides a base for all interested parties to discuss and critique experiences and data relating conventional EM testing to ‘fast’ EM tests. The ultimate aim of such discussions is to find a ‘link’ between the conventional and the ‘fast’.

MISSION:
The EM SIG will strive for a method(s) to show the ‘link’ between conventional and ‘fast’ EM testing. Understanding the current data from participants, how it correlates and what other possible strategies exist to arrive at meaningful correlation between conventional and ‘fast’ tests. The SIG is interested in all points of view on the correlation issue.

Some ideas being considered:

1. SWEAT vs some slower test;
2. Round Robin testing — more range in temperature and current;
3. Structures — which ones are applicable?;
4. Conventional EM correlatable to product die?

ROADMAP:

1. Gather and maintain a list of individuals interested and active in EM testing of all types that are interested in participating in this SIG.
2. Match the needs of the participants with the subset tasks envisioned by the SIG.
3. Encourage participation of the EM SIG members on their experiences with methodology and data.

TIMEFRAME: SHORT TERM (6-12 mos.):

- Develop a list of areas of interest to the SIC.
- Determine the best fit of the participants to the areas of interest.
- Assign SIG members groups for work in their area of interest.
- Provide a regular forum to discuss the details of their inquiries, i.e. teleconference calls, local meetings, etc.

ELECTROMIGRATION SPECIAL INTEREST GROUP (cont)

LONG TERM (> 12 mos.):

- Evaluate the data.
- Test conclusions from data in further experiments.
- Share information with the whole WLR community.

EXPECTED ACTIVITIES

1. Share testing experiences.
2. Discuss possibility of non-conventional failure mechanisms.
3. Meet at IRW and IRPS.
4. Hold regular teleconference calls.
5. Present data at conferences or to journals.

RESOURCES/FUNDING:
All resources are derived from the SIG members. The SIG is not a 1egally organized group and, as such, does not have resources of its own. Contributors to the SIG wlll determine the extent of distribution of the details.

MEMBERSHIP:
Membership is open to anyone able to actively contribute to the SIG.

MEMBERSHIP ROSTER:

Ken Bowers	Micro Instruments	619-746-2010/0433
Yeong Chen	Rockwe1l	714-833-4060/6680
Ting Chien	Sharp Microelectronics	206-834-8772/8611
Gordon Claudius	Rockwell	714-833-4060/6680
Mike Dreyer	Motorola	602-898-5001/897-4511
David Erhart	Motorola	602-821-4256/4167
Paul Flynn	Intel	
David Hannaman	Silicon Systems Inc.	714-573-6371/6910
H.H.Hoang	SGS Thomson	214-466-7182/6008
Tom Hoyle	EXAR Corporation	408-434-6400/6643
Mohamed Khidr	National Semiconductor	408-721-6474/7266
Arthur Kuo	LSI Logic	408-433-6360/1486
Paul Marcoux	Hewlett-Packard	415-857-5415/852-8508
Y.F.Lin	Hewlett-Packard	
Cleston Messick	National Semiconductor	801-562 7546/7500
Nancy McCurry	AT&T Bell Labs	215-439-7339/6443
Bryan Root	Sienna Technologies	612-688-6106/2417
Harry Schafft	NIST	301-975-2234/948-4081
Terry Spooner	Digital Equipment Corp.	508-568-4667/4681
Kamila Tenenbaum	Ericsson Telecom	4608-7199596/7069
Morris Tsou	VLSI Technology	408-434-7973/7935
Barbara Vasquez	Motorola	602-897-4696/4511
Wei-Wei Yeung	Watkins-Johnson	415-493-4141/1027
John Yue	AMD	408-749-3189/5584
Co-Leaders:		
Marty Johnson	National Semiconductor	408-721-3077/732-6017
Raif Hijab	AMD	408-749-2250/5585

CHARTER FOR WAFER-LEVEL/DIE LEVEL BURN-IN SPECIAL INTEREST GROUP

DEFINITION:

The Wafer-Level/Die-Level Burn-in SIG provides a forum to explore, investigate, and relate methods and mechanisms for performing the burn-in function at the wafer- or die-level of integrated circuit manufacture and to further the concept of Known Good Die in general.

OBJECTIVE:

The Wafer-Level/Die-Level Burn-in SIG exists to further the knowledge base regarding both the mechanics of wafer- or die-level burn-in and to promote the concept of Known Good Die (KGD).

METHODS - Phase 1 (12 months)

1. Gather and maintain a list of individuals involved in or interested in W-L/D-L burn-in or KGD.
2. Gather information about systems of performing this burn-in and disseminate it through the SIG membership.
3. Gather information about KGD programs and disseminate it through the SIG membership.

METHODS - Phase II (> 12 months)

Investigate and explore the reliability relationships between KGD programs and the traditional packaged reliability testing.

MEMBERSHIP:

- Membership is open to anyone able to actively contribute or participate in its function. Members may include those interested in supplying or using multichip modules or those involved in a Known Good Die program.
- Equipment manufacturers are welcome with the *proviso* that they actively share what information they can about their own systems.
- The SIG will not be used as a sales forum. The membership may be polled for information requests, but may not be used as a mass-mailing list.

Membership Roster: (Not available at this time.)

CHARTER FOR THE WAFER LEVEL RELIABILITY IMPLEMENTATION SPECIAL INTEREST GROUP

DEFINITION:

For the purpose of this SIG, WLR is defined as relatively fast tests which can be applied to a significant sample of a production line - much like parametric test. WLR is not a new concept. However, the specifics remain somewhat nebulous, and the practical implementation of programs in the production world is not a trivial task. Areas of discussion should include any WLR test capable of predicting a potential product reliability weakness. These would include, but not be limited to, dielectric integrity and stability, interconnect reliability, and hot carrier effects.

FORMAT:

It is expected that participants be ready to discuss implementation procedures, specific text procedures, WLR success stories, analysis and use of WLR data, and correlation ox WLR date to long term, classical reliability testing. A presentation on the structure of a successful company WLR program should occur at each meeting.

TIME TABLE:

There is no specific time frame or milestones for this SIG. It should operate as long as its existence is useful.

SIG GOAL:

To provide a forum for the open exchange of ideas and methodologies for implementing an effective Wafer Level Reliability (WLR) program.

WHAT IS EXPECTED:

SEMICONDUCTOR MANUFACTURERS:

A free and open exchange of ideas and techniques is required. It is important to share what works and what fails is WLR analysis. This is not intended to infringe on company confidential information.

VENDORS OF EQUIPMENT AND SERVICES:

Your knowledge is invaluable please share it openly. This is not a forum for sales. Please respect this precept.

CUSTOMERS OF SEMICONDUCTOR PRODUCTS:

You know what your requirements are. Your function is to work with the manufacturers to inform them of these requirements and to work towards the realization of their fulfillment.

MEMBERSHIP ROSTER
WLR IMPLEMENTATION SIG OF THE IRW

MEMBER	COMPANY	PHONE
BECK, CLARK	RAYTHEON	415-966-7685
CHAMNESS, DAVID	HEWLETT-PACKARD	303-229-6910
CLAUDIUS, GORDON*	ROCKWELL INTERNAT'L	714-833-4060
DANAHER, HUGH	REEDHOLM INSTRU.	510-490-5666
ENGEL, PEDRO	HEWLETT-PACKARD	303-229-3809
HIJAB, RAIF	AMD	408-749-2250
HILL, IRA	EXAR	408-434-6400
HOANG, HOANG*	SGS-THOMSON	214-466-7182
LANGLEY, BRIAN	HEWLETT-PACKARD	415-857-8204
LE, TAM	SGS-THOMSON	214-466-7081
MARCOUX, PAUL	HEWLETT-PACKARD	415-857-5415
REEDHOLM, JIM	REEDHOLM INSTRU.	510-490-5666
SNYDER, SCOTT	TEXAS INSTRUMENTS	214-995-1907
TRIMBLE, BILL	REEDHOLM INSTRU.	510-490-5666
TURNER, TIM	TURNER ENG. TECH.	817-491-9517

SIG ATTENDEES AT 1993 IRPS

* CO-CHAIRS