

“Fast Physics Based III-V On-Wafer Reliability Characterisation”, M. Brandt, Infineon Technologies AG; H. Ganis, V. Krozer, TU Chemnitz; M. Schüssler, C. Sydlo, B. Mottet, Institut für Hochfrequenztechnik, TU Darmstadt; S. Cassette, S. Delage, Thomson-CSF-LCR, H. L. Hartnagel, Institut für Hochfrequenztechnik, TU Darmstadt

“Effects of RTA and WSix-Polycide Gate Processes on MOSFET Reliability for Giga-bit Scale DRAMs”, D. Park, N.-J. Son, DRAM PA Team, DRAM Development Division, Samsung Electronics Co. Ltd.; J.-Y. Kim, TD Team, R&D Center, Samsung Electronics Co. Ltd.; W. Lee, DRAM PA Team, DRAM Development Division, Samsung Electronics Co. Ltd.

“Reliability Issues of Ultra-Thick Oxides”, U. Schwalke, M. Pölzl, T. Sekinger, M. Kerber, Infineon Technologies AG

“Characterization of Extrusion Formation During High Temperature Anneal”, J. Kelsey-Wynne, F. Chen, J. Furukawa, T. Sullivan, IBM Microelectronics, Technology RE

“LSF Technique to Analyze Intrinsic TDDB Failures”, H. Katto, Science University of Tokyo, Suwa College

“Wafer Level Reliability Testing of Hetrojunction Bipolar Transistors”, E. Sabin, J. Scarpulla, E. Kaneshiro, S. Dacus, TRW

“The Different Gate Oxide Degradation Mechanism under Constant Voltage/Current Stress and Ramp Voltage Stress”, Y. En, X. Kong, H. Luo, China Electronic Product Reliability and Environmental Testing Research Institute

“Surface roughness effects on I-V and C-V characteristics of ultra-thin gate MOS transistors”, J. Zhang, J. S. Yuan, University of Central Florida, School of Electrical Engineering and Computer Science

“Developing Aged SPICE Models for Hot Carrier Reliability Simulation”, Q. Ye, H. Terletzki, Infineon Technologies Corp.; W. Tonti, IBM Microelectronics, Semiconductor R&D Center

“An improved substrate current model for deep submicron CMOS transistors”, W. Li, J. S. Yuan University of Central Florida, School of Electrical Engineering and Computer Science

“Gate Oxide Integrity under AC Stress”, X. Duan, University of Central Florida, Department of Physics; W. Wu, J. S. Yuan, University of Central Florida, School of Electrical Engineering and Computer Science

“Electromigration performance for Al/SiO₂, Cu/SiO₂, and Cu/low-k interconnect systems subject to Joule heating”, W. Wu, J. S. Yuan, University of Central Florida, School of Electrical Engineering and Computer Science; S. H. Kang, A. S. Oates, Bell Labs, Lucent Technologies

“A Probabilistic-Physics-of-Failure/Short-Time-Test Approach to Reliability Assurance for Deep-Submicron Transistors and Optical Interconnects in Multi-GHz Chips”, A. Haggag, K. Hess, W. McMahon, K. Cheng, J. Lee, J. Lyding, University of Illinois at Urbana-Champaign, Beckman Institute

“Standardizing EM Structures for Evaluation and Qualification of Aluminum Alloys with Barrier Metals”, M. J. Dion, Intersil Corp.

“Analysis of Hot Carrier Effects of SOI NFD NMOSFET”, R. Zhang, Texas Instruments; P. H. Chan, HKUST; S. R. Banna, Intel Corp.; M. Chan, HKUST

“Implementation of short-time classical HC Stress for In-line WLR of sub-0.5um nMOSFETs”, R. Gonella, STMicroelectronics, Central R&D labs

“Improved ring oscillator design techniques to generate realistic AC waveforms for reliability testing”, H. Le, Agilent

“Methods for Increasing the Burn-In Efficiency”, K. Nierle, Infineon Technologies Corp.; A. D. Norris, IBM Microelectronics

“Off-state degradation of 170nm and 140nm buried LDD pMOSFETs with different HALO implants”, S. Holzhauser, A. Narr, Infineon Technologies AG