October 12-15, 1998

http://www.irps.org/irw/

IEEE/Integrated Reliability Workshop
P.O. Box 308
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PROGRAM ANNOUNCEMENT!

Workshop Experience

You are cordially invited to participate in the 1998 Integrated Reliability Workshop. *The Workshop provides a unique forum for sharing new approaches to achieve and maintain microelectronic reliability*. Here you will closely interact with your peers at moderated discussion groups, open poster sessions, presentations and special interest groups. All Workshop activities take place in a relaxed and rustic setting that promotes an atmosphere of interactive learning and knowledge sharing.

Major Technical Themes

Increased performance and reduced cost — these have driven rapid growth and unprecedented technical innovation in the semiconductor industry. To meet these demands, new materials and processes must be introduced for deep-submicron integrated circuit technology. These new materials necessitate new and revised physical models for reliability. Reflecting this need, discussion groups will focus on Cu metal and low-k dielectrics, ultra-thin oxides, ESD and new C-V techniques for reliability. The technical program includes a designing-in reliability session with papers on thermal modeling, Cu reliability, via reliability and stress voiding. A contributors to failure session provides papers on physical models for ultra-thin dielectric reliability. A reliability test structures session has papers on ESD and several novel techniques to assess plasma damage. A WLR session provides papers on oxide breakdown in a 64MB DRAM, and a new CV characterization technique. There are also tutorials on analysis of oxide data and DRAM design for reliablility.

'98 Workshop Features:

- **Keynote**
  Semiconductor Equipment Industry: Migration from Equipment to Entire Process Module Solutions
  Dennis Yost, Applied Materials
- **Group Discussions**
  - Interconnect Reliability–with focus on Copper
  - Oxides–ultra thin oxides
  - ESD–requirements, testing, & protection development
  - C-V measurements–its implication on reliability
- **Tutorials**
  - The Analysis of Oxide Reliability Data
  - Reliability Issues & the Develpment of Advanced DRAM Products
- **16+ Technical Presentations on:**
  - Designing In Reliability
  - Wafer Level Reliability
  - Contributors to Failure
  - Reliability Test Structures
- **Open Poster Sessions**
- **Special Interest Groups**

Keynote: Semiconductor Equipment Industry: Migration from Equipment to Entire Process Module Solutions—Dennis Yost, Applied Materials, Santa Clara, CA

In the 1960's and early '70s the semiconductor industry was characterized as a vertically integrated industry with each company building their own tools, developing their own technology, building their own chips for use in their own systems that were eventually sold. As the industry has matured and continues to mature, the vertical integration of the industry has for the most part dissolved and continues to evolve into disintegrated, highly specialized segments. IC designers are focusing on putting multiple macro-modules (DRAM, SRAM, MPU, Analog, etc..) together to produce the entire system on a chip. The foundries are focusing on getting and manufacturing the capability to produce all the technologies for the design houses. This is putting increased pressure on the semiconductor equipment suppliers to not only supply guaranteed individual equipment performance, but more recently guaranteed performance of sub-modules (Shallow Trench Isolation, Advanced Cu interconnect, etc.) that are used to build the macro-modules. For the interconnect, as an example, the defect density, electrical CD control, via resistance and required reliability performance are being evaluated and characterized in response to the demands. In fact guaranteed performance levels are not far off from being required by the customer as part of the module purchase. This eventual requirement has forced equipment suppliers to develop and enhance many of the capabilities related to electrical performance and reliability testing that typically only resided with their customers.

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Motorola
Harry A. Schafft
NIST

—over—

Tutorials

In our continuing effort to enhance the value of the workshop experience there will be a tutorial on Monday afternoon and one on Tuesday afternoon.

Monday Tutorial in Angora Room:

The Analysis of Oxide Reliability Data—William Hunter of Texas Instruments, Dallas, TX

Techniques for measuring gate oxide reliability, such as TDDB, voltage ramps, and current ramps have existed for a long time, but many of these are applied qualitatively. We discuss here detailed aspects of analysis methods which can be applied to these techniques to make absolute reliability determinations. Along the way, we discuss important aspects such as failure rate based methodologies, band-bending corrections to measured gate voltages, active gate oxide area scaling, and quasi-static lifetime transformations.

Tuesday Tutorial in Angora Room:

Reliability Issues & the Development of Advanced DRAM Products—Wayne Ellis of IBM, Essex Junction, VT

Because of the all points addressable array of minimum feature size structures, DRAMs have been a powerful vehicle to develop techniques and insights into the relationships between technology and the achievement of manufacturability and final product reliability. This tutorial will discuss how today's reliability issues are addressed in the realm of high performance DRAM product design and development. Because of increased demands for product performance in a wider market, the issue of functional reliability in the system electrical environment will be introduced. Discussion of functional reliability will cover how this issue can relate to and also be independent of traditional reliability issues. The tutorial will cover:

- Basic DRAM architecture and function.
- Design for reliability, testability and manufacturability techniques in DRAMs.
- Burn in.
- Functional reliability

Open Poster Sessions

The Technical Program will include two open poster sessions. *All attendees have the opportunity to present a poster to communicate their ideas and results on a technical project or issue.* Please indicate your intention to bring a poster by reserving a poster display board (32″ × 40″ or 81 cm × 100 cm) in the space provided on the registration form. Your work should be in Landscape format on 8½×11″ or A4 paper with a maximum of twelve pages. In addition, you are invited to submit a two-page abstract of your poster presentation for inclusion in the Workshop Final Report. This is a great opportunity for you to share your work with your peers.

Special Interest Groups (SIG)

The SIG program at the Workshop has been very successful in fostering collaborative work on important reliability issues and we look forward to continuing growth and renewal in our SIGs. The formation of SIGs is encouraged as a natural extension of the Discussion Group sessions. Anyone interested in more information about SIGs see http://www.irps.org/irw/sig/.

Discussion Groups

The evening discussion group program is regarded as a favorite highlight of the workshop experience. Attendees will have a choice of four topics on both Tuesday and Wednesday evenings. The same four topics will be discussed for 90 minutes each night. This year's topics are:

1. Interconnect Reliability - with a focus on copper

Moderators: Tim Sullivan (IBM) and Carl Thompson (MIT)

To meet anticipated requirements over the next 15 years, the U.S. National Technology Roadmap for Semiconductors (NTRS) charts an aggressive path for evolution of current interconnect technology. Insertion of new interconnect materials (Cu as the primary conductor, with refractory metal liners) is already underway, and, to stay on the NTRS timeline, insertion of new dielectric materials will be required in the near future. With interconnect lengths of kilometers per circuit, minimum line widths shrinking below 100nm, the number of metallization levels moving toward 10, and the use of an interconnect metal which must be fully isolated from the dielectric, enormous reliability challenges must be met during a period of rapid development of new materials and processes. The goals of this discussion group will be to identify areas of greatest concern, and share lessons learned, and anticipated needs.

Specific discussion topics will include:

- Can the same reliability approaches that were used for Al be applied to Cu?
- Is electromigration-induced failure still an issue for Cu-based alloys? What are the new design rules?; Are new design strategies enabled?, Are existing design strategies still OK?
- How do liners for Cu affect electromigration?
- Are there reliability issues with the liners themselves? How easy is it to insure that liners are continuous everywhere on a kilometer of interconnect?, Are there wear-out failure mechanisms for liners, such as cracking due to thermal cycling?, How can liner reliability be assessed?
- Are there new processing-related defects arising from Cu-based technologies which lead to reliability issues?, How important is Cu adhesion?, How significant are the differences in Cu deposition techniques?
- What are the implications of dual damascene vias?: Will liner integrity in vias be a problem?, Will aspect ratio uniformity be maintained ?, Will stress become an issue?
- How will the mechanical and thermal properties of Low-K dielectrics affect reliability?
- Are there other properties of Cu or Low-K, different from Al and SiO_2, which could bring in unanticipated reliability challenges?

2. Oxides - ultra thin oxides

Moderators: Rolf-Peter Vollertsen (Siemens) & Dave Dumin (Clemson Univ.)

A lot of open questions still exist in the area of oxide reliability. New aspects come into play when the oxide thickness is scaled down to only a few nm. What should we mainly be measuring, electric or thermal (catastrophic dielectric) breakdowns; non-destructive, soft- or quasi breakdowns; intrinsic and/or extrinsic breakdowns; Qbd, Tbd or Ebd? In really thin oxides, who cares if there are failures since intrinsic oxides conduct so much current anyway because it may be hard to tell when there is a short circuit in parallel with a leaky intrinsic oxide? Besides, a lot of bad things, like SILC's, Vt shifts, gm shifts, etc. happen long before intrinsic oxide failures. On the other hand aren't the extrinsic breakdowns much more important than the intrinsic? How is oxide reliability affected by the change conduction mechanisms from Fowler-Nordheim to direct tunneling? Especially, what effect has it on the reliability measurement methods? How, for example, will SILC or any other leakage current at low fields be monitored during highly accelerated stress measurements? How can a manufacturer sell a thin oxide with a low Qbd measured with traditional reliability test when the customer still requires the old target specs? What are the realistic future targets of ultra thin oxide reliability? How can we measure them?

Other discussion topics of interest are:

- Trap generation and its relevance to oxide breakdown.
- What does Qbd mean when the oxide thickness decreases?
- Influence of copper-metallization on oxide reliability.
- New lifetime extrapolation models for extrinsic and intrinsic breakdowns.
- Extrapolation to very low cumulative failure probabilities in the extrinsic region.
- Is a straight line fit in the Weibull plot valid?

3. Electrostatic Discharge - requirements, testing, protection development

Moderators: Horst Gieser (Fraunhofer IFT) and Steve Voldman (IBM)

Electrostatic Discharge is one of the major yield and reliability concerns for present and future technologies. The DC-breakdown voltages of gate

(continued on back of registration form)

1998 *International* INTEGRATED RELIABILITY WORKSHOP

PRELIMINARY PROGRAM

MONDAY, October 12

1:00 – 8:00 p.m. Lodge check-in. Get room assignment (prearranged) & room key, with lodge area map and information. (ADA please notify desk of special needs)

1:00 – 3:00 p.m. Registration: Pick up badges & handout (*Dining Room Lounge*) Sign up for Discussion Groups and SIG meeting

3:00 – 5:00 p.m. Tutorial Session #1: "The Analysis of Oxide Reliability Data" William Hunter of Texas Instruments, Inc., Dallas, TX *Angora Room* *(note tutorial session #2 is on Tuesday afternoon)*

5:00 – 6:00 p.m. Registration: Pick up badges and handout (*Dining Room Lounge*) Discussion Group Assignments/SIG signup

5:00 – 6:00 p.m. Mixer & Poster Session, *Cathedral Room*

6:00 – 7:30 p.m. DINNER, *Dining Room*

7:00 – 7:30 p.m. Registration for late arrivals (*Dining Room Lounge*)

7:30 – 9:00 p.m. Mixer & Poster Session, *Cathedral Room*

9:00 – 10:00 p.m. SIG Meeting (all SIGs), *Angora Room*

TUESDAY, October 13

7:00 a.m. BREAKFAST (until 8:00 a.m.)

8:15 – 8:30 a.m. Welcome & Introduction: Raif Hijab, General Chair, *Angora Room* Technical Program Overview: Eric Snyder, Technical Program Chair

8:30 – 9:30 a.m. Keynote: Semiconductor Equipment Industry: Migration from equipment to entire process module solutions—Dennis Yost, Applied Materials, Santa Clara, CA

9:30 – 10:00 a.m. Break

10:00 – 11:40 a.m. Session #1: Designing In Reliability (DIR), Harry Schafft, NIST, Chair

- DIR-1 "Thermal Conductance of IC Interconnects Embedded in Dielectric," J.P. Gill, T.D. Sullivan, and D.L. Harmon of IBM Microelectronics, Essex Junction, VT
- DIR-2 "Wafer Level Electromigration Applied to Advance Copper/Low k Dielectric Process Sequence Integration," Donald Pierce of Sandia Technologies, Albuquerque, NM; James Educato, Viren Rana and Dennis Yost of Applied Materials, Santa Clara, CA
- DIR-3 "Wafer Level Monitoring and Process Optimization for Robust Via EM Reliability," T. Zhao, C. Shih, J. McCollum, F. Hawley, F. Issaq, B. Cronquist, R. Lambertson, E. Hamdy of Actel, Sunnyvale, CA; Z. Yang, C. Chern, M. Liao, G. Say, G. Koh, L. Chan, R. Sundaresan of Chartered Semiconductor Manufacturing, Singapore
- DIR-4 "A Study of Stress Voiding Effect on AlSi Metal Bank Allowed Lifetime for a IC Foundry Fabs," K.P. Lin, C.D. Chang, K.S. Huang, S.L. Hsu of Taiwan Semiconductor Manufacturing Company Ltd., Hsin-Chu, Taiwan R.O.C.

11:40 a.m. – 12:10 p.m. Group Picture

12:10 – 1:30 p.m. LUNCH, *Dining Room*

2:00 – 4:00 p.m. Tutorial Session #2 in the Angora Room: "Reliability Issues & the Development of Advanced DRAM Products" Wayne Ellis of IBM, Essex Junction, VT

4:00 – 6:00 p.m. Poster Session/Late News Papers

6:00 – 7:30 p.m. DINNER, *Dining Room*

7:30 – 9:00 p.m. Discussion Groups (90 minute parallel sessions for each topic) Attendees are to participate in one of the four groups:

1. Interconnect Reliability - with a focus on copper, *Angora Room*
2. Oxides - ultra thin oxides, *Old Lodge*
3. ESD Electrostatic Discharge - Requirements, Testing, Protection Development, *Cathedral Room*
4. C-V measurements, *Tallac Room*

9:00 – 10:30 p.m. Individual SIG Meetings

WEDNESDAY, October 14

7:00 a.m. BREAKFAST (until 8:00 a.m.)

8:15 – 8:30 a.m. Announcements, *Angora Room*

8:30 – 10:10 a.m. Session #2 Wafer Level Reliability (WLR), Gordon Claudius, Rockwell & Doug Menke, Motorola, Co-chairs

- WLR-1 "Practical Triggering of Early Breakdown in Thin Oxides," J.C. Jackson and D.J. Dumin of Clemson University; Clemson, SC and Cleston Messick of Fairchild Semiconductor, West Jordan, UT
- WLR-2 "Complete method for Ebd Correction by Series Resistance Characterization," David K. Monroe and Scot E. Swanson of Sandia National Laboratories, Albuquerque, NM
- WLR-3 "A Constant Gate Current Technique for Obtaining Low-Frequency C-V Characteristics of MOS Capacitors," Jack G. Qian and Roy A. Hensley of Dallas Semiconductor Inc., Dallas, TX and Eric Littlefield of Hewlett-Packard Co., Englewood, CO
- WLR-4 "The Life Time Model using the Correlation between Dielectric Thickness, and Voltage Stress for 64MB Accelerated Reliability Testing," Yumi Kwon, Namhyun Cha, Samjin Whang, Namsung Cho, Whajoon Lee of Samsung Electronics Co. ltd; Yongin-City, Kyungki-Do, Korea

10:10 – 10:30 a.m. Break

10:30 a.m. – 12:10 p.m. Session #3: Contributors to Failure (CTF), John Suehle, NIST & Prasad Chaparala, National Semiconductor, Co-chairs

- CTF-1 "Electric Field and Temperature Acceleration of Quasi-Breakdown Phenomena in Ultrathin Oxides," D. Roy, S. Bruyere and E. Vincent of ST Microelectronics, Crolles, France; G. Ghibaudo of LPSC/ENSERG, Grenoble, France
- CTF-2 "A Comprehensive Physical Model of Oxide Wearout and Breakdown Involving Trap Generation, Charging and Discharging," D. Qian and D.J. Dumin of Clemson University, Clemson, SC
- CTF-3 "A Preliminary Investigation of the Kinetics of Post-Oxidation Anneal Induced E'-Precursor Formation," J.F. Conley, Jr. and W.F. McArthur of Dynamics Research Corp., Beaverton, OR and P.M. Lenahan of Pennsylvania State University, University Park, PA
- CTF-4 "A New Mechanism for Gate Oxide Degradation," Chuan H. Liu of United Microelectronics Corp., Hsin-Chu, Taiwan, R.O.C.; Thomas A. DeMassa of Arizona State University, Tempe, AZ; and Julian J. Sanchez of Intel Corp., Chandler, AZ

12:15 – 1:30 p.m. LUNCH, *Dining Room* (Take out Lunch bags available)
1:30 – 6:00 p.m. Open The afternoon is free for discussion, hiking and other recreation
6:00 – 7:30 p.m. DINNER, *Dining Room*
7:30 – 9:00 p.m. Discussion Groups (90 minute parallel sessions for each topic) Attendees are to participate in one of the four groups:

1. Interconnect Reliability - with a focus on copper, *Angora Room*
2. Oxides - ultra thin oxides, *Old Lodge*
3. ESD Electrostatic Discharge - Requirements, Testing, Protection Development, *Cathedral Room*
4. C-V measurements, *Tallac Room*

9:00 – 10:30 p.m. Individual SIG Meetings

THURSDAY, October 15

7:00 a.m. BREAKFAST (until 8:00 a.m.)
8:15 – 8:30 a.m. Announcements, *Angora Room*
8:30 – 10:10 a.m. Session #4: Reliability Test Structures, John Conley, DRC & Homi Nariman, AMD, Co-chairs

RTS-1 "ESD Technology Benchmarking for Evaluation of Electrostatic Discharge Robustness of CMOS Technologies," S. Voldman of IBM Microelectronics, Essex Junction, VT; W. Anderson of Digital Equipment Corporation, Shrewsbury, MA; R. Ashton of Lucent Technologies, Orlando FL; M. Chaine of Texas Instruments Inc., Houston, TX; C. Duvvury of Texas Instruments Inc., Dallas, TX; T. Maloney of Intel Corp., Santa Clara, CA; and E. Worley of Rockwell Semiconductor Systems, Newport Beach, CA

RTS-2 "Non-Contact In-Line Monitoring of Plasma-Induced Latent Damage," Tim Turner and Steve Weinzierl of Keithley Instruments, Cleveland, OH

RTS-3 "Monitoring Charging in High Current Ion Implanters Yields Optimum Preventive Maintenance Schedules and Procedures," Henry Gonzalez, Steven Reno, Cleston Messick of Fairchild Semiconductor, West Jordan, UT; Wes Lukaszek of Wafer Charging Monitors, Woodside, CA; Thomas Romanski of Eaton Corporation, Tempe, AZ

RTS-4 "Characterizing Electron Shower with CHARM-2 wafers on Eaton NV-8200P Medium Current Ion Implanter," Steve Reno, Henry Gonzalez, and Cleston Messick of Fairchild Semiconductor, West Jordan, UT, Wes Lukaszek of Wafer Charging Monitors, Woodside, CA; David A. St. Angelo, Klaus Becker and Bobby Rogers of Eaton Corporation, Austin, TX

10:10 – 10:30 a.m. Break (checkout at this time if not staying for JEDEC meeting)
10:30 – 10:45 a.m. Discussion Group Summaries
10:45 – 11:05 a.m. SIG Report
11:05 – 11:30 a.m. Wrap-Up
noon – 1:30 p.m. LUNCH, *Dining Room*
Workshop Ends—Leave the Stanford Sierra Camp unless attending JC14.2
2:00 p.m. JEDEC 14.2 Committee on Wafer Level Reliability Meeting

✂ *(cut ✂ here and mail bottom portion)* ✂

1998 IRW REGISTRATION FORM (Use also for reserving accommodations to EIA/JEDEC Committee JC14.2 meeting, Oct. 15-16)

(Please type, print clearly, or attach business card)

NAME: ______________ (Last) ______________ (First) ______ (Initial) TITLE: ______________

COMPANY: ______________________________ Mail Code

ADDRESS: ______________________________

______________ City ______________ State/Country ______________ Zip/Postal Code

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❍ Address is HOME, Company not to be included on mailing label
❍ Please check here if you do not wish to receive mail other than from IRW & IRPS
❍ Please check here if under the Americans With Disabilities Act, you require any auxiliary aids or service. Please call (315) 339-3971.

For rooming assignments, please check one: male ❍ female ❍

Each Attendee will only attend one Discussion Group each night. Please Indicate your Discussion Group Preference

Tues	Wed	Discussion Group
		Interconnect Reliability – w/focus on Cu
		Oxides – ultra thin oxides
		ESD – req'mnts, testing, protection developement
		C-V measurements

❍ WILL ❍ WILL NOT ATTEND MONDAY TUTORIAL (3-5 p.m.).
❍ WILL ❍ WILL NOT ATTEND TUESDAY TUTORIAL (2-4 p.m.).

REGISTRATION FEES (US$)

IEEE Member ______________ (member No. Req'd) . $900* ________
NON-IEEE Member .... $950* ________
* *Includes meals, lodging, Handout, & Final Report. (Mon. eve., Oct. 12 – Thur. noon, Oct. 15)*
EXTRA COPIES of Workshop Final Report ..... Qty: ______ x $80 ________
JC14.2 accommodations .... $160† ________
TOTAL REMITTED $ ________

Meeting registration automatically includes a room reservation.

SORRY, WE DO NOT TAKE CREDIT CARDS

☐ MAKE CHECKS PAYABLE TO **"IEEE INTEGRATED RELIABILITY WORKSHOP"**

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P.O. Box 308
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For registration information:
phone: 315-339-3971
FAX: 315-336-9134
email: iirw@compuserve.com
http://www.irps.org/irw

YOUR POSTER TITLE: ______________________________

You will be provided with a poster board for one of the poster sessions to share your ideas and your results on a technical topic or issue. Instructions will be sent to you if you register for a poster. You will be provided with a 32" x 40" poster board.

**The Workshop Registration Fee includes: your housing accommodations at the Stanford Sierra Camp cabins, all meals and refreshments (no-host bar), on-site recreation activities, parking for your car, the Presentation Viewgraph Booklet (at the workshop), and the Final Report (after the workshop).*

†*The JEDEC Committee fee for accommodatons includes: housing on Thursday night, meals (from dinner on Thursday through buffet lunch on Friday), refreshments, and parking for your car.*

CANCELLATION fees: $50 AFTER SEPTEMBER 18; FULL FEE AFTER OCTOBER 2

RESPONSIBILITIES OF ATTENDEES

You are expected to come prepared to participate actively in the discussions and meetings by sharing your experiences, concerns, questions, views, technical information, and test data, as appropriate. Your active involvement in the formal, as well as in the informal meetings and activities, is the key ingredient for maximizing the value of the workshop for you and your fellow attendees.

ARRANGEMENTS INFORMATION

Air Travel Group Rates: The IEEE/EDS has arranged for Group rates with **United Airlines**: 5% off the lowest available fare. Call 1-800-521-4041 to check restrictions and fares. Provide United with the Meeting ID Number: 513NU.

Transportation Note: The Stanford Sierra Camp is located on Fallen Leaf Lake, a few miles from South Lake Tahoe. The nearest major airport is the Reno International Airport. Reno is approximately two hours from Stanford Sierra Camp. Currently no commercial flights are available to the South Lake Tahoe Airport.

- Transportation is available from Reno International Airport to the South Lake Tahoe terminus at Horizons Casino via the ***Tahoe Casino Express***. For ***Tahoe Casino Express*** schedule details see back of registration form or call 800-446-6128.

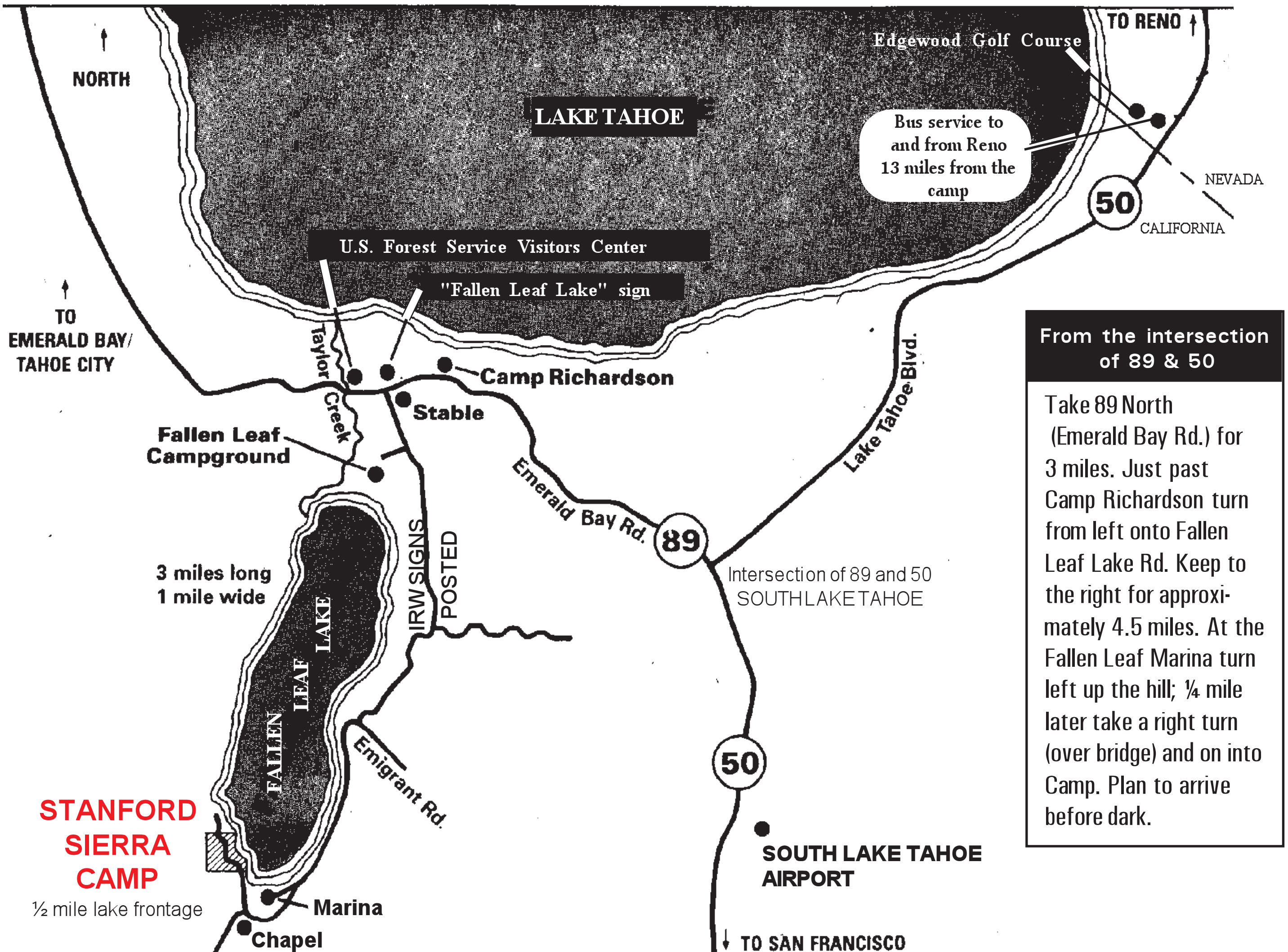
ACCOMMODATIONS

The Stanford Sierra Camp provides an ideal setting for the workshop. The isolated location and the absence of distractions, such as in-room phones and television sets, encourages extensive interaction among the Workshop attendees. Clusters of 2 and 3 bedroom cabins are nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake. Please note; while each attendee is assigned a bedroom, bathroom facilities within each cabin are shared. All rooms have decks with magnificent views of Fallen Leaf Lake and surrounding Sierra peaks.

- **All participants must stay at the camp during the workshop.**
- **We cannot accommodate spouses or any companions at the camp**.
- **Accommodations are *not* available at the Stanford Camp for any day before or after the workshop.**
- Smoking is permitted outdoors only. Smoking will not be permitted in the sleeping or meeting rooms.
- Arrangements can be made for those with special dietary or physical requirements. Please send your requirements with the registration or call 315-339-3971.
- A message board will be available for incoming calls, (916) 541-1244. There are pay telephones for outgoing calls. There are no telephones in the rooms.

WHAT TO BRING

It may be cold or warm at 6000 feet in the Sierra in October. We recommend that you bring warm clothing and a coat. Comfortable, informal dress is encouraged. No suits, ties, or high heels please. You may want to bring hiking shoes. There are numerous outstanding hiking trails around the camp. A small flashlight would be helpful to find your cabin after dark.



TAHOE CASINO EXPRESS

The Tahoe Casino Express runs from Reno to Tahoe between 6 a.m. and midnight with departures from Reno at: 6:15 a.m., 8:15, 9:15, 10:15, 11:15, 12:15 p.m., 1:15, 2:15, 3:15, 5:30, 7:30, 9:30, 10:30 and 12:30 a.m.. The Express costs $17 each way ($30 round trip) and tickets can be purchased at the Express counter located in the baggage area in the Reno airport. Travel time is approximately 1½ hours. The Casino Express can be reached at 800-446-6128.

The Express leaves the Horizon Casino at Lake Tahoe and returns to Reno on the following schedule: 4:10 a.m., 6:10, 8:10, 9:10, 10:10, 11:10, 12:10 p.m., 1:10, 2:10, 3:10, 4:10, 5:10, 7:25, and 10:25 p.m. Tickets may be purchased in the Horizon Casino at the main cashier's cage.

Stanford Sierra Camp offers courtesy transportation for conference attendees from the Horizon Casino between 10 a.m. and 10 p.m. on Registration Day (Monday, Oct. 12). Return trips to the Casino are offered on the last day of the conference only. If you are planning on using the Casino Express, please notify Stanford Sierra Camp (916-541-1244) at least ONE WEEK prior to your arrival date. The IRW is offering emergency service to and from the casino. If you find yourself stranded, please call the camp at the same number.

DISCUSSION GROUPS *(continued from page 2)*

oxides go below the trigger voltages of pn-junctions used for protection. Thus, the realization of effective protection elements becomes a real challenge and the risk of ESD damage in the core increases, especially for Charged Device Model (CDM) events. Increased amounts of energy and discharge current should be handled safely by smaller protection structures with minimum parasitic effects on the RF-performance. High pin counts, chip size packages and CDM-situations are raising many questions on how to protect these devices and how to test and qualify their ESD-protection reliability. Demanding development cycle times do not allow the trial-and-error method while calling for better wafer level (test) methods and more effective use of electro-thermal simulations. The discussion group intends to discuss the current approaches for these problems and to identify future needs with possible solutions.

Further topics of interest may be:

- How much protection is necessary?
- Technology versus design influence.
- Charged device model/socket discharge model & real world.
- Transmission line pulsing.
- Sub-nanosecond pulse methodology
- Process impact and process monitor methods.
- Failure criteria.
- ESD and reliability.
- Failure analysis.

4. C-V MEASUREMENTS - AND ITS IMPLICATION ON OXIDE, TRANSISTOR AND NON-VOLATILE MEMORY CELL RELIABILITY

Moderators: Udo Schwalke (Siemens) and Barton Gordon (Materials Development Corporation)

For several decades, the capacitance-voltage (C-V) method has been a popular tool to study semiconductor and oxide properties. For example, the extraction of SiO_2/Si interface state densities together with their distribution in the band gap and the determination of fixed oxide charges provided useful information for the understanding of MOS degradation phenomena and oxide breakdown. However, after so many years, is the C-V method still of interest and what is currently its implication on oxide, transistor and non-volatile memory cell reliability? It is the aim of the discussion group to sample the present extent of use of C-V techniques among the participants, discuss possible applications of C-V measurements within the framework of MOS reliability and evaluate some recent developments in the field of C-V measurements.

Discussion Topics:

- Ultra thin gate oxides: How to measure the oxide thickness accurately?
- Impact of slow traps on quasi-static C-V characteristics: What do I measure?
- Drawbacks of a fixed ramp rate: Waste of time and loss of information?
- Minority carrier lifetime, deep-depletion profiling: Monitoring Si damage?
- Limits of C-V measurements and their correlation to reliability testing.
- Problems inherent in measurements of very thin or very thick oxides.
- Is C-V dead?
- Will C-V be replaced by non-contact techniques?

JEDEC 14.2 MEETING

The JEDEC 14.2, Wafer Level Reliability Standards Committee, meeting will be held immediately after the Workshop at the Stanford Sierra Camp on Thursday afternoon and Friday morning. Members, alternates, and guests are welcome. The cost for the accommodations is $160.00, which includes Thursday night dinner and lodging *and* Friday breakfast and lunch. All attendees must leave the camp after lunch on Friday. If you have any questions or if you want to become a member of JC-14.2, please call the JEDEC office at (703) 907-7558 or www.jedec.org or call Mike Dion, JC-14.2 Chair, at (704) 724-7067.

MORE INFORMATION

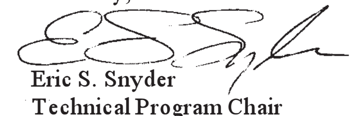
We expect an exciting workshop again this year. We look forward to your active participation in the many Workshop activities and your valuable contribution to the technical discussions. If you have any questions, please contact the Technical Program Chair, Eric S. Snyder, by phone, 505-872-0011, or fax, ...0022, or e-mail: snyderST@aol.com, or the General Chair, Raif S. Hijab, at (510) 624-7213...fax...249-4260 rhijab@corp.cirrus.com.

REGISTER NOW!

Complete and mail the enclosed registration form. Please register early. We have sold out in previous years. Space at the Camp limits the Workshop to roughly 120 attendees.

We look forward to seeing you at the '98 Workshop!

Sincerely,



Eric S. Snyder
Technical Program Chair