Discussion Group Summary

C-V Measurements - and Its Implication on Oxide, Transistor and Non-Volatile Memory Cell Reliability

moderated by

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Introduction

The C-V Measurements Discussion Group met to examine the role of the C-V technique in device reliability. Attendees with varied backgrounds participated. The topics of discussion were guided by the questionnaire shown in Appendix I.

Background	Tuesday	Wednesday
Manufacturer	12	13
Vendor	2	2
Research/Academic	4	4
Other	1	0

C-V Measurement Usage

Most attendees employed both high frequency and quasi-static C-V measurements to complement their reliability studies. The general consensus was that C-V techniques were easy to use and produced useful information about oxide thickness, trap density and flatband voltage. One participant did not use C-V information in TDDB testing.

C-V Measurement Problems

Attendees raised measurement and analysis issues for both thick and thin oxides. Thick oxides offer insufficient capacitance change for accurate analysis. Thin oxides (less than 5 nm) are difficult to measure because of current flow due to either tunneling or conduction. Quantum mechanical effects and poly gate depletion invalidate the simple relationship between accumulation capacitance and oxide thickness and complicate analysis of thin oxide C-V data. Users either employed quantum simulation of quasi-static C-V data or flatband voltage models for high frequency C-V data to determine oxide thickness and channel doping.

One attendee reported discrepancies in oxide thickness values determined by C-V measurements and by ellipsometry. Poly depletion and quantum effects were offered as an explanation of this.

C-V measurements, in particular quasi-static C-V, were considered time consuming and inefficient. This is due to the slow fixed ramp rates used to achieve equilibrium. In order to improve efficiency, an adaptive C-V technique was proposed which uses a variable time-delay to achieve optimized, equilibrium controlled sweeps. The equilibrium time constant can be recorded as a function of gate voltage which will provide additional information on the MOS system (i.e. minority carrier generation, slow traps etc.)

Other C-V Measurements

Problems with other measurements based on C-V techniques limited their use in actual test structures. The use of protection diodes precluded deep depletion measurements of capacitance-time characteristics to find minority carrier lifetime. Also, C-V for doping profiling was considered to be less useful in view of deep sub-µm CMOS. Limitations to access doping close to the oxide interface due to Debye-length limit and insufficient depth resolution were mentioned. Pulsed C-V techniques would help to extend deep depletion profile, but the usable maximum voltage is reduced by the thinner oxides due to dielectric breakdown.

C-V Measurement Priorities

Most attendees were satisfied with the accuracy of their C-V instrumentation. They were disappointed with the lack of universally accepted software for the extraction of critical values from both high frequency and quasi-static C-

V data from thin oxide devices. Oxide thickness, interface trap density and threshold voltage values had high priority.

Summary

C-V measurements continue to be an important technique used in device reliability applications. However, the analysis methods available have not kept up with the trend towards ultra thin oxides. Integration of proven data analysis software to account for quantum effects into C-V measurement packages offered by the leading C-V equipment manufactures would be highly desirable. In addition, novel C-V measurement techniques to account for leakage currents in direct-tunneling oxides (< 3nm), direct observation of very slow traps and improved measurement efficiency are also on the wish-list. These challenges will insure that the field of C-V measurements remains an active area of research.

Acknowledgment

We would like to thank all attendees for their interest, their challenging questions and valuable contributions.

Appendix I

Questionnaire:
(Original questionnaire available at:
http://www.irps.org/irw/dg_ques.htm)

1. Do you use C-V measurements at your facility to complement MOS reliability studies?
If your answer is YES,
(a) please specify the reliability studies of interest (e.g. oxide breakdown, BT-stress, transistor degradation, NVM cell reliability, etc.),
(b) the C-V technique you use (e.g. LF and/or HF C-V, etc.) and the parameters you extract (e.g. oxide thickness, interface state densities, etc.)
(c) please state your motivation for choosing C-V measurements in reliability studies
(d) please briefly summarize your experiences with C-V measurements (what has worked well and where did you find problems)

2. If your answer is NO,
(a) please explain why
(b) please mention the alternatives you are using instead of C-V

3. What do you think are the major advantages of C-V measurements?
(a) needs only very simple MOS test structures (capacitors)? (Y/N)
(b) data interpretation straight forward? (Y/N)
(c) easy to be implemented, commercially available? (Y/N)
(d) what else? (please list)

4. What are the drawbacks/limitations of C-V measurements?
(a) measurement time? (Y/N)
(b) signal-to-noise requirements? (Y/N)
(c) what else? (please list)

5. Do you consider C-V measurements useful for following reliability studies?
(Y/N; please comment)
(a) In-line monitoring of process damage (plasma damage, implantation damage) and its correlation to MOS quality and reliability
(b) Studies on the degradation mechanisms of ultra thin oxides, incl. soft breakdown phenomena
(c) Investigation of NVM cell reliability
(d) Any other suggestions? (Please indicate)