Discussion Group Summary Report

Electrostatic Discharge – ESD

Moderated by:

Horst Gieser
Fraunhofer IFT
Hansastr.27d
D80686 Munich
GERMANY
Tel: ++49-89-54759-020
Fax: ++49-89-54759-475
gieser@ift.fhg.de

Eugene Worley
Rockwell Semiconductors
MS/ 503-260
3411 Jamboree Road
Newport Beach , CA 92658-8902
U.S.A.
Tel: (714) 833-4922
eugene.worley@rss.rockwell.com

INTRODUCTION

The Quality and Reliability Council of Sematech has rated Electrostatic Discharge as number three of the yield and reliability problems for future integrated circuits. The DC-breakdown voltage of ultra thin gate oxides falls beyond the breakdown trigger voltage of regular pn-junctions thereby reducing the safety margin for protection schemes and demanding alternative solutions. Smaller protection structures with a low level of parasitic effects are required for RF-performance and also should handle increased amounts of energy and discharge currents. The risk for ESD damage in the core increases for both Human Body Model HBM and Charged Device Model CDM events. High pin counts, chip size packages and CDM-situations are raising many questions on how to protect these devices and how to test and qualify their ESD-protection reliably with minimum resources. Demanding development cycle times do not allow the trial-and-error method and call for better wafer level (test) methods and effective use of electrothermal simulations.

The following topics were suggested:

- How much protection is necessary?
- Technology versus design Influence
- Process impact and process monitor methods
- Failure criteria
- Failure analysis
- ESD and reliability
- Package trends and ESD
- Charged Device Model CDM, SDM, do we need it for Real World?
- How to guess sub-nanosecond single shot pulses ?
- Transmission Line Pulsing - from lab method to qualification method
- Wafer level ESD-qualification ?

The discussion group intended to discuss the current approaches for these problems and to identify future needs with possible solutions.

ATTENDANCE

11 attendees - nearly exclusively from industry – participated. Only few of them were already experienced in the field of ESD. It became obvious that in most companies ESD is tackled by specialists who attend other conferences on a regular basis. WLR-attendees that were not able to participate suggested that a third discussion group on Monday night might attract more attendees to side topics of WLR in the future. A tutorial would be helpful to introduce the current status.

10	Industry
1	Applied Research
> 6	IC-Manufacturers

DISCUSSION SUMMARY [1]

The moderators started the meeting providing an overview over typical ESD-failure signatures and explained test techniques that reproduce these failure signatures and are used to quantify the level of ESD-susceptibility. They pointed out that the discharge current is the dominant parameter for both - HBM Human Body Model and CDM Charged Device Model. In case of the CDM the discharge duration is on the order of few ns, while the peak current may reach several tens of Amperes depending on the capacitance to ground, the inductance and the pre-charge voltage of the device. Therefore, every Ω of resistance in the power bus translates into a voltage drop of tens of Volts which adds to the voltage drop across the protection element and stresses the oxides. Both stress models are necessary in order to cover the full spectrum of ESD-related failure signatures. HBM discharge is in many cases responsible for burned out junctions, low-level leakage of LDD-transistors and for metal fusing in conjunction with narrow power buses.

[1] This summary reflects the personal opinion and view of the moderator and may not reflect a commonly agreed position of the group.

HBM may address gate oxide failures too. However, CDM and its derivatives, which better represent today's manufacturing ESD stress environment, produce gate oxide damage more frequently. While the failure sites are most often located in the circuitry of the discharged pin internal HBM and CDM-failures have been seen that resulted from weak clamping of the different supply rails against each other. These internal gate oxide ruptures, that may cause a marginal leakage current (50 nA.. few µA) are in particular difficult to identify during the regular parametric and functional test without IDDQ test. They were identified earlier to have a high probability of failing lethally during burn-in (BI), or due to subsequent low level pulse stress (<50V HBM). Careless product analysis of BI-fails could lead to the conclusion of weak gate oxides. SDM (Socket Discharge Model) may result in more severe damage.

In general, HBM tests are demanded by customers as well as by internal specifications. 2kV HBM seems to be acceptable for standard parts although special RF-parts (GaAs) may fail below 100V and others require 15 to 25kV. Despite correlation problems Machine Model test is still in limited use although few people have yet reported MM-specific field failures. The majority of ESD-related yield loss has been reported as coming from CDM and its derivatives. Although many semiconductor manufacturers are performing CDM/FCDM and/or SDM-tests to identify weak designs, uncertainties about the test standards and the poor correlation in terms of failure voltage between these testers has hindered the introduction of formal tester specifications. In general, devices that withstand 1 kV CDM are considered to be robust but in many cases, this figure is difficult to achieve. Although the calibration of the CDM-tester and single shot metrology setup is limited to a bandwidth of 1 GHz, devices with short leads are known to discharge much faster in the real world.

Reproducibility of a test method is key for the acceptance of an ESD-stress model.

ESD-PROTECTION

Protection circuits and schemes relying on breakdown devices (Diodes, gg-NMOS, SCR) and (distributed) active supply clamps in conjunction with forward biased diodes were discussed. The latter approach is in particular useful for digital products that are made in different technologies. Ultra thin oxides might require diode strings in forward bias. While standard inputs seem to be of little concern, power sequence dependent multiple-voltage IOs and high-voltage programming pins of flash memories require careful design. More detailed descriptions of protection structures and schemes can be found in the Proceedings of the EOS/ESD-Symposium, and the reference books of C.Duvvury and T.J. Maloney. Furthermore, in Feb98 Sematech released the document "Test Structures for Benchmarking the ESD Robustness of CMOS-Technologies" to the public (visit www.sematech.org/public/docubase/abstract/3452atr.htm) It defines a standard set of test structures to be evaluated in high current and voltage ranges and a strategy of implementation and tabulation for various technologies.

A significant interest in electro-thermal modeling and simulation of the ESD-protection scheme has been expressed in the questionnaire although the time was too limited for discussion. Only few companies are already working on numerical simulation of ESD-events.

FUTURE PERSPECTIVES

Although there are already devices (µ-BGA, MCM) with more that 1000 pins on the market and up to 5000 are predicted, the number of companies that have to test integrated circuits with more than 512 pins is still very limited. No HBM test systems with more than 1024 pins are on the market requiring new test strategies.

The principles of ESD-qualification tests may need some careful reconsideration to be valid in terms of physics. For current induced failure modes, pre-charge voltage is only meaningful for a well defined discharge circuit. This pre-requisite is lost for CDM at the latest and may be lost for high-pin count HBM too. Reproducibility of CDM is dominated by the air discharge with vague electrode configurations.

High current square pulses generated by transmission lines with well defined impedances should help to solve problems. Here the discharge takes place in a relay. Today these TLP-setups with pulse metrology are used for the ESD-hardening of technologies and protection elements and provide quantitative insights for the calibrated simulation in the high current domain. They are used to debug pad cells of products, but it requires a common understanding between customers and manufacturers of ICs as well as of automated test systems to qualify products. Very fast square pulses have the potential to replace CDM and SDM by a method that identifies weakness on chip- or even wafer level (CC-TLP). The combination of the chip and a ground plane above it, acts as a capacitor that differentiates the square pulse. The assumption is that a robust device on chip-level will survive in any package. Further correlation studies are necessary.

It has been commonly agreed that the only purpose of all ESD-protection schemes and all ESD-test effort is to avoid yield loss and field returns caused by Electrostatic Discharge. Our mission is to harden ICs for the Real World and to identify physically meaningful and re-

producible test methods that reproduce field failures and identify weak designs in a very early stage of the design and manufacturing process of an integrated circuit. Neglecting the momentum of HBM-, MM-, CDM- test data bases that have been established for years, square pulses on wafer level and/or packaged devices have a very high potential for the qualification of future devices.

Robust gate oxides and metallization should be looked at from the perspective of WLR and ESD in the future.

QUESTIONNAIRE

0) Are you semiconductor customer (a) or supplier (b)?

1) What is your primary job function?

2) How would you rate your expertise in
(Beginner 0...5 Expert)
a) ESD - protection design
b) ESD - technology hardening
c) ESD - testing
d) Numerical simulation for ESD
e) Failure analysis
f) Generation and metrology of sub-ns pulses

3) What kind(s) of technology (ies) are you involved with?

4) What kind of high current tests are you performing ?
a) HBM MIL
b) HBM ESDA
c) HBM JEDEC
d) HBM EIAJ
d) MM ESDA
e) MM JEDEC
f) CDM ESDA
g) CDM JEDEC
h) SDM ESDA
i) Transmission Line Pulsing
j) None

5) What kind of high current tests are you outsourcing ?
a) HBM MIL
b) HBM ESDA
c) HBM JEDEC
d) HBM EIAJ
d) MM ESDA
e) MM JEDEC
f) CDM ESDA
g) CDM JEDEC
h) SDM ESDA
i) Transmission Line Pulsing
j) None

6) Are you satisfied with repeatability and correlation ?
a)yes b)no
Which stress models, technologies, particular cases ?

7) Are you performing (a) or would you perform (b) wafer level ESD tests ?

8) Do you disagree 0 ... 5 fully agree ?
"Chip scale packages and flip chip assemblies minimize the influence of the package on the ESD-failure threshold"

9) Are the demands for stress models and withstand voltages mainly driven by
a) the customers ?
b) the competition ?
c) the internal quality policy ?

10) How much protection in which model is sufficient to survive Real World?
Is it increasing or decreasing with time ?

11) What are your and your customers requirements to accept an alternative qualification procedure for ESD ?

12) Did you see reliability problems traceable to ESD ?

13) Please comment on my point of view that the goals of CDM/SDM or whatever very fast transient ESD-testing should be (disagree 0 ....5 fully agree)

a) to have a test method available that reproduces failure signatures of field failures, that cannot be reproduced by HBM and MM.
b) to be able to detect a CDM-sensitive design as early as possible in the process.
c) to be able to quantify the amount of stress that a device can withstand before it fails with the typical failure signatures independent from the individual test system.
d) to have a reproducible method for the whole stress scale.
e) to have a test method and standard available that complies with the rules of physics and can thus be adapted to the tools (oscilloscopes etc) that are technically available.

13) How important is or will modeling and numerical simulation of ESD be for your company ?
(Not even thinking about 0 ... 5 extremely)

14) Can you contribute case studies in any of the above topics to the workshop ? For a fruitful discussion, they are highly appreciated, independent of the level. Can you provide material in advance? (Even published!)