Discussion Group Summary

OXIDES - ultra thin oxides

moderated by

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Introduction

Gate oxide thickness is continuously scaled down to meet aggressive performance targets. Today a 6 nm oxide is called ”thick” and 1.5 nm oxides are expected to hit manufacturing in less than 10 years according to the SIA roadmap. New aspects come into play when the oxide thickness is scaled down to only a few nm. Some of these aspects were put in a questionnaire which was available on the Internet and is reprinted in the appendix. The intention of the questionnaire was to get an idea of the background and opinion of the people in the group. Four responses to the questionnaire were received by e-mail before the workshop and 13 people answered the questionnaire at the first discussion session (total return: 17). The results of the questionnaire were reviewed on both evenings. Six out of the nine questions were used to initiate discussions. Additional topics came up during the discussion.

Attendance

A show of hands at each session start revealed the assembly of the group. Due to some people joining later the numbers given in the table below might by slightly off.

	Tuesday	Wednesday
developers	6	15
manufacturers	7	10
customers	2	2
research	6	3
vendor	1	4
total	≥22	≥34

Answers of Attendees to the Questionnaire

The thinnest oxide thickness in which participants have experience started as low as 2 nm and ranged up to 10 nm with a majority in the sub 6 nm range. Mostly time to breakdown is measured (CVS) but some use fast methods measuring Ebd. There was common ground on the question which voltage acceleration plot is preferred. Other questions resulted in opposite opinions (see appendix for details) and were used to get the discussion started. Despite a relatively clear vote in the questionnaire the most time was spent on the discussion of hard breakdown vs. soft breakdown (question 3).

Discussion Results

On both evenings we talked about a range of topics including the issues in the questionnaire (questions 3, 4, 6-9). Here is a summary of the topics we focused on:

In the first session the opinion on soft or quasi breakdown was that it would be restricted to a range between 3 and 5 nm and that it would occur only at high fields (>7MV/cm). Also it would be more prevalent on capacitors with larger area. So the conclusion was that soft breakdown is no problem at operation conditions and therefore only hard breakdown needs to be considered. During the second session it was stated that soft breakdown had been observed also on 2.5 nm oxide and that for 3 nm oxide available data down to 5 MV/cm show soft breakdown. Possible mechanisms for soft breakdown were discussed and it was suspected that the occurrence may also depend on the measurement equipment impedance. It was concluded that a verification of soft breakdown at operation condition is important. The influence of temperature on soft breakdown was unclear. On the other hand soft breakdown seems to be no problem for products which can drive enough current, like most logic circuits. A problem is expected on DRAMs and in analog circuits (due to mismatched devices).

Concerning the importance of extrinsic distributions, there was wide agreement. However, it was also felt that the intrinsic distribution needs to be checked to make sure it is well beyond end of product life. It remained open how

much it needs to be beyond end of life. Discussion on bimodal distributions clarified some special cases with odd shapes or lack of sufficient extrinsic data points. Furthermore, it was argued, that the extrinsic portion could be improved much more easily than the intrinsic portion, e.g., by yield learning, therefore the intrinsic distributions might be more important. Due to the effect of Burn-In the intrinsic distributions are more critical particularly if they are close to end-of-life.

The difference between SILC and soft breakdown was discussed and it was concluded that it is useful to monitor the leakage at operation condition by interrupting the stress. Circuit designers are supposed to provide an appropriate leakage criterion.

Trap formation models were discussed in both sessions. The differences in properties of radiation induced oxide damage (no bias) versus voltage stress induced damage was pointed out in this context.

A hot topic was the validity of extrapolation from highly accelerated stress conditions to operation condition. Some people saw no extrapolation problems for intrinsic distributions. Others supported the stress of packaged test structures at low voltages to verify the validity of the model. Someone suggested to simply use the correct model, but did not state what the correct model is.

Future Aspects which have not been fully discussed

Burn-In issues and their impact on gate oxide were topics which need future attention. Also the question of how much margin should a projection have to the end-of-life point remained open. Another unanswered question - despite intense discussion - was: are thinner oxides less reliable than thicker oxides at a given field? The suggestion from the questionnaire (appendix, #10) have not been considered. Soft breakdown and its relevance to product deserves future attention again.

Appendix

Questionnaire and analyzed answers

(Original questionnaire available at:
http://www.irps.org/irw/dg_ques.htm)

1. What is the oxide thickness range you have experience with (in nm)?
   Lower end of range: 2-6nm, 8.5 and 10 nm
2. What is your preferred way of reliability assessment? Choose one: tbd, Qbd, Ebd, other - please specify.
   9 tbd (CVS), 1 QBD (CCS), 3 Ebd,1 Vbd
3. What is the breakdown criterion used? Choose one or rank several: hard breakdown, soft breakdown, SILC, Vt shift, gm shift.
   13 hard breakdown, 4 soft (quasi) breakdown
4. Do you monitor the leakage current at low voltage during highly accelerated stresses?
   8 yes, 8 no
   a. If "No", is it necessary for oxides below 6 nm? (Yes or No)
      1 yes, 3 no , 1 only below 3 nm
5. Which voltage acceleration plot do you prefer? Choose one: E, 1/E, other.
   16 E, 1 1/E (no preference)
   a. If "other", please include short description and reference
6. Do you consider highly accelerated wafer level stresses sufficient? (Yes or No)
   5 yes, 10 no, 1 not sure
   a. If "No", are packaged module stresses at lower stress conditions required? (Yes or No)
   8 yes
7. Do the projections from med/high level stress represent the correct/worst case result at low voltage despite, e.g., a conduction mechanism change? (Yes or No)
   4 yes, 4 no, 9 not sure
8. Which fails are more important: extrinsic or intrinsic (wearout)? (extr. or intr.)
   10 extr., 1 intr., 3 both, 3 depends on conditions
9. Does a breakdown of ultra thin oxide affect the device function? (Yes or No)
   11 yes, 2 depends on condition, 4 not sure
10. Any further suggestions for the discussion?
    - breakdown criteria for ultra-thin oxides
    - how do we do Burn-In considering the strong field increase with the traditional approach of simple voltage scaling
    - correlation to product failure (assuming dominant failure mode)