

Discussion Group Summary

Interconnect Reliability--with a focus on Copper

Moderators

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Introduction

The Interconnect Reliability Discussion Group met twice, on Tuesday evening and on Wednesday evening, and was attended by 25 participants Tuesday and about 10 participants on Wednesday. The intended focus was to be on Cu, and as a way to organize thoughts and to provide a comparative basis for understanding Cu reliability, the initial portion of the discussion focused on issues in Al metallizations.

Discussion Summary

The 25 participants who attended the Monday night session all were experienced with, and involved in, reliability activities within their organizations. Because only two people had responded to the questionnaire, we began with discussion of question 2, what failure criteria were used. Some used a fractional or percentage resistance shift, such as 10% or 20%, some used an absolute value, such as 10 Ohms. Difficulty arises in trying to compare the performance of different technologies having shunt layers of different thickness, because the resistance change per void size depends on the resistance of the exposed shunt layer. A suggestion was made that all results be normalized to void size, which would be independent of resistance shift, but a difficulty with that is that the actual resistance shift might be important for some designs. Most people use percentage resistance shift, but few people had a method of normalization between structures of different length, or between different technologies.

We then discussed how moving from a RIE technology to a dual damascene technology would affect the measurement of electromigration and stress voiding. Significant differences could arise due to deposition methods, different types of liners and the geometry of the liners. The discussion on redundant layers and barrier layers stimulated the question

Whether barrier layers are designed with respect to the line current density. Most participants thought not. Even greater effects could arise by having the via material changed from tungsten (W) to aluminum (Al), because then the side wall coverage of liners would be thin and would affect the rate of resistance increase for voids forming in the vias.

When considering copper (Cu), we discussed the implications of having a pure material vs. an alloy such as AlCu. In the latter case the onset of void growth is postponed until the Cu is swept far enough away from the negative via to allow the Al to move. This effect is called incubation time,

and is expected to be absent in the case of pure Cu. Most people didn't attempt to measure incubation time in Al, but instead, measured the resultant time to reach failure. The absence of an alloying element in Cu changes the current dependency of EM failure from -2 to -1. Some concern was expressed that Cu vias would behave differently from W studs because the Cu liner might not be as much of a flux-divergence site for electromigration as W has been.

One new reliability concern was introduced. Sematech has observed that for Cu lines with Si₃N₄ as the top diffusion barrier, sometimes the barrier can delaminate. When neighboring lines at minimum separation carry voltages of opposite polarity, the Cu will migrate from the positive line to the negative line and cause line-to-line shorts. A temperature/bias stress was suggested as the best way to activate and accelerate this mechanism. Some discussion on the number of sites to test took place without resolution, and a criterion of from 10-100 pA was suggested. Biasing electromigration extrusion monitors was suggested as a way to accelerate the problem during electromigration stressing. It was also suggested to use an addressable DRAM array with very high leakage sensitivity as a way identify "precursor" sites which would eventually turn into delamination/shorts.

It was also noted that the resistivity of Cu decreases with time after deposition, sometimes as long as a week, and that an anneal was needed to stabilize the metal. This was seen as a complication to electromigration tests, because the resistance drop would hide resistance increases from EM damage. The self annealing of the copper has been found to correlate with grain growth, which means the absorption of grain boundaries. When the initial grain sizes are small, this could mean a substantial increase in Cu film stress, and might generate nucleation sites for stress voiding.

Effects of low-K dielectrics on reliability were addressed. It was noted that low-K materials appear to be more susceptible to cracking and moisture absorption. Indeed, some electromigration data with Cu lines had shown a higher incidence of extrusion fails at higher current densities than would be expected for Al. We discussed whether a higher percentage shift for EM failure would put us at risk for more extrusion shorts, and noted that extrusions usually occur considerably later than high resistance shifts for Al, but that the case might be different for Cu. Although there were no concrete suggestions, it was generally thought that there was a need for additional test structures to evaluate potential

exposures posed by low-K. Materials suppliers were not thought to check the electrical properties of dielectrics, and this was seen as a gap which needed to be filled. The challenges of low-K were viewed as affecting the reliability of interconnects as well.

It was noted that the thermal dissipation of low-K dielectrics was lower than that of conventional SiO₂, and this could lead to complications both in interpretation of test results and in product reliability performance. An example for product was the effect of high current pulses on subsequent electromigration lifetime. This may not be an issue for parts made with conventional SiO₂, but could become a concern if the thermal conductivity of the low-K dielectrics began to degrade significantly.

For dual damascene structures, we discussed where to place taps (sense lines) to be able to detect voiding in vias. There was also discussion about how the variable thickness of the side wall liner in Cu and Al vias would affect the distribution of failure times -- higher sigma, opens? Misalignment, or the lack thereof should also be more important for dual damascened parts, since there is no upper redundant layer for the descending via to contact.

WLR general philosophy was addressed. Fabless companies want a way to check on the reliability of the parts that are being made for them during fabrication. The only way seems to be wafer level testing. However, lifetime projections from wafer level data are not yet universally believed, both due to the high acceleration of wafer-level tests and because of suspected mechanism changes between wafer level and module level tests (e.g., EM incubation time). Also, some failure mechanisms, such as stress voiding, have too small an acceleration factor to be amenable to wafer level testing, other than identifying that voids are already present. The case for Cu may be different. The fabs were supposed to build in reliability through qualified controls, SPC feedback and controlled maintenance, and the wafer level tests would confirm that the controls were working.

Additional issues are that fabs are decreasing the space allocated for test structures in the kerf (scribe lanes), and resources for establishing the correlation between WLR test and package testing is scarce. This would negate the use of the aforementioned DRAM scheme to detect delamination sites in Cu parts as a manufacturing WLR structure. General consensus was that WLR had to be fast (couldn't tie up a prober) and should expose detrimental process changes, such as oxygen contamination in metals, patterning or processing errors, or gross defects. Hence, generally WLR, at least for FSA, means a way to monitor process goodness for changes which affect the reliability of the product.

We finished the second night with the question of how to address Cu grain size effects. How do we relate the grain size and texture to deposition method, line aspect ratio, thickness and annealing history. This question remained unanswered.

Questionnaire:

To meet anticipated requirements over the next 15 years, the U.S. National Technology Roadmap for Semiconductors charts an aggressive path for evolution of current interconnect technology. Insertion of new interconnect materials (Cu as the primary conductor, with refractory metal liners) is already underway, and, to stay on the NTRS timeline, insertion of new dielectric materials will be required in the near future. With interconnect lengths of kilometers per circuit, minimum linewidths shrinking below 100nm, the number of metallization levels moving toward 10, and the use of an interconnect metal which must be fully isolated from the dielectric, enormous reliability challenges must be met during a period of rapid development of new materials and processes. The goals of this discussion group will be to identify areas of greatest concern, and share lessons learned, and anticipated needs.

Specific discussion topics will include:

- Can the same reliability approaches that were used for Al be applied to Cu?
- Is electromigration-induced failure still an issue for Cu-based alloys?
 - ◊ What are the new design rules?
 - ◊ Are new design strategies enabled?
 - ◊ Are existing design strategies still OK?
- How do liners for Cu affect electromigration?
- Are there reliability issues with the liners themselves?
 - ◊ How easy is it to insure that liners are continuous everywhere on a kilometer of interconnect?
 - ◊ Are there wear-out failure mechanisms for liners, such as cracking due to thermal cycling?
 - ◊ How can liner reliability be assessed?
- Are there new processing-related defects arising from Cu-based technologies which lead to reliability issues?
 - ◊ How important is Cu adhesion?
 - ◊ How significant are the differences in Cu deposition techniques?
- What are the implications of dual damascene vias?
 - ◊ Will liner integrity in vias be a problem?
 - ◊ Will aspect ratio uniformity be maintained?
 - ◊ Will stress become an issue?
- How will the mechanical and thermal properties of Low-K dielectrics affect reliability?
- Are there other properties of Cu or Low-K, different from Al and SiO₂, which could bring in unanticipated reliability challenges?

Appendix