October 23-26, 2000

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IEEE/Integrated Reliability Workshop
P.O. Box 308
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PROGRAM ANNOUNCEMENT!

Workshop Experience

You are cordially invited to participate in the 2000 Integrated Reliability Workshop. It provides a unique environment for envisioning, developing, and sharing reliability technology for present and future semiconductor applications. Here you will closely interact with your peers at moderated discussion groups, open poster sessions, technical presentations, and special interest groups. All Workshop activities take place in a relaxed and rustic setting that promotes an atmosphere of interactive learning and knowledge sharing. You should come away from the workshop intellectually refreshed!

'00 Workshop Features:

- ✶ **Keynote**
  - **D. J. DiMaria and J. H. Stathis, IBM**
  - ***Defect Generation and Reliability of Ultra-thin SiO_2 at Low Voltage***
- ✶ **Group Discussions**
  - **WLR Monitoring**
  - **Ultra-Thin Oxides**
  - **Electromigration**
  - **Burn In**
  - **Negative Bias Temperature Instabilities**
- ✶ **Tutorials**
  - **Managing Technology Qualification**
  - **IC Fab Technology/Control**
  - **Ultra-Thin Oxide Reliability for ULSI**
- ✶ **25+ Technical Presentations on:**
  - **Customer Product Reliability Requirements**
  - **Designing-In Reliability**
  - **Reliability Characterisation & Models**
  - **Contributors to Failure**
  - **Wafer Level Reliability**
- ✶ **Two Videos on:**
  - **Oxide Wearout/Breakdown/Reliability**
  - **MEMS Performance & Reliability**
- ✶ **Refereed/Open Poster Sessions**
- ✶ **Special Interest Groups**

Major Technical Themes

Increased performance, reduced cost, shortened design cycles, new markets – these have driven rapid growth and still unprecedented technical innovation in the semiconductor industry. To meet these demands, new materials and processes are continually introduced for use in deep submicron technology necessitating updated and new models for reliability determination. Reflecting these trends, the technical program begins with a challenging keynote by Dr. D. J. DiMaria from IBM, a leading researcher in oxide reliability in the microelectronics industry. His talk is titled *Defect Generation and Reliability of Ultra-thin SiO_2 at Low Voltage*. The technical sessions cover a broad spectrum of topics from Designing-In Reliability where the focus is on design rule limitations, the influence of lithography on reliability and statistical methods to BEOL issues in the Wafer Level Reliability session. Another session, Customer Product Reliability Requirements, addresses the need to provide product-based models and metrics for circuit level reliability assessment. The physical characterization of devices and materials is addressed in four sessions that cover test methods and defect mechanisms in oxides and interconnect materials. These sessions address the importance of thin oxide related reliability aspects such as: quasi breakdown, plasma induced charging, stress induced leakage currents, trap generation and atomic scale defects. Also, device reliability is highlighted for sub half-micron technologies and there are two contributions on negative bias temperature instabilities. This year's Tutorial Program addresses three very important topics in the IC industry, Technology Qualification for a Foundry/Fabless Partnership, Fabrication Technology and Yield Control, and Ultra-Thin Gate Oxides. These tutorials offer our attendees state-of-the-art instruction on topics crucial to understanding the current IC reliability requirements. In addition to these tutorials we are also providing an opportunity to observe two IEEE instructional videos. The first is *Oxide Wearout, Breakdown, and Reliability* by Dr. David Dumin of Clemson University and the second, on one of the newest areas in semiconductor manufacturer, is *MEMS Performance and Reliability* by Paul McWhorter, Samuel L. Miller, and William M. Miller of Sandia Laboratories. This year's Discussion Groups have been tailored to address reliability issues that will enhance understanding of the materials, processes and techniques crucial to research, development and manufacture of IC's. Our topics this year include WLR Monitoring, Burn In, Electromigration, Negative Bias Temperature Instability (NBTI) and a group on Ultra-Thin Oxides, which will be led by our keynote speaker, Dr. Dan DiMaria. The poster sessions will repeat some of the themes that are being highlighted in the presentations and expand on these themes with invited posters on such topics as the physics of compound materials and devices, SPICE models, electromigration test structures and models, instrumentation developments, and mathematical techniques for data analysis. Finally, there will be opportunities to bring your own unique ideas and concerns to the table during the Special Interest Group sessions that are arranged on site to meet the special needs of the participants.

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KEYNOTE

Defect Generation and Reliability of Ultra-thin SiO_2 at Low Voltage—*D.J. DiMaria and J.H. Stathis, IBM, Yorktown Heights, NY*

The microelectronics industry owes its considerable success largely to the existence of the thermal oxide of silicon. However, recently a concern has been raised that the reliability of ulrathin SiO_2 layers may limit the continued scaling of gate oxides less than about 2nm. In this talk we will review the physics of oxide breakdown. Electrons tunneling through the gate oxide generate defects until a critical density is reached and the oxide breaks down. The critical defect density is explained by the formation of a percolation path of defects across the oxide. Only < 1% of the these paths ultimately lead to destructive breakdown, and the microscopic nature of these defects is not known. The rate of defect generation decreases exponentially with supply voltage, below a threshold voltage of about 5V for hot electron induced hydrogen release. However, the tunnel current also increases exponentially with decreasing oxide thickness, leading to a diminishing margin for reliability as device dimensions are scaled.

TUTORIALS

Chair: Douglas R. Menke, Motorola

Managing Technology Qualification in a Foundry/Fabless Partnership—*Raif Hijab, Cirrus Logic*

Tutorial Session #1A Monday, 1:30–3:30 p.m.*(Angora Room)*

This tutorial addresses the qualification requirements of a new foundry technology in the emerging foundry/fabless semiconductor manufacturer model. It describes the key steps involved in assuring that the foundry technolgy meets the minimum performance and reliability needs of the semiconductor manufacturer. This topic is of interest beyond the pure foundry/fabless house community, since many IDMs are contracting out a major portion of their semiconductor wafer manufacture, while many are offering foundry services to absorb any idle capacity they might have. This has highlighted the need for more widely accepted qualification criteria, and a uniform language and format of exchanging qualification data between foundry and customer.

The tutorial will cover discussion of the methodology outlined in the JEDEC/FSA draft procedure "Standard Foundry Process Qualification Guidlines", which has been submitted for JEDEC letter ballot. This includes the minimum set of measurements required to qualify a semiconductor wafer process, applicable standards, responsibilities of foundry and fabless house, and reporting requirements. The tutorial will also address the question of ongoing reliability monitoring, and how it leverages both PCM electrical data and wafer level reliability monitor data.

Integrated Circuit Fabrication Technology and Yield Control—*Ernest Levine, Tom Houghton, and Parth Dave, IBM*

Tutorial Session, 1B *&* 2B, Monday, 1:30–5:45 p.m. (*Old Lodge*)

This tutorial details in a step-by-step fashion (from buying the wafer up to the final interconnect structure made by Cu damascene techniques) how a logic chip is built and what are the associated yield control/metrology steps encountered during fabrication. The basic steps, which are applicable to any state-of-the-art chip facility, will be described in such detail that the attendee will understand the reason for each step, the logic of the sequence used, as well as the systematic and random defects that may be encountered. Additionally, a discussion of an active yield control strategy will be described, including in-line inspection techniques and points, use of CD, overlay, and AFM — both now and in the near in future. Cross sections, top-down defect appearances, etc. at each key step will be used to illustrate the fabrication process and the defects found. Methodologies used to track down root causes of various failure mechanisms will be discused and illustrated.

Ultra-Thin Gate Oxide Reliability for ULSI Applications—*Ernest Y. Wu, IBM Co. Microelectronics Division*

Tutorial Session #2A, Monday, 3:45–5:45 p.m. *(Angora Room)*

The aggressive scaling of gate oxide thickness for high performance and density in microelectronics industry has reached an unprecedented pace. The extraordinary demand of oxide thickness reduction raises serious concerns for oxide reliability. In this tutorial, the current status and future perspectives of ultra-thin gate oxide reliability will be reviewed. Various reliability evaluation measurements and methodologies are critically examined. Breakdown statistics and percolation model are discussed in light of recent finding of thickness-dependent Weibull shape factors. The measurement techniques of Weibull characteristic parameters are discussed. The issues of microscopic and macroscopic oxide thickness uniformity are considered. Their impact on Weibull breakdown characteristics and oxide reliability is addressed in detail. Various projection schemes in terms of voltage vs. field and time-to-breakdown vs. charge-to-breakdown are discussed. Relative importance of breakdown characteristic time and Weibull shape factor is highlighted using a two-dimensional reliability analysis. The current knowledge of voltage and temperature dependence of time (charge)-to-breakdown is reviewed in the framework of several published models. Finally, different breakdown modes (soft vs. hard breakdown) are reviewed with the emphasis on physical origin, post-breakdown conduction properties, and current runaway dynamics. The implications of different breakdown modes for transistor characteristics and circuit operations are discussed. It is concluded that all above aspects should be carefully and thoroughly considered in oxide reliability evaluation and projection.

DISCUSSION GROUPS

Chair: William J. Vigrass, Texas Instruments

The evening discussion group program is regarded as a favorite highlight of the workshop experience. Attendees will have a choice of 4 topics on both Tuesday and Wednesday evening. Topics 4 and 5 will be offered only once on Tuesday and Wednesday, respectively. You are encouraged to bring along data and/or ideas on transparancies for discussion in the discussion group.

1. WLR Monitoring: *Andreas Martin, Infineon Technologies & Eric Snyder, Sandia Technologies*

Wafer Level reliability, or WLR, refers to a category of stresses which are performed by directly applying temperature, voltage, and/or current stress on specially designed test structures, thus quickly providing data on a wide range of reliability issues. Because of their flexible design and use, WLR tests have become pervasive in the Microelectronics Industry, for applications ranging from technology/process development, to the monitoring of manufacturing lines. By and large, the success of WLR has resided in its ability to provide useful data at elevated stress conditions in a very small amount of time (sec to min), compared to package-level testing. In a fast paced, high volume development or production environment, stepping from traditional WLR to fast WLR is easily done. But what exactly is fast WLR, and how can it be useful to you and your boss?

We hope that by participating in this discussion group, you will come away with answers to these, and other questions, such as:

- Advantages/disadvantages of fast WLR.
- Is traditional WLR fast enough?
- How widely is fast WLR used and should you switch?
- Use which physical models for the interpretation of fast WLR data?
- Success stories, etc.

2. Ultra-Thin Oxides: *Daniel DiMaria, IBM and John Suehle, National Institute of Standards and Technology*

Recent reports indicate that SiO_2 may be able to be scaled down to 1.6 nm. Characterizing gate oxides in this thickness regime presents new challenges in terms of reliability testing, analysis, and projection. The aggressive scaling of oxide thickness has raised several important questions:

- Is intrinsic reliability being compromised?
- Are the physics of failure different than thicker gate oxides?
- Do we know what we are doing when characterizing ultra-thin films?
- When will high-k films be required?

Some of the issues to be addressed include hard and soft breakdown, acceleration parameters for TDDB, the effect of soft breakdown on circuit performance, physical models for oxide breakdown, and testing techniques. Participants are invited to present any new results or ideas to help clarify or further confuse these issues.

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2000 *International*
INTEGRATED RELIABILITY WORKSHOP
PRELIMINARY PROGRAM

MONDAY, October 23

1:00 – 8:00 p.m. Lodge check-in. Get room assignment (prearranged) & room key, with lodge area map and information. (if physically challenged please notify desk of special needs)

1:00 – 6:00 p.m. Registration: Pick up badges & handout (*Dining Room Lounge*) Discussion Group Assignments; SIG Signup

1:30 – 3:30 p.m. Tutorial Session #1: tutorial A & B in parallel

A: "Managing Technology Qualification in a Foundry/Fabless Partnership"	B: "Integrated Circuit Fabrication Technology & Yield Control, Part 1"

3:30 – 4:00 p.m. Break

4:00 – 6:00 p.m. Tutorial Session #2: tutorial A & B in parallel

A: "Ultra-Thin Oxide Reliability for ULSI Applications"	B: "Integrated Circuit Fabrication Technology & Yield Control, Part 2"

5:45 – 6:15 p.m. Poster Preparation (*Old Lodge*)

6:00 – 7:30 p.m. DINNER, *(Dining Room)* dine with your session chair

7:30 – 7:45 p.m. Introduction of workshop agenda in detail: DG, SIG, Mixer & Posters *(Angora Room)*

7:45 – 8:00 p.m. Discussion Group Assignments/SIG signup (*Dining Room Lounge*); Poster Preparation (*Old Lodge*)

8:00 – 10:30 p.m. Mixer & Poster Session, *(Cathedral Room)*

TUESDAY, October 24

6:30 – 8:00 a.m. BREAKFAST *(Dining Room)*

8:15 – 8:30 a.m. Welcome & Introduction: William Tonti, General Chair & Technical Program Overview: Andreas Martin, Tech. Prog. Chair *(Angora Room)*

8:30 – 9:30 a.m. Keynote: "Defect Generation & Reliability of Ultra-thin SiO_2 at Low Voltage"—D.J. DiMaria & J.H. Stathis., IBM T.J. Watson Res. Ctr

9:30 – 10:00 a.m. Break

10:00 – 11:40 a.m. Session #1: Designing-In Reliability (DIR), Chairs: John Suehle, NIST & Brian Langley, Agilent Technologies

- DIR-1 "Deep-Censoring Method For Early Reliability Assessment", H.A. Schafft, NIST, L.M. Head, Rowan Univ., J.A. Lechner, Consultant, J.P. Gill, & T.D. Sullivan, IBM
- DIR-2 "Analysis & Optimization of Stress Conditions for Gate Oxide Wearout Using Monte Carlo Simulation", R.P. Vollertsen, Infineon Technologies, & A. Strong, IBM
- DIR-3 "Design Rule Limitations Due to Hot Carrier Degradation of NMOS Transistor Under DC Stress", D. Regis, C. Dekeukeleire, W. Vanderbauwhede, A. Demesmaeker, & A. Pergoot, Alcatel Microelectronics
- DIR-4 Withdrawn

11:40 – 12:10 p.m. Group Picture

12:10 – 1:40 p.m. LUNCH, *Dining Room*

1:40 – 3:20 p.m. Session #2 Customer Product Reliability Requirements (CPR), Chairs: Bill Vigrass, TI & Cleston Messick, Fairchild Semiconductor

- CPR-1 "On the Methodology of Assessing Hot-Carrier Reliability of Analog Circuits", H. Le, MIT, W. Jiang, Intel, J.E. Chung, Motorola, P.J. Marcoux, Hewlett Packard
- CPR-2 "Fast-bit-limited Lifetime Modeling of Advanced Floating Gate Non-volatile Memories", A. Scarpa, G. Tao, H. Dijkstra & F. Kuper, Philips Semiconductors
- CPR-3 "Reliability Studies on Sub 100 nm SOI-MNSFETs", S. Mahapatra, V.R. Rao, J. Vasi, Indian Institute of Technology, B. Cheng, Motorola, & J.C.S. Woo, Univ. of CA, Los Angeles
- CPR-4 "Fault-Tolerant Approaches Based on Evolvable Hardware & Using Reconfigurable Electronic Devices", D. Keymeulen, A. Stoica, R. Zebulum & Y. Jin, JPL

3:20 – 4:00 p.m. Break

4:00 – 5:40 p.m. Session #3 Contributors to Failure (CTF), Chairs: Andreas Martin, Infineon Technologies & Nguyen Bui, Parthus Technologies

- CTF-1 "Plasma-Induced-Damage (PID) Free 29Å Nitrided Gate Oxide of 130 nm CMOS Devices for High Performance Microprocessor Manufacturing", G. Klein, H. Nariman, D. Wu, J. Tao, B. Bandyopadhyay, D. Wristers, E. Ibok, M. McBride, J. Tsiang, D.H. Ju, and P. Fang, AMD
- CTF-2 "Quasi-Breakdown in Ultra-thin Oxides: Some Insights on the Physical Mechanisms", S. Bruyere, D. Roy, E. Vincent, STMicroelectronics, & G. Ghibaudo, LPCS/ENSERG
- CTF-3 "Soft Breakdown Model of 20 Å Gate Oxide", C.-Y. Ko, R.Y. Shiue, & J. Yue, TSMC
- CTF-4 "Gate Reliability Comparison of 110 & 100 Substrates", A. Strong, E. Wu, IBM, H. Tews, Infineon Technologies, D. Tibel, IBM, R. Malik, Infineon Technologies, & O. Cain, CDI Corp.

6:00 – 7:30 p.m. DINNER, *Dining Room*

7:30 – 9:00 p.m. Discussion Groups,: Chair: Bill Vigrass, *TI* (90 minute parallel sessions for each topic) Attendees are to participate in one of the four groups:

1. WLR Monitoring: *Andreas Martin, Infineon & Eric Snyder, Sandia Technologies*	2. Ultra-Thin Oxides: *Daniel DiMaria, IBM, & John Suehle, NIST*	3. Electromigration: *Harry Schafft, NIST & Tim Sullivan, IBM*	4. Burn In: *Raif Hijab, Cirrus Logic & Rolf P. Vollertsen, Infineon*

9:00 – 10:30 p.m. Individual SIG Meetings (to be announced at camp)

WEDNESDAY, October 25

6:30 – 8:00 a.m. BREAKFAST *(Dinning Room)*

8:15 – 8:30 a.m. Announcements, *(Angora Room)*

8:30 – 10:10 a.m. Session #4: Reliability Characterisation & Models (RCM), Chairs: Harry A. Schafft, NIST & Murat Okandan, Sandia National Labs

- RCM-1 "Electromigration Testing on Via Line Structures with a SWEAT Method in Comparision to Standard Package Level Tests", A. Zitzelsberger, A. Pietsch, & J. von Hagen, Infineon Technologies
- RCM-2 "Comparison of Isothermal, Constant Current & SWEAT Wafer Level EM Testing Methods", D. Tibel, T. Lee, & T. Sullivan, IBM Microelectronics

	RCM-3	"A Correlation Between Highly Accelerated Wafer Level & Standard Package Level Electromigration Tests on Deep Sub-micron via-line Structures", M. Lepper, R. Bauer, & A.E. Zitzelsberger, Infineon Technologies
	RCM-4	"The Effect of Stress Interruption & Alternating Biased Stress on Ultra-Thin Gate Dielectric Reliability", B. Wang, Univ. of MD, J.S. Suehle, E.M. Vogel, NIST, & J.B. Bernstein, Univ. of MD
10:10– 10:45 a.m.	Break	
10:45 – 12:00 p.m.	Session #5 Wafer Level Reliability (WLR), Chairs: Emmanuel Vincent, STMicroelectronics & Tomasz Brozek, PDF Solutions	
	WLR-1	"Basic BEOL Parameters from Isothermal Wafer Level Electromigration Testing", T.D. Sullivan, T. Lee & D. Tibel, IBM Microelectronics
	WLR-2	"New SWEAT Method for Fast, Accurate & Stable Electromigration Testing on Wafer Level", J. von Hagen, G. Antonin, J. Fazekas, Infineon Technologies, L.M. Head, Rowan Univ., & H.A. Schafft, NIST
	WLR-3	"A Novel Electrical Test to Differentiate Gate-to-Source/Drain Silicide Short from Gate Oxide Short", A. Yassine, K. Wieczorek, K. Olasupo & V. Heinig, AMD
12:00 – 1:30 p.m.	LUNCH, *(Dining Room* — Take out Lunch bags available)	
1:30 – 4:30 p.m.	Open	The afternoon is free for discussion, hiking & other recreation; or for viewing videos shown in parallel: (1) Oxide Wearout/Breakdown/Reliability (*Angora Room*); (2) MEMS Performance and Reliability *(Cathedral Room)*
4:30 – 6:00 p.m.	Mixer & Poster Session, *(Cathedral Room)*	
6:00 – 7:30 p.m.	DINNER, *(Dining Room)*	
7:30 – 9:00 p.m.	Discussion Groups (90 minute parallel sessions for each topic) Attendees are to participate in one of the four groups:	

1. WLR Monitoring:	2. Ultra-Thin Oxides:	3. Electromigration:	4. Neg. Bias Temp. Instabilities:
Andreas Martin, Infineon & Eric Snyder, Sandia Technologies	*Daniel DiMaria, IBM, & John Suehle, NIST*	*Harry Schafft, NIST & Tim Sullivan, IBM*	*Emmanuel Vincent, STMicroelectronics & Brian Langley, Agilent*

9:00 – 10:30 p.m.	Individual SIG Meetings

THURSDAY, October 26

6:30 – 8:00 a.m.	BREAKFAST (*Dining Room*)	
8:15 – 8:30 a.m.	Announcements, *(Angora Room)*	
8:30 – 10:10 a.m.	Session #6: Contributors to Failure (CTF), Chairs: Homi Nariman, AMD, & Prasad Chaparala, National Semiconductor	
	CTF-5	"Threshold Voltage Drift in PMOSFET´s due to NBTI & HCI", P. Chaparala, National Semiconductor, P. Lim, Stanford University, & J. Shibley, National Semiconductor
	CTF-6	"Negative Bias Temperature Instability (NBTI) in Deep Sub-micron p^+-gate pMOSFETs", C.H. Liu, Y.F. Chen, S.K. Fan, M.T. Lee, M.H. Lin, C.H. Chou, W.C. Chang, S.C. Huang, Y.J. Chang, & K.Y. Fu, United Microelectronics Corp.
	CTF-7	"Improving the Accuracy of "Shift & Ratio" Channel Length Extraction Method In Deep Submicron Technology", Q. Ye, Infineon, Y. Li, W.R. Tonti, W. Berry, C. Parks, & R. Mohler, IBM Microelectronics
	CTF-8	"Reliability of Via & Its Diagnosis by E-Beam Probing", W. Xia, M. Villafana, J. Tappan, T. Watson, & M. Campbell, Qualcomm Inc.
10:10 – 10:45 a.m.	Break (checkout at this time if not staying for JEDEC meeting)	
10:45 – 12:00 a.m.	Session #7: Contributors to Failure (CTF), Chairs: John Conley, NASA JPL & Abdullah Yassine, AMD	
	CTF-9	"Modeling Trap Generation Process In Thin Oxides", G. Bersuker, Y. Jeon, G. Gale, J. Guan, & H. Huff, SEMATECH
	CTF-10	"Identification of Atomic Scale Defects Involved in Oxide Leakage Currents", P.M. Lenahan, J.J. Mele, Penn State Univ., S.T. Liu, Honeywell, R.K. Lowry & D. Woodbury, Intersil
	CTF-11	"Stress-Induced Leakage Current Comparison of Giga-bit Scale DRAM Capacitors with OCS (One-Cylinder-Storage) Node", D. Park, H. Ban, S. Jung, H. Yang, & W. Lee, Samsung Electronics
12:00 – 12:30 p.m.	Wrap-Up	
12:30 – 1:30 p.m.	LUNCH, *(Dining Room)* & then the Workshop Ends—Leave the Stanford Sierra Camp unless attending JC14.2	
2:00 p.m.	JEDEC 14.2 Committee on Wafer Level Reliability Meeting	

2000 IRW REGISTRATION FORM (Use also for reserving accommodations to EIA/JEDEC Committee JC14.2 meeting, Oct. 26-27)

(Please type, print or attach business card) *Meeting registration automatically includes a room reservation.*

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Discussion Group Preference (circle one **Tues**; one **Wed**): **Tues:** 1 2 3 4 ; **Wed:** 1 2 3 4

☐ Will need poster boards for poster entitled : _____

Method of Payment: ❑Check: Make checks payable to: **2000 IEEE/IRW**
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REGISTRATION FEES (US$)

IEEE Member _____ **$925*** _____
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** Includes all meals, lodging, Handout, & Final Report. (Mon. eve., Oct. 23–Thur. noon, Oct. 26)*

EXTRA COPIES of Workshop Final Report .....Qty: _____ x **$80** _____
JC-14.2 Mtg. accommodations ... **$160** _____
TOTAL REMITTED $ _____

Cancellation fees: $50 after Sept. 29; full fee after Oct. 13

Send this completed form and payment to:
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TAHOE CASINO EXPRESS: The Tahoe Casino Express **runs from Reno to Tahoe** between 8 a.m. and midnight with departures from Reno at: 8:15 a.m., 9:15, 10:15, 11:15, 12:15 p.m., 1:15, 2:15, 3:15, 5:30, 7:30, 9:30, 10:30 and 12:30 a.m. The Express costs $17 each way ($30 round trip) and tickets can be purchased at the Express counter located in the baggage area in the Reno airport. Travel time is approximately 1½ hours. The Casino Express can be reached at 800-446-6128. The Express **leaves the Horizon Casino at Lake Tahoe and returns to Reno** on the following schedule: 4:10 a.m., 6:10, 8:10, 9:10, 10:10, 11:10, 12:10 p.m., 1:10, 2:10, 3:10, 4:10, 5:10, 7:25, and 10:25 p.m. Tickets may be purchased in the Horizon Casino at the main cashier's cage.

Stanford Sierra Camp offers courtesy transportation for conference attendees from the Horizon Casino between 10 a.m. and 10 p.m. on Registration Day (Monday, Oct. 18). Return trips to the Casino are offered on the last day of the conference only. If you are planning on using the Casino Express, please notify Stanford Sierra Camp (530-541-1244) at least ONE WEEK prior to your arrival date. If you find yourself stranded, please call the camp at the same number. The IRW Arrangements Committee may be able to provide emergency service to and from the casino.

(continued from page 2)

3. ELECTROMIGRATION: *Harry A. Schafft, NIST and Tim Sullivan, IBM Microelectronics*

Focal points for discussion will include the following:

- Observations and issues in Al-based metallization, such as comparison of and/or standardization of structures for qualification purposes, and effects of test structure design on test data.
- EM in Cu metallizations; differences from Al, (e.g., linewidth dependence, deposition method, etc.); failure criteria, possible pitfalls of high-temperature testing.
- Wafer level and package level EM for both Cu and Al; effects of different structures on failure distributions, self-heating, and test algorithm.
- Effects of low-K dielectrics on EM and EM testing.

The intent of the discussion group will be to explore areas of interest to the participants in a casual environment. The moderators will have material to stimulate discussion, but no set agenda will be followed.

4. BURN IN: *Raif Hijab, Cirrus Logic Inc. and Rolf P. Vollertsen, Infineon Technologies*

Burn-In is an integral part of IC productions. It serves to screen weak parts and improve the failure rate during early life. Besides this benefit it is expensive and it might degrade intrinsic properties by the high stress conditions or introduce additional fails due to ESD or handling problems. Considerations on how to reduce Burn-In cost and increase screen efficiency lead to concepts like wafer level Burn-In or IDDQ measurements. However, the success of alternative measures depends on the failure mechanism.

The goal of the discussion group is to sample the experience with Burn-In among the participants, evaluate recent developments and discuss possible strategy changes to address future needs. Discussion topics of interest are:

- How effective is Burn-In in general and for certain failure mechanisms?
- What are the risks of Burn-In and how to limit those?
- Why is the usefulness of Burn-In product dependent?
- How can Burn-In be optimized?
- Do we need Burn-In at all and why?
- How to replace or eliminate Burn-In?
- What are the alternatives and do they work reliably?

5. NBTI: *Emmanuel Vincent, STMicroelectronics & Brian Langley, Agilent Technologies*

Deep-submicron technologies encounter a novel failure mechanism associated to MOS device threshold voltage shift after gate stress under elevated temperature. This phenomenon, so-called (Negative) Bias Temperature Instabilities (NBTI) impacts more likely on P-channel MOS devices and may affect especially the analog block reliability.

Topics to be debated during this discussion group include:

- Underlying physics
- Test methodologies and procedures
- Test structures
- Effects on PMOS vs. NMOS...

SPECIAL INTEREST GROUPS

Chair: William Vigrass,Texas Instruments

The Special Interest Groups (SIGs) program at the Workshop has been very successful in fostering collaborative work on important reliability issues and we look forward to continuing growth and renewal in our SIGs. The formation of SIGs is encouraged as a natural extension of the Discussion Group sessions. Anyone interested in more information on SIGs see http://www.irps.org/irw/sig/.

REFEREED & OPEN POSTER SESSIONS

(Monday & Wednesday Evening)

Chair: Rolf Vollertsen, Infineon Technologies

We have 15 refereed posters! In addition, all attendees have the opportunity to present a poster to communicate and discuss their ideas and newest results on technical projects or issues. Please indicate your intention to bring a poster by reserving a poster display board (32" × 40" or 81 cm × 100 cm) in the space provided on the registration form. Your work should be in Landscape format on 8½ × 11" or A4 paper with a maximum of twelve pages. In addition, you are invited to submit a two-page abstract of your poster presentation for inclusion in the Workshop Final Report. See www.irps.org/irw/poster/ for details and deadlines. This is a great opportunity for you to share your work with your peers. If you are presenting a refereed or invited poster a display board will be reserved for you.

JEDEC 14.2 MEETING. The JEDEC 14.2, Wafer Level Reliability Standards Committee, meeting will be held immediately after the Workshop at the Stanford Sierra Camp on Thursday afternoon and Friday morning. Members, alternates, and guests are welcome. The cost for the accommodations is $160.00, which includes Thursday night dinner and lodging *and* Friday breakfast and lunch. All attendees must leave the camp after lunch on Friday. If you have any questions or if you want to become a member of JC-14.2, please call the JEDEC office at (703) 907-7558 or www.jedec.org or call Mike Dion, JC-14.2 Chair, at (407) 724-7067.

MORE INFORMATION. We expect an exciting workshop again this year. We look forward to your active participation in the many Workshop activities and your valuable contribution to the technical discussions. If you have additional questions, please contact either: the Technical Program Chair, Andreas Martin, by phone, ++49 89 234 45257; fax ...45822; or e-mail: Andreas.Martin@Infineon.com; the Tech. Prog. Vice Chair, Linda Head, by phone 856-256-5335, fax ...5241, email: head@rowan.edu; or the General Chair, William R. Tonti, by phone, 802-769-6561; fax ...6567; or e-mail: wtonti@us.ibm.com. Web site: www.irps.org/irw.

REGISTER NOW!

Complete and send in the enclosed registration form. Please register early. We have sold out in past years. Space at the Camp limits IRW to roughly 120 attendees.

We look forward to seeing you at the Workshop!

Sincerely,

Andreas Martin

Andreas Martin
Technical Program Chair

RESPONSIBILITIES OF ATTENDEES

You are expected to come prepared to participate actively in the discussions and meetings by sharing your experiences, concerns, questions, views, technical information, and test data, as appropriate. Your active involvement in the formal, as well as in the informal meetings and activities, is the key ingredient for maximizing the value of the workshop for you and your fellow attendees.

ACCOMMODATIONS

The Stanford Sierra Camp provides an ideal setting for the workshop. The isolated location and the absence of distractions, such as in-room phones and television sets, encourages extensive interaction among the Workshop attendees. Clusters of 2 and 3 bedroom cabins are nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake. Please note; while each attendee is assigned a bedroom, bathroom facilities within each cabin are shared. All rooms have decks with magnificent views of Fallen Leaf Lake and surrounding Sierra peaks.

- **All participants must stay at the camp during the workshop.**
- **We cannot accommodate spouses or any companions at the camp**.
- **Accommodations are *not* available at the Stanford Camp for any day before or after the workshop.**
- Smoking is permitted outdoors only. Smoking will not be permitted in the sleeping or meeting rooms.
- Arrangements can be made for those with special dietary or physical requirements. Please send your requirements with the registration or call 315-339-3968.
- A message board will be available for incoming calls, (530) 541-1244. There are pay telephones for outgoing calls. There are no telephones in the rooms.

ARRANGEMENTS INFORMATION

The IRW has negotiated special car meeting rates with Hertz, guaranteed one week before through one week after the workshop. When you make reservations use the Hertz meeting CV# 022R0171, and call within the US at 800-654-240, in Canada call 800-269-0600, otherwise call 405-749-4434.

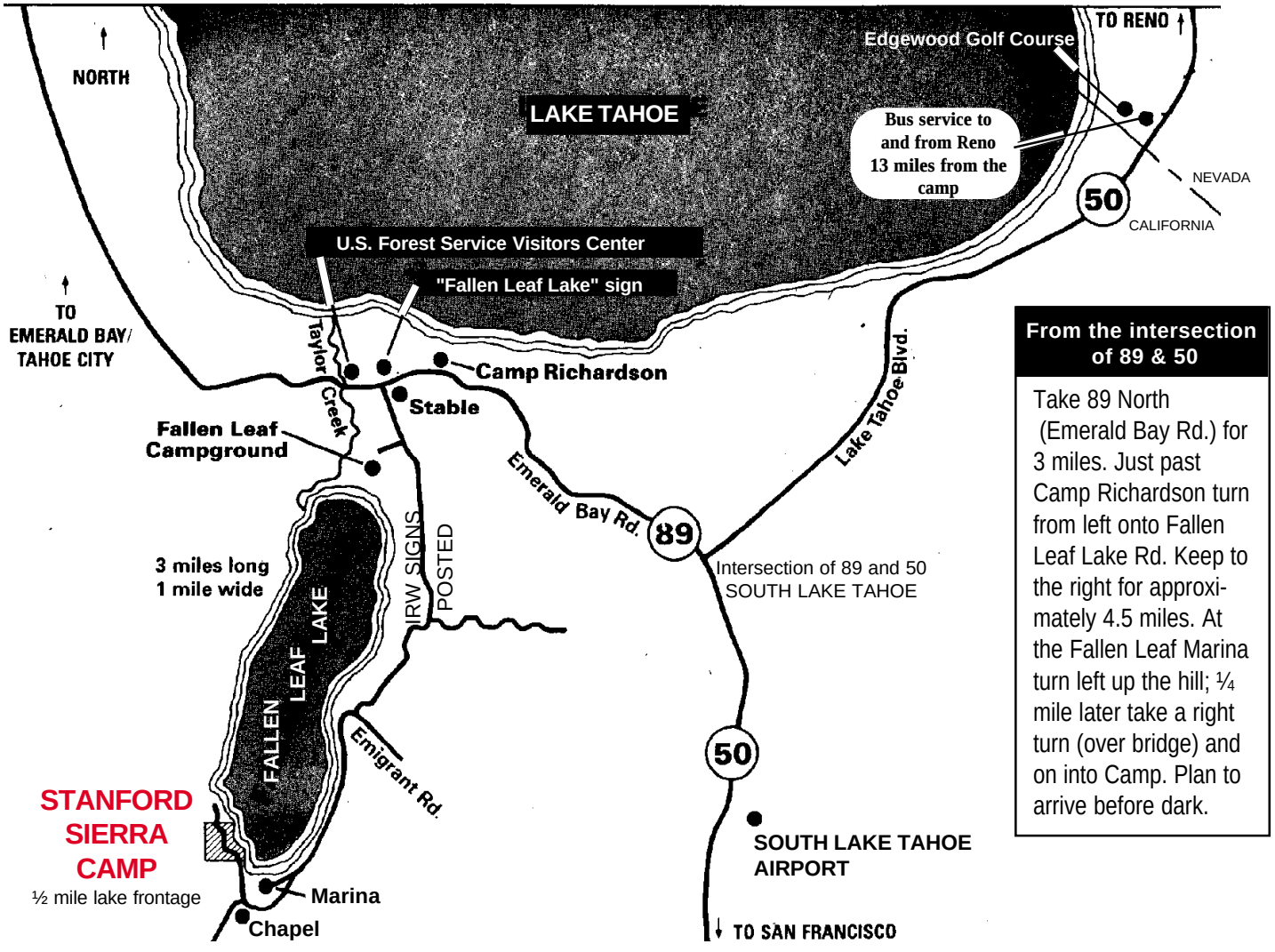
AIR TRAVEL GROUP RATES: The IEEE/EDS has arranged for Group rates with **United Airlines**: 5% off the lowest available fare. Call 1-800-521-4041 to check restrictions and fares. Provide United with the Meeting ID Number: 546XX.

TRANSPORTATION NOTE: The Stanford Sierra Camp is located on Fallen Leaf Lake, a few miles from South Lake Tahoe. The nearest major airport is the Reno International Airport. Reno is approximately two hours from Stanford Sierra Camp. Currently no commercial flights are available to the South Lake Tahoe Airport.

- Transportation is available from Reno International Airport to the South Lake Tahoe terminus at Horizons Casino via the ***Tahoe Casino Express***. For ***Tahoe Casino Express*** schedule details see back of this page or call 800-446-6128.

WHAT TO BRING

It may be cold or warm at 6000 feet in the Sierra in October. We recommend that you bring warm clothing and a coat. Comfortable, informal dress is encouraged. No suits, ties, or high heels please. You may want to bring hiking shoes. There are numerous outstanding hiking trails around the camp. A small flashlight would be helpful to find your cabin after dark.



From the intersection of 89 & 50

Take 89 North (Emerald Bay Rd.) for 3 miles. Just past Camp Richardson turn from left onto Fallen Leaf Lake Rd. Keep to the right for approximately 4.5 miles. At the Fallen Leaf Marina turn left up the hill; ¼ mile later take a right turn (over bridge) and on into Camp. Plan to arrive before dark.