2002 INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM

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APRIL 7 – 11, 2002 • HYATT REGENCY DALLAS • DALLAS, TEXAS

(www.irps.org for updates)

PRELIMINARY PROGRAM

RELIABILITY PHYSICS TUTORIALS: Two days, Sunday and Monday, 8:00 a.m. – 5:00 p.m., April 7-8

Tutorial Tracks (Two registration choices): Reliability Fundamentals, Sunday April 7 and/or Topics in Advanced Reliability, Monday, • April 8
Two sets of Tutorial Notes (See last page of this program or www.irps.org/tutorials.htm for details)
Chair: T.M. Moore, Omniprobe Vice Chairs: C.L. Henderson, Sandia National Labs and C. Hartfield, TI

Sunday, April 7, 7:30 p.m. – 9:30 p.m. — **SER PANEL DISCUSSION WORKSHOP**

Tuesday, April 9, 8:00 a.m. — Plenary Session

SYMPOSIUM OPENING: • General Chair: William R. Tonti, IBM MicroElectronics • Technical Program Chair: Bernie M. Pietrucha, Rowan University
KEYNOTE ADDRESS: Bernard S. Meyerson, IBM Vice President, Communication, Research & Development Center

NON VOLATILE MEMORIES

- Localization of SILC in Flash Memories after Program/Erase Cycling—D. Ielmini et al., Politecnico di Milano/A.S. Spinelli, Università degli Studi dell'Insubria/A. Visconti, STM
- A New Reliability Model for Post-Cycling Charge Retention of Flash Memories—H.P. Belgal/N. Righos/I. Kalastirsky/J. Peterson/R. Shiner/N.R. Mielke, Intel
- Statistical Modeling of the Program/Erase Cycling Acceleration of Low Temperature Data Retention in Floating Gate Nonvolatile Memories—A. Hoefler et al., Motorola
- Physical Description of Anomalous Charge Loss of Floating Gate Based NVMs and Identification of its Dominant Parameter—F. Schuler et al., IMEC
- Cause of Data Retention Loss in Nitride-Based Localized Trapping Storage Flash Memory Cells—W.J. Tsai et al., Macronix/S.H. Gu et al., Nat. Chiao-Tung Univ.
- Empirical Model for Fatigue of PZT Ferroelectric Memories—J. Rodriguez et al., TI/S. Gilbert, Agilent
- DIELECTRICS: ESREF Best Paper (Invited) Failures in Ultrathin Oxides: Stored Energy or Carrier Energy Driven?—S. Bruyere et al., STMicroelectronics/ G. Ghibaudo, LPCS/ENSERG

Tuesday, April 9, 2:00 p.m. — Parallel Sessions

DIELECTRICS I

- A Thorough Investigation of Progressive Breakdown in Ultra-thin Oxides: Physical Understanding and Application for Industrial Reliability Assessment—F. Monsieur/ E. Vincent/D. Roy/S. Bruyere, STM/G. Pananakakis/G. Ghibaudo, LPCS/ENSERG
- Location and Hardness of the Oxide Breakdown in Short Channel n- and p-MOSFETs—F. Crupi, Univ. degli Studi di Messina/B. Kacze et al., IMEC
- Polarity Dependent Oxide Breakdown of NFET Structures for Ultra-Thin Gate Oxide — Is Gate Voltage the Only Controlling Variable for Ultra-Thin Oxide Breakdown?—E. Wu/ W. Lai/M. Khare/L.K. Han/J. McKenna/D. Harmon/A. Strong, IBM
- Gate Oxide Reliability Of Drain-Side Stresses Compared To Gate Stresses—N.A. Dumin/ K. Liu/S.-H. Yang, TI

HOT CARRIERS

- NBT-induced Hot Carrier (HC) Effect: Positive Feedback Mechanism in p-MOSFET's Degradation—H. Aono et al., Hitachi
- A Drain Avalanche Hot Carrier Lifetime Model for n- and p-Channel MOSFET's—N. Koike/ K. Tatsuuma, Matsushita Electric
- Excess Hot-Carrier Currents in SOI MOSFETs and Its Implications—P. Su, UC Berkeley/ K. Goto/T. Sugii, Fujitsu Lab/C. Hu, UC Berkeley
- Effects of Hot-Carrier Stress on the RF Performance of 0.18 µm Technology NMOSFETs and Circuits—S. Naseh/M.J. Deen/O. Marinov, McMaster Univ.
- Hot Carrier Reliability of N-LDMOS Transistor Arrays for Power BiCMOS Applications—D.J. Brisbin/A. Strachan/P. Chaparala/National Semiconductor

MEMS

- (Invited) RF MEMS Switches and Applications—H.S. Newman, Naval Research Lab
- (Invited)Techniques for Reliability Analysis of MEMS RF Switch—J. DeNatale, Rockwell Science Center
- Digital Micromirror Device™(DMD™ Hinge Memory Lifetime Reliability Modeling—A.B. Sontheimer, TI
- Pin-Joint Design Effect on the Reliability of a Polysilicon Microengine—D. Tanner et al., Sandia National Labs

ASSEMBLY/PACKAGING

- (Invited) Product-specific 'Moisture Levels': A Conceptual Framework—R.C. Blish II/S. Sidharth, AMD
- (Invited) Hermeticity Issues in MEMS Packaging—S.J.Jacobs/ J.J. Malone/L.K. Magel/S.A. Miller, TI DLP(Tm) Products
- (Invited) Probing and Wire Bonding of Aluminum Capped Copper Pads—G. Hotchkiss/J. Aronoff/J. Broz/C. Hartfield/R. James/L. Stark/W. Subido/V.Sundararaman/H. Test, TI
- Accelerated Reliability - Thermal & Mechanical Fatigue Solder Joints Methodologies—N.E. Strifas/C. Vaughan, NSWCDD/M. Ruzzene, Catholic Univ.

Tuesday, April 9, 7:00 p.m., Union Station — **RECEPTION & POSTER SESSION**

• **AWARDS PRESENTATIONS,** Eric S. Snyder, 2001 TPC • **RECEPTION SPEAKER:** Jack Kilby, inventor, engineer, & Nobel Prize laureate

DEVICE DIELECTRICS POSTERS

- Stress Induced Leakage Current and Bulk Oxide Trapping: Temperature Evolution—G. Ghidini/ A. Sebastiani/D. Brazzelli, STM
- Atomistic Model For E' Center Generation During Electrical Stress—G. Bersuker, SEMATECH/Anatoli Korkin, Motorola/Yongjoo Jeon/ Howard R. Huff, SEMATECH
- Charging Effects on Reliability of HfO_2 Devices with Polysilicon Gate Electrode—K. Onishi/C. S. Kang/ R. Choi/H.-J. Cho/S. Gopalan/R. Nieh/S. Krishnan/ J.C. Lee, UT Austin
- Modeling Kinetics of Gate Oxide Reliability Using Stretched Exponents—M.S. Krishnan/V. Kol'dyaev, PDF Solutions

DEVICE & PROCESS POSTERS

- Electrothermal Simulation of SiC GTO Thyristor with a Turn-off Snubber in a Clamped Inductive Load Circuit—P.B. Shah, U.S. Army Research Lab
- Temperature Dependence of Ron, sp in Silicon Carbide and GaAs Schottky Diode—J. Luo/ K.J. Chung/H. Huang/J.B. Bernstein, Univ. of MD

HOT CARRIERS POSTERS

- Sub-0.25µm MOSFET Impact Ionization and Photon Generation Dynamics Based on High-resolution Photo-Emission Spectrum Analysis—R.Muniandy, Intel Philippines
- Hot Carrier Reliability of n-MOSFET with Ultra-thin HfO_2 Gate Dielectric and Poly-Si Gate—Q. Lu/ H.Takeuchi/R. Lin/T.-J. King/C. Hu, UC Berkeley/ K. Onishi/R.Choi/C.-S. Kang/J.C. Lee, UT Austin

INTERCONNECTS POSTERS

- Electrical Characterization of Copper Penetration Effects in Silicon Dioxide—J. Cluzel/F. Mondon/ D. Blachier, CEA/LETI/Y. Morand, STM/L. Martel/ G. Reimbold, CEA/LETI
- Electromigration Threshold Length Effect in Dual Damascene Copper Oxide Interconnects—L. Arnaud, CEA-LETI
- Recovery of Open Via after Electromigration in Cu Dual Damascene Interconnect—Y. Sun/P. Zhou/ D.Y. Kim/K.E. Goodson/S.S. Wong, Stanford Univ.

NON VOLATILE MEMORIES POSTERS

- A Complete Study of SILC Effects on EEPROM Reliability—L.Larcher/S. Bertulu/ P. Pavan, Univ. di Modena
- Effects of Fowler Nordheim Tunneling Stress vs. Channel Hot Electron Stress on Data Retention Characteristics of Floating Gate Non-Volatile Memories—M.Suhail/T.Harp/ J. Bridwell/P.J.Kuhn, Motorola

Wednesday, April 10, 8:00 a.m. — Parallel Sessions

ESD & LATCHUP

- Investigation of Gate to Contact Spacing Effect on ESD Robustness of Salicided Deep Submicron Single Finger NMOS Transistors—K.-H. Oh, Stanford Univ./C. Duvvury, TI/ K. Banerjee, Stanford Univ./R.W. Dutton, TI
- Novel ESD Protection Structure with Embedded SCR LDMOS for Smart Power Technology—J.R. Shih, TSMC
- ESD Circuit Simulation for the Prevention of ESD Failures — Application to Products in a 0.18 µm CMOS Technology—H. Wolf/H. Gieser, Fraunhofer Inst. ZM/W. Stadler/ K. Esmark, Infineon
- Electrostatic Discharge Induced Oxide Breakdown Characterization in a 0.1µm CMOS Technology—A. Salman, George Mason Univ./R. Gauthier/E. Wu, IBM/ P. Riess, Infineon/ C. Putnam/M. Muhammad, IBM/M. Woo, OAO Services/D. Ioannou, George Mason Univ.

COMPOUND SEMICONDUCTORS I

- High Current Transmission Line Pulse (TLP) and ESD Characterization of a Silicon Germanium Heterojunction Bipolar Transistor with Carbon Incorporated—B. Ronan, Princetown Univ. /S.H. Voldman et al., IBM
- Wafer Level Forward Current Reliability Analysis of 120GHz Production SiGe HBTs under Accelerated Current Stress—J.-S. Rieh et al., IBM
- Physical Mechanisms of Performance Instabilities such as Gate-Lag and Kink Phenomena in GaAs MESFETs—Y. Mitani et al., Shibaura Inst. of Tech.

FAILURE ANALYSIS

- Recovery of Shifted MOS Parameters Induced by Focused Ion Beam Exposure—K. Chen et al., TI
- Reliability of Ultra Thinning of Flip Chips for Through-Silicon Analyses—E. Le Roy/C.-C. Tsao, Schlumberger/S. Saha/ M.E. Potter, Agere Systems
- Neural Network Classification of Photoemission Spectra— S.J. Frank, TI
- Physical Analysis of Ti-migration in 33Å Gate Oxide Breakdown—K.L. Pey, Nat. Univ. of Singapore/C.H. Tung, Inst. of Microelectronics/W.H. Lin, Chartered Semiconductor Mfg./ M.K. Radhakrishnan, Inst. of Microelectronics

PRODUCT RELIABILITY I

- Soft Error Rate Mitigation Techniques for Modern Microcircuits—D.G. Mavis/P.H. Eaton, Mission Research
- SER Reliability of 1TRAM Designs—D. Sinitsky/S. Peng/ J. Wang/T.C. Ong, TSMC/F.C. Hsu, Mosys/E. Chen, TSMC

Wednesday, April 10, 2:00 p.m.— Parallel Sessions

COMPOUND SEMICONDUCTORS II

- Reliability Test of MESFETs in Presence of Hot Electrons—S. Mil'shtein, Univ. of Mass. Lowell/P. Ersland, M/A-COM/C. Gil, Univ. of Mass. Lowell
- Innovative Nitride Passivation on Pseudomorphic GaAs HEMTs and Its Impact on Device's Performance—Y.-C. Chou et al., TRW/H.K.Kim et al., Bathel Material Research/G.P. Li, UC Irvine
- Evolution of DC and Microwave Degradation Induced by High-Temperature Accelerated Lifetest of Pseudomorphic GaAs and InGaAs/InAlAs/InP HEMT MMICs—Y.-C. Chou et al., TRW

DEVICE & PROCESS

- Impact of Negative Bias Temperature Instability on Digital Circuit Reliability— V.K. Reddy et al., TI
- Leakage Current and Reliability Evaluation of Re-oxidized Nitride and Conventional Oxides—E.Y. Wu et al., IBM/R.-P. Vollertsen, Infineon
- Extending the Reliability Scaling Limit of Gate Dielectrics through Remote Plasma Nitridation of N_2-O-Grown Oxides and NO RTA Treatment—C.H. Liu et al., United Microelectronics
- N-FET HCI Reliability Improvement by Nitrogen Interstialization and its Mechanism—J.R. Shih et al., TSMC
- Mechanism of Device Degradation under AC stress in Low-Temperature Polycrystalline Silicon TFTs—Y. Toyota/T. Shiba/M. Ohkura, Hitachi Ltd.

PRODUCT RELIABILITY II

- Evaluation of STI Degradation Causing DRAM Standby Current Failure in Burn-in Mode Operation Using a Carrier Injection Method—S.-W. Hong et al., Samsung Electronic
- Charge Trapping Induced DRAM Data Retention Time Degradation under Wafer-Level Burn-in Stress—H.W. Seo et al., Samsung Electronic
- A Technique to Predict Gate Oxide Reliability using Fast On-Line Q_{BD} Testing—E. Mullen, Analog Devices/J. Prendergast, Inst. of Technology/C. Leveugle/J. Molyneaux, Analog Devices/J.S. Suehle, NIST

INTERCONNECTS

- (Invited) Investigation of Via-Dominated Multi-Modal Electromigration Failure Distributions in Dual Damascene Cu Interconnects with a Discussion of the Statistical Implications—J.P. Gill/T.D. Sullivan/S. Yankee, IBM/H. Barth/A. von Glasow, Infineon
- Pseudo-Breakdown Events Induced by Biased-Thermal-Stressing of Intra-Level Cu Interconnects–Reliability & Performance Impact—W.S. Song et al., Samsung Electronics
- Stress-Induced Voiding Under Vias Connected To Wide Cu Metal Leads— E. Ogawa et al., TI
- Electromigration Study of Cu/low k Dual-damascene Interconnects— K.D. Lee et al., SEMATECH/P.S. Ho, Univ. of TX
- Electromigration of Cu and Al Using Wafer Level Isothermal Technique— T.C. Lee/D.M. Tibel/T.D. Sullivan, IBM
- Modeling and Analysis of Via Hot Spots and Implications for ULSI Interconnect Reliability—S. Im/K. Banerjee/K.E. Goodson, Stanford Univ.

Wednesday, April 10, 7:30 p.m. — **Workshop Sessions** —
Workshop Chair: S. Krishnan, Texas Instruments, s-krishnan1@ti.com

Workshop	Moderator(s)
• Cu/low-k EM	Paul Ho
• ESD	Charvaka Duvvury & Tim Maloney
• Dielectrics	Paul Nicollian & Eric Vogel
• FA	Larry Wagner
• Product Reliability & Qual	Jay Ondrusek

Workshop	Moderator(s)
• NBTI	Prasad Chaprala & G. LaRosa
• Fast WLR Monitoring for Fab Process	Fred Kuper & Eric Snyder
• Packaging	TBD
• Flash/FRAM	T. San, A. Mihnea, & S. Traynor
• MEMS	Mike Douglass
• Charging	Paul Aum

Thursday, April 11, 8:00 a.m. — Plenary Session

PROCESS INDUCED DAMAGE

- (Invited) Use of NVM based sensors in investigating physical mechanisms responsible for charging damage—W. Lukaszek, Wafer Charging Monitors
- Influence of Plasma Edge Damage on Erase Characteristics of NOR Flash EEPROM using Channel Erase Method—D.-K. Lee/W.H. Lee/Y.-H. Na/K.-S. Kim/ K. O. Ahn/K.-D. Suh, Samsung Electronics/Y. Roh, Sungkyunkwan Univ.
- Enhanced Plasma Charging Damage due to AC Charging Effect—Y. Jin/W.Y. Teo/Y.T. Hou/F.H. Gn/H.F. Lim/Z.Y. Han M.F. Li, Chartered Semiconductor Mfg.
- The Influence of IMD Bake Process on Buried Channel PMOS Hot Carrier Reliability of Advanced DRAM—S.J. Ahn et al., Samsung Electronics
- Impact Of Focused Ion Beam Assisted Front End Processing On n-MOSFET Degradation—A. Lugstein/W. Brezna/E. Bertagnolli, Vienna Univ. of Technology

PANEL DISCUSSION— "Product Qualification in the 21st Century"

Panel: Bob Knoell-Visteon (Automotive user); Nick Lycoudes-Motorola (Automotive supplier); Ted Lach-Lucent (Telecom user); Phil Bechtold-Agere (Telecom supplier)

Thursday, April 11, 1:35 p.m. — Plenary Session

SPECIAL TOPIC—GERMICIDAL IRRADIATION OF THE US MAIL: CAN ICS SURVIVE WHILE BACTERIA PERISH?

Three papers dealing with irradiation of US mail to kill anthrax spores & the survivability of semiconductors at those radiation levels. Check back for updates.

DIELECTRICS II

- Imaging Breakdown Spots in SiO_2 Films and MOS Devices with a Conductive Atomic Force Microscope—M. Porti et al., Univ. Autònoma de Barcelona
- Analysis of Exponential Decay Transient Current in MOS Capacitors—R. Yamada/J. Yugami, Hitachi Ltd.
- Modeling of Substrate Related Extrinsic Oxide Failure Distributions—T. Pompl/M. Kerber/G. Innertsberger/K.-H. Allers/M. Obry/A. Krasemann/D.Temmler, Infineon
- Soft Breakdown Enhanced Hysteresis Effects in Ultra-Thin Oxide SOI nMOSFETs—M.C. Chen et al., Nat. Chiao-Tung Univ./S.H. Lu et al., UMC
- Time-dependent Dielectric Breakdown in poly-Si CVD HfO_2 Gate Stack—S.-J. Lee/C.H. Lee/C.H. Choi/W.P. Bai/Y.H. Kim/D.L. Kwong, UT Austin

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- Foreign Attendees who are not paying by credit card: Please do not remit fee with advance registration form. Advance Foreign Registrants will receive advance registration rates upon arrival. Only U.S. currency will be accepted. Go to Advanced Unpaid Desk upon arrival.
- *Email confirmation* (or post if no email) of Advance Registration by 3/25/02 will be sent. Badge(s), receipt, Proceedings, and CDROM must be picked up at the Symposium Registration Desk during registration hours when you arrive at the Symposium.
- Cancellation fees: $50 after March 22, 2002; Refunds (minus any cancellation fees) honored by written request up to March 28, 2002. No refunds after March 28.
- A set of Basic Reliability Physics Tutorial Notes will be provided for the Basic Topic Tutorials on Sunday and a set of Advanced Reliability Physics Tutorial Notes will be provided for the Advanced Topic Tutorials are included in the respective Tutorial Fee ($260 advance, $300 door).
- Badge for companion (spouse, guest) going to Companion Hospitality Suite available.
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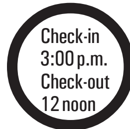

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2002 RELIABILITY PHYSICS EQUIPMENT DEMONSTRATION and Exhibit Program

Exhibits will be open from Monday, April 8 through Thursday, April 11, 2002 and will be open to the public on Tuesday through Thursday

The IEEE - International Reliability Physics Symposium is pleased to announce their annual Equipment Demonstration and Exhibit Program. Exhibits will be open from Monday, April 8, through Thursday, April 11, 2002, and will be open to the public on Tuesday through Thursday.

For more information contact: David Barber, Scien-Tech Associates, Inc., P.O. Box 2097, Banner Elk, North Carolina 28604-2097, U.S.A., P: 1-828-898-6375, F: 1-828-898-6379, Email: dbarbsta@aol.com.

Exhibitors at press time:

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- Hypervision, Inc.
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- Sandia National Laboratories
- Xpeqt AG

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IRPS COMPANIONS' PROGRAM

The IRPS, is again, pleased to offer a Companions' Tour Program. In addition there will be a Hospitality Suite, for spouses and guests of IRPS attendees, open Monday through Thursday, 8:00 a.m. to 10:00 a.m.

For more information on the Companions' Program please contact Sandy Barber, P.O. Box 2098, Banner Elk, NC 28604-2098, or phone 828-898-6375 **(Monday through Friday, 10:00 a.m. to 4:30 p.m. EST),** or send an Email to: sandyirps@aol.com.

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TUTORIAL TRACK: RELIABILITY FUNDAMENTALS

111. Intro Reliability—Tim Rost & Vijay Reddy, TI (8:00 – 11:30)
112. Gate Oxide Reliability—Eric Vogel, NIST (1:30 – 3:00)
113. ESD—Charvaka Duvvury, TI (3:30 – 5:00)
121. Radiation Induced Soft Errors in Silicon Components & Computer Systems—Rob Baumann, TI & Jose Maiz, Intel, et al. (8:00 – 5:00)
131. Errors and Reliability—Kristof Croes & Luc Tielemans (8:00 – 9:30)
132. Failure Analysis—Larry Wagner,Texas Instruments (10:00 – 11:30)
133. New Phenomena in the Device Reliability Physics of Advanced Submicron CMOS Technologies—Giuseppe LaRosa, IBM (1:30 – 5:00)
141. The Basics of Electromigration with a View towards Cu Dual-damascene Reliability—Ennis Ogawa, TI (8:00 – 9:30)
142. WLR—Eric Snyder, Sandia Technologies (10:00 – 11:30)
143. Burn-In—Glenn Shirley, Intel (1:30 – 3:00)

TUTORIAL TRACK: TOPICS IN ADVANCED RELIABILITY

211. Reliability Issues for Advanced IC Technologies—Tony Oates, Agere (8:00 – 11:30)
212. Cu–Based Interconnect Structures—John Sanchez, AMD (1:30 – 3:00)
213. ESD & Radio Frequency—Steven Voldman, IBM (3:30 – 5:00)
221. Gate Oxide Reliability—Paul Nicolian, TI (8:00 – 9:30)
222. Ant. Charging (PID)—Srikanth Krishnan & Anand Krishnan, TI (10:00 – 11:30)
223. Atomic Scale Defects—Pat Lenahan, Penn State (1:30 – 3:00)
224. Trap Generation Phenomena—Gennadi Bersuker, SEMATECH (3:30 – 5:00)
231. MicroRaman—Ingrid DeWolf, IMEC (8:00 – 9:30)
232. Next Generator Imaging—Gay Samuelson, Intel (10:00 – 11:30)
233. MOEMS Reliability—Susanne Arney et al., Lucent (1:30 – 5:00)
241. Analog/MS—Jae-Sung Rieh & Fernando Guarin, IBM (8:00 – 9:30)
242. FRAM—Domokos Hadnagy, Ramtron (10:00 – 11:30)
243. GaAs MMIC Reliability—Ken Decker, Triquint Semiconductor (1:30 – 3:00)
244. HBT—Tim Henderson, Triquint Semiconductor (3:30 – 5:00)

(For the latest tutorial details—see www.irps.org/tutorials.htm)