2001 INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM

FINAL PROGRAM

Monday, • April 30, • 8:00 a.m.–5:00 p.m. — TUTORIALS — Chair: T. Rost, TI

Morning Session (8:00 a.m. - 11:30 a.m.)

1. Errors Made When Performing Reliability Experiments: Discussion, Consequences and Applications—L. Tielemans, DESTIN N.V., and K. Croes, IMO, LUC, *(8:00 a.m. - 11:30 a.m., Scotland)*
2. Silicon Amnesia: A Tutorial on Radiation Induced Soft Errors—R. Baumann, Texas Instruments *(8:00 a.m. - 9:30 a.m., England)*
3. Semiconductor Foundry Qualification–**Panel Discussion**—Panel Members: R. Hijab, Cirrus Logic, Y.J. Chang, UMC, C.-K. Lau, Chartered, A. Preussger, Infineon, and J. Yue, TSMC *(10:00 a.m. - 11:30 a.m., England)*
4. New Phenomena in the Device Reliability Physics of Advanced Submicron CMOS Technologies—G. La Rosa, S. Rauch, and F. Guarin, IBM Microelectronics, *(8:00 a.m. - 11:30 a.m., Great Hall North)*
5. ESD Reliability Physics, Devices and Circuits—S.H. Voldman, IBM *(8:00 a.m. - 11:30 a.m., Ireland)*

Afternoon Session (1:30 p.m. - 5:00 p.m.)

6. Aerosol Spray and the Cooling of Microelectronics—P.J. Boudreaux, Laboratory for Physical Sciences and D.E. Tilton, Isothermal Systems Research, Inc. *(1:30 p.m. - 3:00 p.m., Scotland)*
7. A Chip Designers Perspective on Reliability—D. Overhauser, Simplex *(1:30 p.m. - 3:00 p.m., Ireland)*
8. Thin Gate Oxide Reliability: Degradation, Statistics and Breakdown Modes—J. Suñé, Universitat Autònoma de Barcelona and E. Miranda, Universidad de Buenos Aires *(1:30 p.m. - 3:00 p.m., Great Hall North)*
9. Ferroelectric Material and Device Reliability—T. D. Hadnagy, Ramtron International Inc., *(3:30 p.m. - 5:00 p.m., Scotland)*
10. Microstructure, Processing and Reliability of Cu-Based Interconnect Structures—J. Sanchez, Jr., Advanced Micro Devices *(3:30 p.m. - 5:00 p.m., Great Hall North)*
11. Qualification for Reliability in Time-to-Market Driven Product Creation Processes—W. Gerling, Infineon Technologies AG and F.-W. Wulfert, Motorola SPS *(1:30 p.m. - 5:00 p.m., England)*

Monday, • April 30, • 5:30 p.m.–7:00 p.m. — EQUIPMENT DEMONSTRATIONS PROGRAM RECEPTION—*Exhibit Hall*

Tuesday, May 1, 8:00 a.m. — *Plenary Session—Great Hall North*

SYMPOSIUM OPENING • KEYNOTE • PRODUCT RELIABILITY I

Tuesday, May 1, 2:00 p.m.

Parallel Session 2A—Great Hall North

PROCESS & RELIABILITY INTERACTIONS

Parallel Session 2B & 2C — Scotland

MEMS

PACKAGING AND ASSEMBLY

Tuesday, May 1, 6:00 –9:00 p.m—POSTER SESSION AND RECEPTION—*England/Ireland*

Wednesday May 2

Parallel Session 3A & 3B— Great Hall North

OXIDE I

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8:00 3A.1 *(Invited)* Physical and Predictive Models of Ultra Thin Oxide Reliability in CMOS Devices and Circuits—*J.H. Stathis* 132

8:25 3A.2 *(Invited)* Direct Experimental Evidence Linking Silicon Dangling Bond Defects to Oxide Leakage Currents—*P.M. Lenahan,* et al. 150

8:50 3A.3 Nanoscale Observations of the Electrical Conduction of Ultra Thin SiO_2 Films with Conducting Atomic Force Microscopy—*M. Porti,* et al. 156

9:15 3A.4 Softening of Breakdown in Ultra-thin Gate Oxide nMOSFETs at Low Inversion Layer Density—*S. Lombardo, F. Crupi, and J.H. Stathis* 163

9:40 3A.5 Calculating the Error in Long Term Oxide Reliability Estimates—*B.P. Linder, J.H. Stathis, and D.J. Frank* 168

10:05 *Coffee Break*

WLR FOR INTERCONNECTS

10:30 3B.1 Comparison of Isothermal, Constant Current and SWEAT Wafer Level EM Testing Methods—*T.C. Lee,* et al 172

10:55 3B.2 Real Case Study For Isothermal EM Test As A Process Control Methodology—*S.-Y. Lee,* et al., ... 184

11:20 3B.3 Experimental Comparison of Wafer Level Reliability (WLR) and Packaged Electromigration Tests—*C. Ryu,* et al. 189

11:45 3B.4 Comparison of Via/Line Package Level vs. Wafer Level Results—*D. Tibel and T.D. Sullivan* 194

12:10 AWARDS LUNCHEON, *England/Ireland*

Parallel Session 4A & 4B — Great Hall North

PRODUCT RELIABILITY II

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2:00 4A.1 Historical Trend in Alpha-Particle induced Soft Error Rates of the Alpha Microprocessor—*N. Seifert,* et al. 259

2:25 4A.2 A Reliability Methodology for Low Temperature Data Retention in Floating Gate Non-Volatile Memories—*P.J. Kuhn,* et al. 266

2:50 4A.3 High-Performance Chip Reliability from Short-Time-Tests: Statistical Models for Optical Interconnect and HCI/TDDB/NBTI Deep-Submicron Transistor Failures—*A. Haggag,* et al. 271

3:15 4A.4 An Application-Specific Usage Model for Flash Memory Read Disturb Reliability—*T.S. Harp,* et al. 280

3:40 *Coffee Break*

FAILURE ANALYSIS

4:05 4B.1 Case History: Novel FA Techniques Used to Recover EEPROM Data from the Swissair 111 Crash—*R. Haythornthwaite,* et al. 283

4:30 4B.2 Novel Nondestructive and Non-electrical-contact Failure Analysis Technique - Laser-SQUID Microscopy—*K. Nikawa and S. Inoue* 289

4:55 4B.3 Analysis of Via-Void Generation Mechanism for Giga-bit-scale DRAM—*D.H. Kim,* et al. 294

5:20 4B.4 Study of Metal Impurities Behavior due to Difference in Isolation Structure on ULSI Devices—*K. Matsukawa,* et al. 299

5:45 4B.5 High SRAM Standby Current Due to the Printing of Spurious Images—*S.-Y. Tang,* et al. 303

Parallel Session 3C & 3D — Scotland

OPTOELECTRONICS AND COMPOUND SEMICONDUCTORS

page

8:00 3C.1 Accelerated Stressing and Degradation Mechanisms for Si-based Photo-emitters—*A. Chatterjee,* et al. 200

8:25 3C.2 Low-Temperature, High-Current Lifetests on InP-Based HBT's—*B.M. Paine, S. Thomas III, and M.J. Delaney* 206

8:50 3C.3 Degradation Characteristics of AlGaN/GaN High Electron Mobility Transistors—*H. Kim,* et al. 214

ESD/LATCHUP

9:15 3D.1 Characterization And Investigation Of The Interaction Between Hot Electron and Electrostatic Discharge Stresses Using NMOS Devices in 0.13 µm CMOS Technology—*A. Salman,* et al. 219

9:40 3D.2 Non-uniform Bipolar Conduction in Single Finger NMOS Transistors and Implications for Deep Submicron ESD Design—*K.-H. Oh,* et al. 226

10:05 *Coffee Break*

10:30 3D.3 Advanced 2D Latch-up Device Simulation-a Powerful Tool During Development in the Pre-silicon Phase—*S. Bargstädt-Franke and K. Oettinger* 235

10:55 3D.4 An Analysis of Bipolar Breakdown and its Application to the Design of ESD Protection Circuits—*S. Joshi,* et al. 240

11:20 3D.5 Parasitic Bipolar Transistor Model using Generated-Hole-Dependent Base Resistance—*K. Suzuki,* et al. 246

11:45 3D.6 Design and Analysis of New Protection Structures for Smart Power Technology with Controlled Trigger and Holding Voltage—*V. De Heyn,* et al. 253

12:10 AWARDS LUNCHEON, *England/Ireland*

Parallel Session 4C & 4D — Scotland

INTERCONNECTS

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2:00 4C.1 The Impact of Trench Geometry and Processing on the Performance and Reliability of Low Voltage Power UMOSFETs—*S.A. Suliman,* et al. . 308

2:25 4C.2 The Effects of Plasma Induced Damage on Transistor Degradation and the Relationship to Field Programmable Gate Array Performance—*F.E. Pagaduan,* et al. 315

2:50 4C.3 Improvement of MOSFET Subthreshold Leakage Current by its Irradiation with Hydrogen Radicals Generated in Microwave-Excited High-Density Inert Gas Plasma—*Y. Saito,* et al. 319

INTERCONNECT RELIABILITY

3:15 4D.1 Reservoir Modeling for Electromigration Improvement of Metal Systems with Refractory Barriers—*M.J. Dion* 327

3:40 *Coffee Break*

4:05 4D.2 The Quantitative Assessment of Stress-induced Voiding in Process Qualification—*A.H. Fischer and A.E. Zitzelsberger* 334

4:30 4D.3 Statistics of Electromigration Early Failures in Cu/oxide Dual-damascene Interconnects—*E.T. Ogawa,* et al. 341

4:55 4D.4 Trade-off Between Reliability and Post-CMP Defects with Recrystallization Anneal in Copper Damascene Interconnects—*G.B. Alers,* et al. 350

5:20 4D.5 Impact of Low-K Dielectrics and Barrier Metals on TDDB Lifetime of Cu Interconnects—*J. Noguchi,* et al. 355

Wednesday • May 2, • 7:30 p.m.
•WORKSHOPS 1. FIB User's group 2. Dielectric Reliability 3. Hot Carriers 4. Failure Analysis 5. Interconnect/Copper & Low K 6. MEMS 7. Package 8. ESD/Latchup 9. Cooling Microelectronics

Thursday May 3 — *Plenary: Session 5, Panel Discussion, and Session 6— Great Hall North*

OXIDE II

8:00 5.1 Relation Between Breakdown Mode and Breakdown Location in Short Channel NMOSFETs and its Impact on Reliability Specifications—*R. Degraeve,* et al. 360

8:25 5.2 Analytic Modeling of Leakage Current Through Multiple Breakdown Paths in SiO_2 Films—*E. Miranda, and J. Suñé* 367

8:50 5.3 Experimental Study of Gate Voltage Scaling for TDDB under Direct Tunneling Regime—*M. Takayanagi, S. Takagi, and Y. Toyoshima* 380

9:15 5.4 Accurate and Robust Noise-based Trigger Algorithm for Soft Breakdown Detection in Ultra Thin Oxides—*P. Roussel,* et al. 386

9:40 5.5 Soft Breakdown Triggers for Large Area Capacitors Under Constant Voltage Stress—*J. Schmitz, H.J. Kretschmann, H.P. Tuinhout, and P.H. Woerlee* 393

10:05 *Coffee Break*

10:20 **IS BURN-IN ELIMINATION POSSIBLE?** *Panel*: Carl Peridier, Agere Systems, Andy Forcier, IBM Microelectronics, Bob Knoell, Visteon, Bharath Rajagopalan, Texas Instruments, *MODERATOR:* William R. Tonti, IBM Microelectronics

HOT CARRIERS

page

2:00 6.1 Role of E-E Scattering in the Enhancement of Channel Hot Carrier Degradation of Deep Sub-Micron NMOSFETs at high V_{GS} Conditions—*S.E. Rauch III,* et al. 399

2:25 6.2 Analysis of New Hot Carrier Degradation Phenomena: "W" or "S" Shape Evolution of LDD NMOSFET—*J.-R. Shih,* et al. 406

2:50 6.3 On the Dominant Interface Trap Generation Process During Hot-Carrier Stressing—*D.S. Ang and C.H. Ling,* 412

3:15 6.4 A New Physical and Quantitative Width Dependent Hot Carrier Model for Shallow-Trench-Isolated —CMOS Devices—*S.S. Chung,* et al. 419

3:40 6.5 Hot-Carrier Reliability of P-MOSFET with Ultra-Thin Silicon Nitride Gate Dielectric—*I. Polishchuk, Y.-C. Yeo, Q. Lu, T.-J. King, and C. Hu* 425

4:05 Symposium Closing Ceremony—A.S. Oates //W.R. Tonti

Don't forget to Vote for Best Paper & Pick up a Momento!