Monday, April 30, 8:00 a.m.–5:00 p.m. — TUTORIALS — Chair: T. Rost, TI

Morning Session (8:00 a.m. - 11:30 a.m.)

1. Errors Made When Performing Reliability Experiments: Discussion, Consequences and Applications—L. Tielmans, DESTIN N.V., and K. Croes, IMO, LUC, (8:00 a.m. - 11:30 a.m., Scotland)
2. Silicon Amnesia: A Tutorial on Radiation Induced Soft Errors—R. Baumann, Texas Instruments (8:00 a.m. - 9:30 a.m., England)
4. New Phenomena in the Device Reliability Physics of Advanced Submicron CMOS Technologies—G. La Rosa, S. Rauch, and F. Guarin, IBM Microelectronics, (8:00 a.m. - 11:30 a.m., Great Hall North)
5. ESD Reliability Physics, Devices and Circuits—S.H. Voldman, IBM (8:00 a.m. - 11:30 a.m., Ireland)

Afternoon Session (1:30 p.m. - 5:00 p.m.)

6. Aerosol Spray and the Cooling of Microelectronics—P.J. Boudreaux, Laboratory for Physical Sciences and D.E. Tilton, Isothermal Systems Research Inc. (1:30 p.m. - 3:00 p.m., Scotland)
7. A Chip Designers Perspective on Reliability—D. Overhauser, Simplex (1:30 p.m. - 3:00 p.m., Ireland)
8. Thin Gate Oxide Reliability: Degradation, Statistics and Breakdown Modes—J. Suñé, Universitat Autònoma de Barcelona and E. Miranda, Universidad de Buenos Aires (1:30 p.m. - 3:00 p.m., Great Hall North)
9. Ferroelectric Material and Device Reliability—T. D. Hadnagy, Ramtron International Inc., (3:30 p.m. - 5:00 p.m., Scotland)
10. Microstructure, Processing and Reliability of Cu-Based Interconnect Structures—J. Sanchez Jr., Advanced Micro Devices (3:30 p.m. - 5:00 p.m., Great Hall North)
11. Qualification for Reliability in Time-to-Market Driven Product Creation Processes—W. Gerling, Infineon Technologies AG and F.-W. Wulfert, Motorola SPS (1:30 p.m. - 5:00 p.m., England)

Tuesday, May 1, 8:00 a.m. — Plenary Session—Great Hall North

SYMPOSIUM OPENING • KEYNOTE • PRODUCT RELIABILITY I

8:00 SYMPOSIUM OPENING—General Chair: A.S. Oates and Technical Program Chair: E.S. Snyder
8:20 KEYNOTE: Integrated Communications Microsystems—Mark Pinto, Chief Technical Officer, Agere Systems (formerly the Microelectronics Div. of Lucent Technologies)
9:30 1.2 A New Method for Predicting Distribution of DRAM Retention Time—Y. Mori, R. Yamada, S. Kamohara, M. Moniwa, K. Ohyu, and T. Yamanaka
9:40 Coffee Break
10:05 1.3 Is Product Screen Enough to Guarantee Low Failure Rate for the Customer?—M.W. Ruprecht, G. La Rosa, and R.G. Filippi
10:30 1.4 Analysis of Erratic Bits in FLASH Memories—A. Chimenton, P. Pellati, and P. Olivo
11:20 1.6 Yield Enhancement and Yield Management of Silicon Foundries using Iddq “Stress Current Signature”—M. Rubin, D. Leary, and S. Natan
11:45 1.7 Applying Dynamic Voltage Stressing to Reduce Early Failure Rate—C.-Y. Tsao, et al.

Tuesday, May 1, 2:00 p.m.

Parallel Session 2A—Great Hall North

PROCESS & RELIABILITY INTERACTIONS

2:00 2A.1 A Study of Formation and Failure Mechanism of CMP Scratch Induced Defects on ILD in a W-damascene interconnect SRAM Cell—S.-M. Jung, et al. ................................. 42
2:25 2A.2 The Effects of STI Process Parameters on the Integrity of Dual Gate Oxides—H. Lim, et al. .......................................................... 48
2:50 2A.3 Improvement in Retention Reliability of SONOS Nonvolatile Memory Devices by Two-step High Temperature Deuterium Anneals—J. Bu and M.H. White, ................................................................. 52
3:15 2A.4 Data Retention Failure in NOR Flash Memory Cells—W.H. Lee, et al. .......................................................... 57
3:40 Coffee Break
4:05 2A.5 A New Conduction Mechanism for the Anomalous Cells in Thin Oxides Flash EEPROMs—A. Modelli, et al. ............................... 61
4:30 2A.6 N-Channel Versus P-Channel Flash EEPROM—Which One has Better Reliabilities—S.S. Chung, et al. .......................................................... 67

MEMS

2:00 2B.1 Reliability of a MEMS Torsional Ratcheting Actuator—D.M. Tanner, et al. ........................................................................ 81
2:25 2B.2 Full Three-Dimensional Motion Characterization of a Gimbaled Electrostatic Microactuator—C. Rembe, et al. ................................................................. 91
3:40 Coffee Break

PACKAGING AND ASSEMBLY

4:30 2C.2 Improving Corrosion-Resistance of Silicon-Glass Micropackages Using Boron Doping and/or Self-Induced Galvanic Bias—B.H. Stark, M.R. Dokmeci, T.J. Harpster, and K. Najafi ................................................. 112
4:55 2C.3 A Fatigue Theory for Solders—S. Wen and L.M. Keer .................................. 120
5:20 2C.4 The Concept of Relative Damage Stress and Its Application to Electronic Packaging Solder Joint Reliability—X. Ma, Y. Qian, and X. Zhang, et al. 128

Tuesday, May 1, 6:00 –9:00 p.m.—POSTER SESSION AND RECEPTION—England/Ireland
parallel session 3a & 3b — great hall north

product reliability ii

2:00 4a.1 historical trend in alpha-particle induced soft error rates of the alpha microprocessor — n. seifert, et al. .................................................. 259
2:25 4a.2 a reliability methodology for low temperature data retention in floating gate non-volatile memories — p.j. kuhn, et al. ......................................... 266
2:50 4a.3 high-performance chip reliability from short-time tests: statistical models for optical interconnect and hci/tddb/nbt1 sub-micron transistor failures — a. hagagg, et al. .............................................................. 271
3:15 4a.4 an application-specific usage model for flash memory read disturb reliability — t.s. harp, et al. .............................................................. 290
3:40 coffee break

failure analysis

4:05 4b.1 case history: novel fa techniques used to recover eeprom data from the swissair 111 crash — r. haythornthwaite, et al. ........................................ 283
4:30 4b.2 combined non-destructive and non-electrical-contact failure analysis technique — laser-squid microscopy — k. nikawa and s. inoue .... 289
4:55 4b.3 analysis of via/void generation mechanism for giga-bit-scale dram — d.h. kim, et al. .............................................................. 294
5:20 4b.4 study of metal impurities behavior due to difference in isolation structure on ulsi devices — k. matsukawa, et al. ........................................ 299
5:45 4b.5 high-sram standby current due to the printing of spurious images — s.-y. tang, et al. .............................................................. 303

Wednesday may 2

workshops


parallel session 3c & 3d — scotland

optoelectronics and compound semiconductors

8:00 3c.1 accelerated stressing and degradation mechanisms for si-based photo-emitters — a. chatterjee, et al. .................................................. 200
8:25 3c.2 low-temperature, high-current lifetimes on n-p-based hbt’s — b.m. paine, s. thomas iii, and m.j. delaney ........................................ 206
8:50 3c.3 degradation characteristics of alga/n-ga n high electron mobility transistors — h. kim, et al. .................................................. 214

esd/latchup

9:15 3d.1 characterization and investigation of the interaction between hot electron and electrostatic discharge stresses using nmos devices in 0.13 μm cmos technology — a. salman, et al. .................................................. 219
9:40 3d.2 non-uniform bipolar conduction in single finger nmos transistors and implications for deep submicron esd design — k.-h. oh, et al. .................. 226
10:05 coffee break
10:30 3d.3 advanced 2d latch-up device simulation-a powerful tool during development in the pre-silicon phase — s. bargstadt-franke and k. oettinger .......................................................... 235
10:55 3d.4 an analysis of bipolar breakdown and its application to the design of esd protection circuits — s. joshi, et al. ........................................ 240
11:20 3d.5 parasitic bipolar transistor modeling using generated-hole-dependent base resistance — k. suzuki, et al. ........................................ 246
11:45 3d.6 design and analysis of new protection structures for smart power technology with controlled trigger and holding voltage — v. de heyn, et al. .................................................. 253

awards luncheon, england/ireland

parallel session 4a & 4b — great hall north

product reliability ii

2:00 4a.1 historical trend in alpha-particle induced soft error rates of the alpha microprocessor — n. seifert, et al. .................................................. 259
2:25 4a.2 a reliability methodology for low temperature data retention in floating gate non-volatile memories — p.j. kuhn, et al. ......................................... 266
2:50 4a.3 high-performance chip reliability from short-time tests: statistical models for optical interconnect and hci/tddb/nbt1 sub-micron transistor failures — a. hagagg, et al. .............................................................. 271
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4:05 4b.1 case history: novel fa techniques used to recover eeprom data from the swissair 111 crash — r. haythornthwaite, et al. ........................................ 283
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5:20 4b.4 study of metal impurities behavior due to difference in isolation structure on ulsi devices — k. matsukawa, et al. ........................................ 299
5:45 4b.5 high-sram standby current due to the printing of spurious images — s.-y. tang, et al. .............................................................. 303

Thursday may 3 — plenary: session 5, panel discussion, and session 6— great hall north

oxide ii

8:00 5.1 relation between breakdown mode and breakdown location in short channel nmosfets and its impact on reliability specifications — r. degraeve, et al. .................................................. 360
8:25 5.2 analytic modeling of leakage current through multiple breakdown paths in si-o2 films — e. miranda, and j. suñé 366
8:50 5.3 experimental study of gate voltage scaling for tddb under direct tunneling regime — m. takayang, s. takagi, and y. toyoshima .................................................. 380
9:15 5.4 accurate and robust noise-based trigger algorithm for soft breakdown detection in ultra thin oxides — p. roussel, et al. ........................................ 386
9:40 5.5 soft breakdown triggers for large area capacitors under constant voltage stress — j. schmitz, h.j. kretschmann, h.p. tuinhout, and p.h. woerlee .................................................. 393
10:05 coffee break
10:20 is burn-in elimination possible? panel: carl peridier, agere systems, andy forcier, ibm microelectronics, bob knoell, visteon, bharath rajagopalan, texas instruments, moderator: william r. tonti, ibm microelectronics

hot carriers

2:00 6.1 role of e-e scattering in the enhancement of channel hot carrier degradation of deep sub-micron nmosfets at high vgs conditions — s.e. rauch iii, et al. .................................................. 399
2:25 6.2 analysis of new hot carrier degradation phenomena: “w” or “s” shape evolution of ldd nmosfet — j.-r. shih, et al. .................................................. 406
2:50 6.3 on the dominant interface trap generation process during hot-carrier stressing — d.s. ang and c.h. ling 412
3:15 6.4 a new physical and quantitative width dependent hot carrier model for shallow-trench-isolated — cmos devices — s.s. chung, et al. .................................................. 419
3:40 6.5 hot-carrier reliability of p-nmosfet with ultra-thin silicon nitride gate dielectric — i. polischuk, y.-c. yeo, q. lu, t.-j. king, and c. hu 425
4:05 symposium closing ceremony — a.s. oates /w.r. tonti