IEEE

2001

INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM

http://www.irps.org/

APRIL 30-May 3, 2001

WYNDHAM PALACE RESORT & SPA
1900 Buena Vista Drive
Lake Buena Vista, FL

TELEPHONE: 407-827-2727

FAX: 407-827-3472

Sponsored by

the IEEE Electron Devices Society
and
the IEEE Reliability Society

HIGHLIGHTS* FOR 2001:

Tutorials	Monday	8:00 a.m.-5:00 p.m.
Equipment Demos	Mon.-Thurs.	by Appointment*
Demo Prog. Reception	Monday	5:30 p.m.-7:00 p.m.
Technical Program	Tuesday	8:00 a.m.-5:45 p.m.
Posters & Reception	Tuesday	6:00-9:00 p.m.
Technical Program	Wednesday	8:00 a.m.-5:45 p.m.
Awards Luncheon	Wednesday	12:10 p.m.
Workshops	Wednesday	7:30 p.m.-9:30 p.m.
Technical Program**	Thursday	8:00 a.m.-4:30 p.m.
**Panel Discussion	Thursday	10:30 a.m.-noon

*Read about details in this program

GENERAL INFORMATION

ADVANCE INFORMATION—Avoid delays and extra expense by registering in advance using the form in the center of this program. Mail it with a check or register via fax (315-336-9134) or on-line at www.irps.org/ with a credit card. Advance registration fees apply only to remittances postmarked on or before April 13, 2001. Written cancellation requests will be honored up to April 13, 2001.

SYMPOSIUM REGISTRATION FEES*

	IEEE Member	Non-Member
Advance Registration	$300	$350
Registration at Symposium	$350	$400

TUTORIAL ATTENDANCE FEES**

Advance Tutorial Fee	$250
Door Tutorial Fee	$290

Apply for IEEE membership at ieee.org/join.html. At the Symposium membership application forms will be available near the registration desk also. For additional registration information, see the card in the center of this program or at www.irps.org/.

*Includes copy of Symposium Proceedings (hard copy & cd), workshop attendance, and luncheon ticket. Additional luncheon tickets may be purchased in advance or on arrival at a cost of $25 per ticket.

** Tutorial fee includes a bound set of notes with a cd for all tutorials (including the ones you don't attend). Please register in advance and indicate tutorial selection on your advance registration form so that appropriate room arrangements can be made for each tutorial subject.

REGISTRATION HOURS

The registration desk will be open at the following times:

Sunday, April 29	3:00 p.m.-9:00 p.m.
Monday, April 30	7:00 a.m.-8:00 p.m.
Tuesday, May 1	7:00 a.m.-2:00 p.m.
Wednesday, May 2	8:00 a.m.-2:00 p.m.
Thursday, May 3	8:00 a.m.-2:00 p.m.

HOTEL RESERVATIONS

Attendees will make their own reservations using the form in the center of this program. Note that a one-night deposit or a credit-card guarantee is required with your room reservation. Early reservations are strongly recommended.

The Wyndham Palace must receive your reservation by ***March 28, 2001*** to get the special single/double rate of $145 for accommodations. When making reservations, refer to "IEEE/IRPS–Group 2478".

SYMPOSIUM PROCEEDINGS (hard copy and cd)

The Proceedings will be provided at the Symposium. Additional copies of the Proceedings can be ordered/purchased from: (1) IRPS Registration using the registration form via on-line, fax, or mail; (2) IRPS Registration at the Symposium; (3) IEEE after May 6 via mail order through the IEEE Service Center, Single Copy Sales Unit, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331. For IEEE Service Center credit card/cash sales call 800-678-IEEE. Request IEEE Catalog No. 01CH37167. A substantial discount will be allowed IEEE members.

PAST PROCEEDINGS/TUTORIALS/VIDEOTAPES—A limited number of past proceedings, past tutorial notes, and previous years' videotape sets will be sold in the Past Publications Booth. The booth will be open during regular registration hours.

VIDEOTAPES—Orders are being taken for a five volume videotape set of the 2001 paper presentations. Order using the registration form via on-line, fax, mail, or at the Symposium. Please order by May 14.

General Chair's Welcome

Anthony S. Oates
General Chair

On behalf of the IRPS management committee, I'd like to welcome you to this year's symposium at the Wyndham Palace Resort in Walt Disney World, Orlando. We are looking forward to a very exciting symposium, featuring the very best in the microelectronics reliability field. This year's meeting will feature an extremely strong technical program, a large range of stimulating tutorials, informal workshops on topics of interest, and an equipment demonstration program where hands-on evaluations are welcomed.

The location of the meeting in Disney World, Orlando, with its proximity to many entertainment options, has prompted us to change the format of some aspects of the conference. These changes emphasize the meeting's technical content while permitting time to enjoy the locale. A new emphasis throughout the conference will be the topic of product reliability, which represents a strong area of interest to our attendees. A unique feature of the IRPS has been its interactive nature, and this year we have attempted to increase this important aspect of the meeting. We have scheduled two panel discussions featuring industry experts, and a Tuesday evening poster session to review all the papers to be presented at the meeting. We hope these changes increase your enjoyment of the meeting and of the technical material presented.

Our traditional tutorial program will be held on Monday, May 1, prior to the conference. Tutorial topics are organized into introductory, product, circuit and device reliability tracks. The topics presented include reviews of the latest findings in several important reliability fields, together with overviews of several newer specialized areas of interest. Monday's activities end with a hosted reception in the equipment demonstration area at 5:30 p.m. Don't forget to sign-up for equipment demo time at the coffee table displays during the conference to ensure that you see the latest in reliability testing and analysis equipment.

The technical program begins on Tuesday morning. Details of the technical program are presented in the Technical Program Chair's introduction. Following our emphasis on product reliability issues, there are two sessions featuring product reliability papers, and a panel discussion will also be held on Thursday to discuss burn-in elimination strategies.

Our Tuesday evening function this year has a different feel. The event will take place in the hotel from 6 to 9 p.m. and will involve a poster display of all the papers to be presented at the conference. This event is intended to act as a preview of all the material available at the meeting, and to promote interaction between the paper authors and attendees in a relaxed atmosphere. Food and beverages will be provided.

Wednesday will feature an awards' luncheon where we will recognize the best papers presented at the 2000 IRPS. Our popular workshop program will be held on Wednesday evening. This is a great opportunity for informal discussions with colleagues and industry experts. Please register in advance for the workshop of interest to you.

The conference ends with a full day of technical presentations on Thursday, but for those attendees who wish to extend their stay in Orlando, we have arranged for a trip to the Kennedy Space Center on Friday. Attendees can sign up for this trip during the conference. Information for the Space Center tour is available on the IRPS home page. Space is limited so register early. For those attendees who wish to take the opportunity to visit the Disney area theme parks, we have arranged for discounted tickets for conference attendees and their families. These tickets may be purchased directly on-line at https://secure.hes-services.com/WDWTicket/IEEE.asp

We hope that you enjoy the 2001 IRPS and we look forward to seeing you in Orlando.

Tony Oates, General Chair

TECHNICAL PROGRAM CHAIR'S MESSAGE

Eric S. Snyder
Technical
Program Chair

What do you and your company get from attending IRPS?

Access to the latest research and applications in *product reliability* and semiconductor reliability physics. You have come to expect cutting-edge dielectric, interconnect, hot carriers, plasma damage, packaging, failure analysis, MEMS, ESD/latchup and compound semiconductor/optoelectronic papers. This year is no exception. We have 64 peer-reviewed technical papers, a keynote address, and three invited technical papers from all over the world. Our keynote address is "Integrated Communications Microsystems" by Mark Pinto, Chief Technical Officer, Agere Systems (formerly the Microelectronics Div. of Lucent Technologies). And, we have added a *product reliability* focus with 11 state-of-the-art papers on *product reliability* and *yield* issues in logic, DRAM and non-volatile memory products. In addition, we will have a panel discussion with experts on Thursday debating: *"Is Burn-In elimination possible?"* There will also be a panel discussion on Monday during the tutorials on *"Foundry process qualification"*.

On Tuesday night you will have the opportunity to meet all authors in a relaxed environment and discuss their work. Workshops will take place on Wednesday evening. They enhance the Technical Program and provide an opportunity for in-depth discussion in specific topical areas. Please sign up for the workshops using the IRPS web page at http://www.irps.org/ws

Eighty-nine experts in semiconductor reliability from industry, academia, and research laboratories assisted each other in the final set of technical papers that make up this years proceedings. While the Florida election results were confusing at best, the IRPS selections were not! As you can see from the enclosed program, their work is to be applauded. The technical program starts on Tuesday at 8:00am. The first session is plenary and focuses on *product reliability*. In the afternoon we have two tracks of papers: one on process and reliability interactions, the other on MEMs reliability and packaging issues. The process reliability session is comprised of several papers on non-volatile memories (NVM). This is due to the drive toward smart electronics and the expanded use of embedded NVMs which fulfill this void. MEMs continue to be an emerging field as companies attempt to take laboratory innovations into the marketplace. The packaging session includes the *best paper* from the ESREF conference.

On Wednesday morning, there are parallel sessions on oxide breakdown and optoelectronics. Consistent with the ever-pressing dielectric reliability issues we have *invited* two papers on ultra-thin oxide breakdown modeling. These papers include "Defect Generation and Reliability of Ultra-thin Silicon Dioxide at Low Voltage" by J.H. Stathis and D.J. DiMaria and "Identification of Atomic Scale Defects Involved in Oxide Leakage Currents" by P.M. Lenahan et.al. This is followed by parallel sessions on fast wafer level reliability used for interconnects and ESD/Latchup.

Wednesday afternoon will also have parallel sessions on product reliability, failure analysis, process-induced plasma damage and interconnect reliability. The failure analysis session includes the paper "Novel FA Techniques Used to Recover EEPROM Data from the Swissair 111 Crash." Interconnects made of Cu and surrounded by low-k dielectric, which increase chip speed, are the focus of the interconnect reliability session. The plasma damage session has a paper showing the relationship between transistor damage and product reliability.

On Thursday, we revert to plenary sessions. The morning has a very strong session on ultra-thin oxides as the reliability of ultra-thin oxides continues to be an issue for the industry. This is followed by the panel discussion *"Is Burn-In elimination possible?"* The technical program

concludes with a session on hot-carrier-induced degradation of deep submicron transistors.

Highlights of this years *Technical Program* include:

- 64 peer reviewed technical papers at the cutting edge.
- NEW: Extended authors corner on Tuesday night. This will give you the opportunity to have an extended discussion with all the authors in a relaxed information poster format.
- NEW: Product reliability of embedded FLASH memories, advanced DRAMs, and Logic.
- NEW: Panel discussion on industry experts on Thursday: *"Is Burn-in elimination possible."* This supplements our product reliability focus and is a critical issue to the industry (and a value to you). Bring your questions and don't miss this event.
- NEW: 8 Interactive Workshops on *Wednesday* night.
- World-class tutorials on Monday. This is your chance to keep up-to-date or to "ramp-up" your knowledge. There will be 10 tutorials on subjects ranging from ultra-thin gate oxides to a chip-designers perspective on reliability.

So, one may ask How do you, your company, institution or laboratory benefit from the IRPS technical program?

Understandably a researcher, educator, or engineer leaves IRPS with fundamental knowledge and a set of technical contacts enabling one to tackle the ever-increasing challenges of semiconductor reliability.

I look forward to meeting you at the IRPS in Orlando.

Eric S. Snyder, Technical Program Chair

ARRANGEMENTS INFORMATION

Chair: **Phil Bechtold, Agere Systems**

Vice Chair: Matt Von Thun, LSI Logic

LOCATION

The Wyndham Palace Resort & Spa is located directly across from, and within walking distance to, Downtown Disney, inclusive of: the Marketplace, Pleasure Island, Cirque du Soleil, Planet Hollywood, the House of Blues and the AMC Movie Theatre complex.

TRANSPORTATION (see www.irps.org)

Reduced rates have been arranged with Delta Airlines and Budget Rent-A-Car. Please refer to the back of the program for specific details regarding these airfare and rental car arrangements. Ground transportation via Mears Motorcoach from the airport to the Wyndham Palace Resort at Disney World is also available. Daily self-parking at the hotel is available free of charge. Valet parking is available at a nominal fee per night. Since this hotel is a Disney property, all registrants will be issued a Disney Transportation System Bus Pass upon check-in, providing continuous complimentary shuttle transportation between the hotel and all Walt Disney World Theme Parks & Attractions.

CONFERENCE ACTIVITIES

Registration, Equipment Demonstrations, Tutorials and paper presentations constituting the Technical Program will held on the Ground Level of the hotel, in/and/or directly adjacent to the Great Hall. In response to expressed attendee interest level on the Registration Form, Workshops will be scheduled in the meeting rooms on the Lobby Level. Consult the map at the back of this program for directions to each venue. The Demo Sign-up/Coffee Sponsors/Break area will be in the Great Hall East/West/Center on the Ground Level.

COMPANIONS' PROGRAM

The IRPS is once again pleased to offer a Companions' Tour Program. In addition, there will be a Hospitality Suite, for spouses and attendees' guests, open Monday through Thursday, 8:00 a.m. to 10:00 a.m. For detailed information on the Companions' Program please contact Sandy Barber, P.O. Box 2098, Banner Elk, NC 28604-2098, or phone (828) 898-6375 (Monday through Friday, 10:00 a.m. through 4:30 p.m. EST), or send an e-mail to **sandyirps@aol.com.**

SPA and FITNESS SERVICES

Fitness Center features state-of-the-art equipment and professional trainers. Services offered include: cardiovascular workouts, resistance weight training, aqua aerobics, comprehensive fitness evaluations and nutrition consultations. Special spa treatments include massage therapy, body treatments and hydrotherapy treatments. Preferred golf at five Walt Disney World 18-hole championship courses. Complimentary use of three heated pools, Jacuzzi, sauna, three-lighted tennis courts and sand volleyball court.

MONDAY TUTORIAL SESSIONS

Attend one or two of five morning tutorial sessions and one or two of six afternoon tutorial sessions by recognized experts & get the notes (both hard copy & CD) for all eleven sessions – A GREAT DEAL!

MONDAY EVENING DEMONSTRATIONS PROGRAM RECEPTION

Support the equipment demonstrators who support IRPS, by participating in a hosted Reception in the Conference/Exhibition Hall on the Ground Level from 5:30 p.m. to 7:00 p.m. Meet with our vendors to get a sneak preview of each company's wares. Utilize this access to your advantage to sign-up for preferential one-on-one consultation times with each vendor peaking your interest. Light refreshments and a buffet will be provided.

TUESDAY EVENING POSTER SESSION & RECEPTION

The Technical Program Committee will be sponsoring an evening Poster Session of all platform paper presentations at this year's Symposium. You will have the opportunity to meet once again with the authors who presented their work in the Tuesday plenary sessions, as well as an opportunity to preview the papers yet to be presented on Wednesday and Thursday at the Symposium. Come join us from 6:00 p.m. to 9:00 p.m. in the England/Ireland room on the Ground Level at the Wyndham Palace for some light entertainment, refreshments, taco bar and a dessert bar. Attendees are encouraged to bring their families and friends who may be travelling with them on this trip. A good time will be had by all!

WEDNESDAY AFTERNOON SYMPOSIUM LUNCHEON

In a departure from IRPS tradition, awards for 2000 IRPS Best and Outstanding papers will be presented immediately following a noontime Luncheon in the England/Ireland room . Make your way over to the Luncheon after completion of the Wednesday morning Technical Sessions to congratulate our Best and Outstanding Paper award recipients! Registered attendees for the Symposium will received one ticket for admission to the Luncheon. Additional tickets may be purchased at the Registration Desk.

WEDNESDAY EVENING WORKSHOPS

Participate in any one of eight **Wednesday Night Workshops.** See who's moderating/signed-up to attend and send any questions you might pose to stimulate the discussion for posting at our web-site: http://www.irps.org/ws.

DISCOUNTED WALT DISNEY WORLD THEME PARK TICKETS

Save through *advanced purchase* of your Disney PARK HOPPER® Meeting/Convention tickets**.** These tickets are created just for you and are ***not*** available at front gates of the *Theme Parks!* Please refer to the attached flyer that's a part of this Advance Program or browse: https://secure.hes-services.com/WDWTicket/IEEE.asp

Discounted tickets are only available through this special offer. Orders placed on or before March 30, 2001 will be sent via regular mail with a handling fee of $3.00 (allow 2 weeks for delivery). Orders placed after March 30, 2001 will be shipped via Federal Express with a handling fee of $10.00. Orders will only be accepted through April 16, 2001.

KENNEDY SPACE CENTER TRIP

After IRPS concludes, save on a Kennedy Space Center excursion on Friday, May 4, 2001. Tour includes: roundtrip bus transportation from

the Wyndham Palace, a maximum **accessbadge** including admission to the Visitor Complex, the IMAX movie, NASA bus tour of the launch pad sites (approx. 4 hours), and a half hour guided tour through the main visitor complex. Depart from Wyndham Palace at 9:00 a.m., returning 7:00 p.m. Price per adult: $32.00. Price per child (age 3-11): $29.00. Contact Margo Markvoort at Gator Tours: 1 800 537-0917 for more information.

EQUIPMENT DEMONSTRATIONS

Chair: **Tom Moore, Texas Instruments**

Vice Chair: Chris Henderson, Sandia National Labs

The Equipment Demonstration program of the IRPS focuses on providing attendees with an opportunity to learn about reliability software and equipment in a confidential, "hands-on" fashion. Unlike typical trade events, sales pressures are minimized, and manufacturers are prepared to help attendees learn about, and test their latest equipment and software developments. Attendees are strongly encouraged to contact the demonstrators prior to the conference, and to make arrangements to bring their own samples, if desired. The following abstracts provide an overview of the nature of each company's demonstration, along with contact information. The www.irps.org web site will contain the latest information as more demonstrators are added to the program.

Demonstrators and other companies providing a variety of reliability physics products and services are also represented in the coffee break area. There, they will provide information on their products and sign-up sheets for demonstrations. You can sign-up for demonstrations at any time during the conference. This service is included in your registration and you can sign-up for as many demonstrations as you like, on a first-come, first-serve basis. *So there is really no better way to evaluate so many state-of-the-art systems, and to collect so much information on services, latest equipment, and software developments …than to participate in the IRPS Demos!*

Hours for equipment demonstrations are as follows:

Monday*, April 30:	Noon - 5:00 p.m.
Tuesday, May 1:	7:30 a.m. - 5:00 p.m.
Wednesday, May 2:	7:30 a.m. - 5:00 p.m.
Thursday, May 3:	7:30 a.m. – Noon

*There will be a hosted Equipment Demonstration Program Reception for all attendees in the demonstration area located in the exhibit hall from 5:30 p.m – 7:00 p.m. on Monday, April 30.

DEMONSTRATORS (as of January 18)

Demo#1: COPPER AND ALUMINUM RELIABILITY TEST SYSTEMS FOR PACKAGE LEVEL AND CONVENTIONAL WAFER LEVEL TESTING—Aetruim, Inc., John Pollock, jpollock@aetrium.com; Tel: 651-704-1800; www.aetrium.com

Aetrium is a leading supplier with the broadest offering of test handlers, burn-in board loaders, automation modules and other proprietary wafer or package level reliability test equipment used by the global microelectronics industry to assemble, inspect and test integrated circuits, discrete components and other electronic components. For a complete listing of offices and description of products visit our website www.aetrium.com.

Demo#2: COMPLETE PREDICTIVE WAFER LEVEL RELIABILITY SOLUTIONS—Agilent Technologies (A subsidiary of HP), Jay Thomas; jay-thomas@agilent.com, Tel: 408-553-2212; www.agilent.com

Agilent's fast and predictive PDG-WLR is available on the full line of Agilent parametric testers including the NEW ultra-low noise Agilent 4073A Test System. Its 1fA current resolution and as much as 30 times decreased low-current measurement time enable critical reliability measurements for DRAM, low-power, FLASH and other

technologies. The complete PDQ-WLR solution is NOW the choice of major foundries and their customers for developing, qualifying and monitoring their process reliability, and includes a NEW PC-based analysis tool and NEW production-based test software. To ensure ultra-thin oxide thickness and other critical parameters, Agilent introduces NEW 4156C Precision Semiconductor Parameter Analyzer, with revolutionary C-V capabilities.

Demo#3: EMISSION MICROSCOPE SYSTEMS FOR BOTH FRONT AND BACKSIDE IMAGING—Alpha Innotech, Tracy Mettier; tmettier@aicemail.com Tel: 510-483-9620; www.alphainnotech.com

Alpha Innotech provides the world's first true Emission Microscope systems for both front and backside imaging. With a 1.3 million pixel binning camera option and patented vibration coupling technology for high magnification imaging on a test head, analytical probestation or benchtop.

Demo#4: ESD TEST EQUIPMENT—Barth Electronics, Jon Barth; jonbarth@aol.com; Tel: 702-293-1576; www.barthelectronics.com

The new TLP pulse curve tracer test system is an electrical analysis tool to clearly pinpoint the onset of ESD failure. Demonstrations on your IC will clearly demonstrate the I-V characteristics and where damage occurs. Significantly smaller IC transistors next year will require the analysis equipment to identify previously unmeasured electrical characteristics. Measuring and displaying the I-V characteristics and damage levels is the only method to assist designers in rapid improvement of ESD immunity levels.

Demo#5: MATERIAL AND DEVICE CHARACTERIZATION ON THE NANOMETER SCALE—Digital Instruments, Veeco Metrology Group, Marlene Carlyle; marlene@di.com; Tel: 805-967-1400; www.di.com.

Digital Instruments will demonstrate the Dimension™ 3100 scanning probe microscope (SPM) system. DI's SPM's offer a range of applications for investigators of reliability physics. These include electrical modules for: Scanning Capacitance Microscopy (SCM), enabling unprecedented imaging resolution of electron and optical device structure & operation through 2 & 3D dopant metrology. Scanning Spreading Resistance Microscopy (SSRM) enables high sensitivity nanometer resolution mapping of resistivity in semiconductors; Tunneling AFM (TUNA) gives 2D maps of gate oxide thickness & integrity for dielectric characterization. Each of these and other techniques such as Scanning Thermal Microscopy (SThM) & Electric Force Microscopy (EFM) provide unique material and device property characterization and failure analysis on the nanometer scale, without requiring vacuum.

Demo#6: IR LASER BASED EMISSION AND CURRENT/VOLTAGE IMAGING MICROSCOPES—Hamamatsu Photonic Systems, Mary Boyle, Tel: 908-231-1116; www.hamamatsu.com

Hamamatsu will demonstrate our line of IR laser based emission and current/voltage imaging microscopes along with our line of customized IR optics. The µAmos IR-OBIRCH (Infrared Optical Beam Induced Resistance Change) system allows for localization of leakage current paths, line voids, high resistive vias and other defects at wavelengths of 1310 nm and/or 1064 nm. The Phemos-1000 is an IR Scanning Optical Microscope based emission microscope offering superior resolution and sensitivity with OBIRCH, MCT and other imaging abilities.

Demo#7: MERCAD TELLURIDE SENSOR WITH UP TO 100X GREATER DETECTION SENSITIVITY—Hypervision Inc., Dan Hurley; dhurley@hypervisioninc.com; Tel: 510-651-7768; www.hypervisioninc.com

Hypervision will be demonstrating the Picnic Combo Platform (PCP). This system ties a high resolution BEAMS CCD Imager to the

Picnic Mercad Telluride array offering sensitivity up to 100X over CCD systems. A virtual Imaging software package projects the design layout onto optical/emission images providing resolution <0.2 µm.

Demo#8: PROBING SOLUTIONS FOR EMISSION MICROSCOPY AND LOW CURRENT/LOW NOISE TEMPERATURE TESTING—Karl Suss America, Inc., Veronica Miller, vmiller@suss.com; Tel: 802-244-5181 x333; www.suss.com

Karl Suss is recognized around the world as a precision manufacturer of innovative probing solutions relating to emission microscopy, 300mm wafers and low current/low noise temperature testing. On display will be a SUSS PA200 Semi-Automatic Probe System and a SUSS PM8 Manual Probe System with the SUSS MFI Atomic Force Microscope Probe - the world's first AFM that can see, contact and electrically test devices smaller than 0.15 µm. The AFM probe head supports a number of active and passive tip cartridges for both precision DC and high speed applications.

Demo#9: MEASUREMENT TECHNIQUES FOR EXTRACTING LOW-LEVEL PARASITIC INTERCONNECT PARAMETERS—Keithley Instruments, Bill Merkel, bmerkel@keithley.com; Tel: 440-248-0400; www.keithley.com

As the industry continues to shift towards smaller dimensions, the critical speed limiting parameters in a semiconductor product shift from transistors to parasitic interconnect parameters. Extraction of these parasitic parameters requires very low level measurements. Keithley Instruments will demonstrate the measurement techniques for extracting these low-level parameters using a Keithley 4200 desktop Semiconductor Parametric Analyzer and microprobes.

Demo#10: FULL SCALE SCHEMATIC TOOLS PACKAGE FOR FA—Knights Technology, Scott Shen, sshen@knights.com; Tel: 408-528-3880; www.electroglas.com

Merlin's Framework, the industry standard CAD Nav software product, will be shown with its new features, branches, and versions. Among them, a package of full-scale schematic tools is ready for failure analysis. KEDIT and Image Overlay options are helping FA engineers. A PC version of Merlin software is available now. FA Wizard is the on-line documentation for all level of FA people, and its' Web version is available now. LogicMap is the new Fault Localization tool for the logic designs.

Demo#11: BURN-IN TEST SOLUTIONS FOR HIGH-POWER DEVICES—Micro Control Company, Lisa Ott Ray, l.ottray@microcontrol.com; Tel: 612-277-9211; www.microcontrol.com

Micro Control Company will be demonstrating its burn-in test solutions for high-power (150-200W) VLSI devices. Our equipment provides active thermal control to each device under test, allowing heating or cooling to individual devices throughout the burn cycle. Micro Control Company's burn-in equipment can be used for performing accelerated life testing on high-power VLSI devices. Having equipment capable of performing life testing on these high power devices will enable attendees to be more effective working with these devices.

Demo #12: TEST SYSTEMS FOR ELECTROMIGRATION AND TDDB—Micro Instruments Co., Curt Haas: chaas@compuserve.com; Tel: 760-746-2010; www.microinstrument.com

Micro Instrument Company will provide a hands-on demonstration of new testing capabilities in our (NEW) SPC4000 test system for electromigration and TDDB. Our (NEW) CH4000 chamber has capability for both aluminum and copper testing with temperatures in the 70°C to 350°C Range. Coupled with our new high resolution Instrumentation for Electromigration and TDDB, the system provides an ideal test platform. New test software allows our existing and new instrumentation to operate within the same environment. The

flexibility of the DM610 software allows the user to program the voltage for Constant Voltage, SILC, I-V Sweep and Interim measurements. The DM610 instrumentation can also perform TDDB, and some Hot Carrier tests. See our upgraded PE9010A for Hot Carrier testing, and our PE9020A for small-lot, multiple-temperature testing to 250°C.

Demo#13: ACCURATE AND RELIABLE DE-CAP RESULTS—NSC/SESA Inc., Suree Marley, skm@sesa.com; Tel: 408-988-5816; www.sesa.com

The Nippon Scientific Corporation PS101 systems are distributed by SESA, Inc. These systems use nitric acid, sulfuric acid or a combination of both to ensure accurate and reliable de-cap results. Acid mix ratios are user-definable, and the temperature control is ±1°C to ensure consistent de-cap for plastic IC's. The facility requirements are 110/120V power, 60PSI nitrogen source and a fume hood. The system weighs 77 lbs. and has dimensions of 35" W × 14" H × 15" D.

Demo#14: TURN-KEY SEMICONDUCTOR RELIABILITY TEST—QualiTau, Tom Bensing, 408-522-9200 x102: tomb@mail.qualitau.com; www.qualitau.com

QualiTau will exhibit various turn-key semiconductor reliability test solutions for performing electromigration, dielectric breakdown and hot carrier degradation testing for package and wafer level, featuring various plug-in modules and complete analysis software. Featured systems are the MIRA, INFINITY, ACE and Multi-Probe system: In addition to the various test applications available on the MIRA, also featured will be the latest design of our High temperature DUT boards and our new 450°C oven system. The ACE is a pulsed Electromigration system with a dedicated temperature control and a current source for every DUT. The state-of-the-art INFINITY system features capability for package level and wafer level TDDB testing with an independent SMU for each DUT. Massively parallel wafer level testing will be demonstrated on QualiTau's Multi-Probe system.

Demo#15: : THERMAL EMISSION AND PHOTO EMISSION MICROSCOPE TECHNOLOGY—Quantum Focus Instruments Corporation, Sarah Rogalewski, sarah@quantumfocus.com; Tel: 508-896-0049; www.quantumfocus.com

QFI will demonstrate the latest in thermal emission and photo emission microscope technology. QFI's new InfraScope III thermal imaging microscope system, capable of .05 deg. C temperature resolution, true temperature thermal mapping and 50 kHz transient capture will be demonstrated. QFI will also demonstrate the new emmi 2000, backside photo emission microscope, using near infrared HgCdTe (mercury cadmium telluride) focal plane array technology.

Demo#16: WAVEFORM MEASUREMENT RESULTS OBTAINED ON AN OPTICAL PROBING SYSTEM—Schlumberger, Eryn Neidle, eneidle@san-jose.tt.slb.com; Tel: 408-586-6872; www.slb.com

Schlumberger Probe Systems Group introduces the IDS PICA, the first image based timing analysis tool displaying (X, Y, Z) photoemission movie-type of data for Flip Chips. It is the first tool in the industry that does not require any layout expertise to perform precision timing meaasurements for design, debug and failure analysis. The patented PICA technology captures photon emissions from switching transistors with high timing accuracy.

Demo#17: ADVANCED SEM SAMPLE PREPARATION SYSTEM—SELA USA, Inc., Elizabeth Kieu, elizabeth@sela.com; Tel: 408-736-3700; www.sela.com

The MC500 is the only SEM sample preparation technique that does not expose your wafer to artifacts, water, chemicals or contamination, and presents no physical contact to the surface or cross sections. The main advantages include: Cryo Cooling mechanism for ductile or

organic top layers (Cu, low-k, polyamide); produces two mirror image sections that provide two chances for analysis so that you never loose or destroy a target; high accuracy (better than 0.5 µm); automation; and speedy process (from 3 min/sample). Over 150 systems have been installed worldwide.

Demo#18: PHOTON EMISSION MICROSCOPY, DIGITAL IMAGING AND CATHODOLUMINESCENCE—Semicaps, Inc., Harkiran San Dhu, harkiran@semicaps.com; Tel: 408-986-0121; www.semicaps.com

Semicaps offers Photon Emission Microscopy for localizing defects in semiconductor devices, digital imaging systems for digitizing images from SEMs & Optical Microscopes into PC compatible file formats, Cathodoluminescence imaging for semiconductor micro-characterization, and SEM peripherals for enhancing and expanding the capabilities of any make of SEM.

Demo#19: NEW SCANNING MICROSCOPY FEATURES IMPROVE SYSTEM THROUGHPUT AND EASE OF USE—Sonix, Inc., Jamie Breneman, info@sonix.com; Tel: 703-440-0222; www.sonix.com

Sonix will demonstrate the new software and hardware features of the UHR2000 – the Ultra High Resolution Scanning Acoustic Microscope. Sonix' patented Simultaneous Pulse-Echo and Through Transmission (PETT™) minimizes down time and provides for quick defect detection and verification in one scan. The new DPR-500 pulser-receiver offers improved bandwidth, as well as modular architecture providing advanced user control and allowing for easy PETT scans. New software features, based on Windows platforms, offer robust image analysis features including the ability to rotate data, produce JEDEC reports, perform auto analysis and execute advanced adhesive thickness measurements and advanced filtering techniques for removal of periodic noise. Attendees (up to 4 per hour) are invited to bring their IC packages and see them in a different light.

Demo#20: NEW VISUAL ACOUSTICS™ OPERATING SOFTWARE BASED ON TRUE WINDOWS NT OPERATING SYSTEM—Sonoscan, Inc., Brandi Apostolos; bapostolos@sonoscan.com; Tel: 847-437-6400 x237; www.sonoscan.com

Sonoscan is introducing its new series of digital C-SAM ® Acoustic Microscopes designated D24 and D9000. These systems feature faster and more accurate scanning up to the theoretical limit of the speed of sound. Sonoscan offers a complete family of 230 MHz transducers (currently 6 different designs) that are optimized for applications such as the inspection of CSPs, etc. For production speed analysis, take a look at our FACTS2™, Fast Automated C-SAM Tray Scanner System. Services also include testing laboratories and an array of educational courses on improving device reliability using Acoustic Micro Imaging technologies.

Demo #21: CONTACT PROBING SOLUTION FOR IMAGING AND PROBING SUB-0.2 µm GEOMETRIES ON FULL WAFERS—The Micromanipulator Co., Karen Schanhals; kschanhals@micromanipulator.com; Tel: 775-882-2400; www.micromanipulator.com

An integrated system solution will be presented featuring Micromanipulator's 300 mm 9920 semi-automatic analytical test station with NetProbe™ (the next generation in navigation control software). Workshop attendees may select their preferred semiconductor test equipment or combine it with Micromanipulator's 9920 station and probe at resolutions up to 0.05 microns. Then see how easy it is to transfer the position data to tabular and graphical analysis programs for future review. Learn how to probe at very low femtoamp levels (less than 10 fA range) and at elevated temperatures using triaxial probes, triaxial chucks, integrated shielding and unique high-stability probes. New and experienced users will appreciate the practical solutions presented at Micromanipulator's workshop resolving incorrect test setups and common errors which can introduce

unwanted leakage and electrical and/or physical noise. Additionally, work with UV laser light for high resolution passivation removal and visible light for conductor separation on ICs for failure analysis and fault isolation. See the only available contact probing solution for imaging and probing sub-0.2 µm geometries on full wafers.

Demo #22: AUTOMATIC ESD AND LATCHUP TESTERS—Thermo KeyTek, Kim Baltier; kbaltier@keytek.com; Tel: 978-275-0800; www.keytek.com

Thermo KeyTek will demonstrate two testers: (1) The NEW ZapMaster Mk.2, an advanced ESD and latchup system for testing devices up to 768 pins; and (2) RCDM, a Robotic CDM ESD test system. Attendees may also operate the equipment themselves, and time permitting, perform ESD tests on one or two of their own devices. (Prior arrangements should be made to ensure appropriate DUT boards are available.)

ADDITIONAL COFFEE BREAK SPONSORS

- Accurel Systems
- B&G International
- BTA Technology
- Electronic Device Failure Analysis Society (ASM)
- Insight Analytical
- Reedholm
- Sagitta
- Sandia National Labs
- ULTRA TEC
- Viko Test Lab – ADEC

TUTORIAL PROGRAM

Chair: **Tim Rost, Texas Instruments**

Vice Chair: Pankaj Dixit, Sun Microsystems

The 2001 IRPS Tutorials program is designed to maximize attendees exposure to core and emerging reliability topics presented by industry leaders. The tutorials are organized into 4 “tracks” this year – Intro, Product, Circuit, and Device. For those who are new to the field of reliability, the Intro track offers introductory tutorials on topics of general and emerging interest. Product, Circuit, and Device tracks offer the experienced engineer an opportunity to hear new developments, exchange technical viewpoints, and broaden their technical skills in these reliability focus areas.

The topics for 2001 include core presentations in the areas of transistor, gate oxide, and Cu interconnect reliability. These areas are of continuing concern in the reliability community as the semiconductor industry steadily pushes for aggressive technology scaling with new materials. At the circuit level, presentations in the area of ESD protection and design reliability address the challenges of moving reliability “upstream” to the circuit simulation and design phase. This is critical in allowing reliable products to be introduced in a timely fashion. At the product level, new understanding and recent concern related to soft errors (SER) is addressed as well as two tutorials focused on product qualification. The first tutorial on qualification is from a semiconductor foundry perspective in the format of a panel discussion. The second tutorial focuses on qualification as an element of the entire product creation process considering increasing time-to-market pressures that exist today.

The 2001 tutorials also include an “Intro” track. One topic that is common to all areas of semiconductor reliability engineering is the statistical nature of reliability experimentation. This introductory tutorial addresses errors that can creep into reliability experiments and extrapolations, and steps that need to be taken to avoid them. Two other talks in the “Intro” track are on topics of emerging interest. The first addresses the thermal engineering aspect of semiconductor reliability. It is becoming increasingly important to understand how to control the temperature of IC’s as power dissipation for high

performance products continues to climb. The second tutorial on an emerging topic is in the area of ferroelectric reliability. Ferroelectric materials and devices are gaining more widespread use and it is becoming important to understand the unique reliability challenges that are associated with them.

The Tutorials program is a great value for IRPS attendees. It is far more economical than bringing experts to your location. With the registration you will receive a copy of the Tutorials Notes which includes the abstracts and viewgraphs of all the tutorials (over 20 hours of reference material!). To facilitate meeting room planning, you are strongly encouraged to register early and indicate your intended attendance choices on the registration card.

Monday April 30, 2001

Room	8:00 a.m. to 9:30	10:00 to 11:30	1:30 to 3:00	3:30 to 5:00 p.m.
Scotland	Topic 1		Topic 6	Topic 9
England	Topic 2	Topic 3	Topic 7	Topic 10
Ireland	Topic 4		Topic 8	
Great Hall North	Topic 5		Topic 11	

Topic 1. ERRORS MADE WHEN PERFORMING RELIABILITY EXPERIMENTS: DISCUSSION, CONSEQUENCES AND APPLICATIONS—L. Tielemans, DESTIN N.V., Diepenbeek, Belgium and K. Croes, IMO, LUC, Diepenbeek, Belgium *(8:00 a.m. - 11:30 a.m., Scotland)*

One of the main purposes of performing reliability experiments is to obtain information on the lifetime of the tested component or system under normal operating conditions. Of course, when estimating such a lifetime at the very end of a testing period, the obtained estimate is subject to all types of error. The main idea of this tutorial is to present an overview of all the potential errors that can be made on the predicted lifetimes.

Topic 2. SILICON AMNESIA: A TUTORIAL ON RADIATION INDUCED SOFT ERRORS—R. Baumann, Texas Instruments *(8:00 a.m. - 9:30 a.m., England)*

With the advent of multi-megabyte embedded memories and technologies with stratospheric transistor counts doing billions of operations per second, all the while operating at voltages approaching threshold voltages, the once ephemeral soft error is rapidly coalescing into a very real concern for a large variety of customers. In this tutorial we will consider how radiation-induced charge generation, transport, and collection can induce soft error events in memory and in logic circuits. We will examine, in detail, the three different radiation mechanisms responsible for soft errors and how these radiation sources can be quantified. Finally, we will discuss the various methods used to determine the impact of soft errors on product performance and design and process methodologies which can greatly reduce the soft error rate.

Topic 3. SEMICONDUCTOR FOUNDRY QUALIFICATION **PANEL DISCUSSION**— Panel Members: R. Hijab, Cirrus Logic, Y.J. Chang, UMC, C.-K. Lau, Chartered, A. Preussger, Infineon, and J. Yue, TSMC *(10:00 a.m. - 11:30 a.m., England)*

Questions to be addressed:

- How do customers know that designs fabricated in semiconductor foundries are free from wearout issues?
- How do semiconductor foundries handle user defined reliability requirements?
- What changes to the qualification strategy and challenges does the semiconductor foundry business anticipate with regard to the introduction of new materials and processes (i.e. Cu / low-k)?

Topic 4. NEW PHENOMENA IN THE DEVICE RELIABILITY PHYSICS OF ADVANCED SUBMICRON CMOS TECHNOLOGIES—G. La Rosa, S. Rauch, and F. Guarin, IBM Microelectronics, Hopewell Junction, NY*(8:00 a.m. - 11:30 a.m., Ireland)*

This tutorial will give an overview of some of the new reliability phenomena observed in MOSFET devices of advanced submicron CMOS technologies and their impact to reliability lifetime projections. Some focus will be given to Hot Carrier Reliability Phenomena such as e-e scattering, secondary impact ionization as well as parasitic drain series resistance effects in NMOSFET as well as hot hole damage in PMOSFET devices. In addition the role of Negative Bias Temperature Instabilites (NBTI) as technology limiter in the design of PMOSFET submicron devices will be discussed. The impact of these phenomena to DC and AC based circuit lifetime projections as well as methodologies will be given.

Topic 5. ESD RELIABILITY PHYSICS, DEVICES AND CIRCUITS—S.H. Voldman, IBM, Essex Junction, VT*(8:00 a.m. - 11:30 a.m., Great Hall North)*

With technology scaling, introduction of new technology types and growth of RF wireless applications, there continues to be a sustained need for understanding ESD phenomenon, providing new ESD solutions, innovations and inventions. In this tutorial, ESD protection of semiconductor devices in advanced CMOS, BiCMOS, Silicon on Insulator (SOI), Silicon on Sapphire (SOS), Gallium Arsenide, and Silicon Germanium (SiGe) technology as well as new ESD disciplines will be discussed. ESD reliability physics of known physical models of silicon devices and interconnects (e.g., Wunsch-Bell, and Dwyer) will first be reviewed and how they relate to ESD protection and ESD pulse models (e.g., HBM, MM, CDM, TLP and VF-TLP) will be discussed. CMOS MOSFET scaling and technology evolution, with the introduction of shallow trench isolation, cobalt salicide, copper interconnects, low K dielectrics and gate dielectric scaling will be reviewed in light of its implications, impacts, advantages and disadvantages to ESD protection. ESD devices, circuits and techniques will be discussed commonly used in memory, microprocessors, and logic. MOSFET-based (e.g., grounded gate, RC- and substrate-triggered) and diode-based ESD networks, as well as ESD Power Clamps, will be reviewed and compared. New SOI ESD physics, circuits and inventions (e.g. SOI lateral polysilicon diode, dynamic threshold body-coupled ESD) will be discussed. Our focus will then shift to BiCMOS, BiCMOS SiGe, RF-CMOS, RF-SOS and GaAs ESD. Power-to-failure, SOA, the Johnson limit, RF fT fMAX tradeoffs and ESD will be highlighted for Silicon Germanium technology. Additionally, ESD physics in non-silicon applications (e.g. semiconductor masks, and the MR, Giant MR and Tunneling MR devices for disk drive industry) will also be highlighted.

Topic 6. AEROSOL SPRAY AND THE COOLING OF MICROELECTRONICS—P.J. Boudreaux, Laboratory for Physical Sciences, College Park, MD and D.E. Tilton, Isothermal Systems Research, Inc., Clarkston, WA *(1:30 p.m. - 3:00 p.m., Scotland)*

Since the advent of VLSI microelectronics, there has been a steady demand for higher and higher performance with a concomitant heat load. This has placed an increasing burden on the thermal capabilities of microelectronic systems. New technological breakthroughs have greatly alleviated this thermal bottleneck and aerosol spray cooling is one of them. It has unique characteristics to add to the thermal design and control of microelectronics. A new thermal management paradigm is possible that greatly enhances the reliability while reducing the overall system size and weight. This liquid phase change technology allows the designer to minimize the maximum temperatures in a system while simultaneously eliminating most of the temperature gradients across components. Aerosol spray cooling is described along with some example applications, which illustrate the remarkable characteristics of this technology.

Topic 7. A CHIP DESIGNERS PERSPECTIVE ON RELIABILITY—D. Overhauser, Simplex, Sunnyvale, CA *(1:30 p.m. - 3:00 p.m., Ireland)*

As mainstream designs move to 0.18-micron processes and below, and increase both design size and power, more chip designers are making reliability analysis a standard part of their design flow. The quality of the analysis varies significantly between different design teams. More aggressive designs require much more extensive analysis of both the process and the design. This tutorial will provide an overview of the approaches to reliability analysis by various design teams for power grids and signal nets. Various methodologies, process analyses, design analyses, and analysis tools will be discussed.

Topic 8. THIN GATE OXIDE RELIABILITY: DEGRADATION, STATISTICS AND BREAKDOWN MODES—J. Suñé, Universitat Autònoma de Barcelona, Bellaterra, Spain and E. Miranda, Universidad de Buenos Aires, Buenos Aires, Argentina *(1:30 p.m. - 3:00 p.m., Great Hall North)*

The dielectric breakdown of thin gate oxides in MOS devices is reviewed with particular emphasis in three relevant issues: oxide degradation, breakdown statistics, and breakdown modes. If one assumes that oxide breakdown is related to the generation of defects in the oxide bulk, the study of oxide degradation under electrical stress is essential. A critical analysis of the different physical models accounting for oxide degradation is briefly presented. The link between defect generation and breakdown has been established by means of simple statistical considerations. A brief overview of the breakdown statistics including the discussion of various models is included. Particular interest is given to a very simple physics-based analytical picture that shares the main features of the numerical percolation models. In thin oxides, at least two different breakdown modes have been identified, namely Soft Breakdown (SBD) and Hard Breakdown (HBD). Understanding the physics underlying these conduction modes is a major concern because SBD might be tolerated at least for some digital applications. We discuss how these breakdown modes show coincident time-to-breakdown statistics in spite of exhibiting huge differences in the post-breakdown current. The properties of both breakdown modes are explained in the common framework of a model based on quantum point contact conduction. The energy dissipation mechanisms that control the prevalence ratio of SBD and HBD events during the breakdown runaway will also be briefly discussed.

Topic 9. FERROELECTRIC MATERIAL AND DEVICE RELIABILITY—T. D. Hadnagy, Ramtron International Inc., Colorado Springs, CO*(3:30 p.m. - 5:00 p.m.,Scotland)*

The last few years has seen the introduction of ferroelectrics based memories. The materials of choice have been PZT and SBT (Y1). There has been extensive research done in the integration of these materials into standard CMOS processing. This work has revealed many issues associated with the control of ferroelectrics properties. Included in these issues is the necessity of not degrading the ferroelectric device properties, the electroding system and maintaining the CMOS device performance. These issues have had a direct impact on the reliability of the final products produced with a particular process flow. Reviewed will be the current understanding about the issues associated with both of the main materials contenders. In particular, the materials properties will be reviewed as a function of processing conditions and deposition conditions. Materials attributes and how they tie into product reliability and ultimately system requirements will be reviewed. Details associated with the major failure modes of ferroelectric memories will be discussed as well as methods circumventing them. The impact of processing conditions as well as materials choices on reliability will be discussed. Process integration issues are currently at a high level of interest and a number of different

solutions are being pursued to address the issues of materials degradation. These include but are not limited to change of electrode structure, capacitor encapsulation methods, as well as process integration changes. The delivery of products to customers and the implementation of quality control mechanisms often reveal low percentage failure mechanisms that are either materials or process related. Finally the current status of product performance to industry standard reliability tests and future directions will be evaluated with an eye on trends and possible markets.

Topic 10. MICROSTRUCTURE, PROCESSING AND RELIABILITY OF CU-BASED INTERCONNECT STRUCTURES—J. Sanchez, Jr., Advanced Micro Devices, Sunnyvale, CA *(3:30 p.m. - 5:00 p.m., Great Hall North)*

The implementation of Cu-based interconnect structures is the result of the development of novel processing schemes and the learning of new paradigms for structure-processing relationships, as well the application of relevant portions of the existing Al-based interconnect knowledge foundation. As an example, the challenging tight pitch metallization schemes for 130 nm generation technologies and beyond, require novel damascene patterning of Cu-filled trenches filled by bottom-up electroplating. The stringent Cu diffusion barrier and electroplating requirements dictate refractory metal and Cu "seed" layers, however experience learned during Al-based multilayer metallization development may be applied to barrier metal/Cu interconnect process development. In addition, basic materials' properties and processing effects will also determine the mechanisms controlling Cu interconnect reliability, although the degree to which individual mechanisms may vary since typical Cu microstructures and mechanical properties vary from typical Al-based structures. This tutorial will describe the key factors that control Cu interconnect reliability: interconnect microstructure and the dependence on processing schemes; mechanical stresses and the dependence on dielectric constraint and thermal processing; and diffusional mechanisms that determine stress evolution, voiding, delamination and interconnect failure.

Topic 11 QUALIFICATION FOR RELIABILITY IN TIME-TO-MARKET DRIVEN PRODUCT CREATION PROCESSES—W. Gerling, Infineon Technologies AG, Muenchen, Germany and F.-W. Wulfert, Motorola SPS, Muenchen, Germany *(1:30 p.m. - 5:00 p.m., England)*

The penetration of semiconductor products into the variety of application segments together with their economic forces of cost and time-to-market enforce more efficient qualification concepts. This influences the organization of the qualification process in relation to the development / innovation process as well as the choice of qualification methodology. This tutorial will introduce a systematic procedure which makes best use of existing knowledge (existing qualification results) and focuses on the aspects which need to be qualified, and an application specific qualification methodology based on the physics of failure, which is adjustable to the requirements of different application segments. Visual examples will also be provided.

Wednesday, May 2, Workshops #1 to #8: 7:30 p.m. - 9:30 p.m.

WORKSHOPS

Chair: **Shekhar D. Khandekar, Intel**
(shekhar.d.khandekar@intel.com)
Vice Chair: Jennifer K. Mc Daniel, Lucent Bell Labs
(jkmcdaniel@lucent.com)

We have arranged eight workshops for the attendees covering topics in reliability physics. You can register for these workshops for no additional costs, but are requested to show your preference during the

registration in order to manage the logistics. A list of moderators with their contact information will be available on the IRPS website so you can send in your questions or your contribution towards that workshop to the appropriate moderator. Send your requests or post data and questions via the IRPS website at www.irps.org/ws.

Overhead projectors will be available in the meeting rooms. Please note that the workshops will be held on Wednesday evening.

• Workshop 1: **FIB User's Group**

The FIB workshop brings together FIB practitioners to share their experience and those who are new to the field and want to become familiar with the diverse aspects of FIB techniques. Topics to be discussed may include, but are not limited to, the challenges of design for reparability, sample preparation, FIB damage, copper challenges, voltage contrast, CAD layout overlay and repair site navigation on deep submicron ICs. Come and participate in discovering how the FIB is enhancing analysis time. Bring any questions, concerns, successes and challenges!

• Workshop 2: **Dielectric Reliability**

What does the data mean? Planning and execution for dielectric reliability data requires a discipline to ensure timely and meaningful information. It is a labor and time intensive effort in which perhaps, one gets only one chance to make it work and there is never enough time. This workshop will concentrate on these issues as they relate to processing conditions, model for voltage (or field) and temperature, area dependence, process/device layout sensitivities (area vs perimeter, etc.), and DC vs transient conditions. The workshop will address how to plan for dielectric data with the existing constraints, and how to analyze the data for maximum information, and what conclusions or actions you should take based on it.

• Workshop 3: **Hot Carriers**

Hot carriers reliability requirements continue to be an issue of concern as we embark on sub 0.15 µm geometries. Careful quantification of the link between DC HC studies and circuit reliability/ performance is critical. The workshop will present possible methodologies to quantify circuit level reliability at very early stage in the technology development cycle. Attendees are encouraged to bring to discussion issues such as software tools to allow HC reliability by design, their limits and future developments to satisfy the need of both reliability and circuit design.

• Workshop 4: **Failure Analysis**

This workshop will focus on recent failure analysis technique developments and analysis. A discussion of techniques oriented at the analysis of current and next generation processes will focus on methods of fault localization and isolation. Analysis techniques suitable for fault localization through the substrate have become vital to the industry with the increasing use of multi-level metal processes and flip-chip packaging. Yield analysis techniques, tools and enhancements are adding to the Failure Analysis success and fault isolation. Feel free to bring questions, concerns and new ideas.

• Workshop 5: **Interconnects/Copper/Low-K**

With the on set of speed and reliability within submicron technology this topic is becoming more popular. The times have changed and new materials and challenges are occurring. At a time where cycle time and performance dominate process development, knowing the right test and what to do with the results is crucial. Join this group in a discussion of development and production testing Al or Cu based systems and its integration with Low K dielectrics. Topics to discuss will include, but not be limited to electromigration, stress voiding, defect detection and control, corrosion, low-K material performance etc…

• Workshop 6: **MEMS**

MEMS reliability continues to be a challenge as new developments and more empirical data availability continue. This workshop will be a great opportunity to share with your colleagues the recent advances in MEMS and how the MEMS growth is shaping.

• Workshop 7: **Package**

Semiconductor packaging is being pushed to limits in terms of I/O and thermal requirements while keeping the size small. This poses a great challenge to the reliability engineers. This workshop will present an opportunity to look into what is all out there for various packages and what different packages and materials are available to meet the needs of high speed, miniaturized applications.

• Workshop 8: **ESD/Latchup**

Even though most manufacturing is automated, ESD damage to the devices can still plague the development of a product. With reducing voltage requirements, but multiple power supplies for ever needing mixed signal semiconductor devices, latch-up can be major concern. The workshop will focus on issues reliability and design engineers face in order to get a robust product out to customers

TECHNICAL PROGRAM

Tuesday, May 1, 8:00 a.m., Great Hall North

SYMPOSIUM OPENING:

Anthony S. Oates, Symposium General Chair
Eric S. Snyder, Technical Program Chair

KEYNOTE: Integrated Communications Microsystems—Mark Pinto, Chief Technical Officer, Agere Systems (formerly the Microelectronics Div. of Lucent Technologies)

PRODUCT RELIABILITY I (*Session 1*)

Co-Chairs: Bob Knoell, Visteon and Dimitar Dimitrov, AMD

1.1 RELIABILITY DEGRADATION OF HIGH DENSITY DRAM CELL TRANSISTOR JUNCTION LEAKAGE CURRENT INDUCED BY BAND-TO-DEFECT TUNNELING UNDER THE OFF-STATE BIAS-TEMPERATURE STRESS—Y.P. Kim, Y.W. Park, J.T. Moon, and S.U. Kim, Samsung Electronics Co., Yongin-City, Korea

The band-to-defect tunneling (BDT) induced junction leakage current of high density DRAM cell transistor under the off-state bias-temperature (B-T) stress is investigated. The BDT leakage current is found to be the most critical limit in DRAM scaling, and the new off-state B-T stress is suggested to assess reliability degradation of the future thin gate oxide DRAM transistor.

1.2 A NEW METHOD FOR PREDICTING DISTRIBUTION OF DRAM RETENTION TIME—Y. Mori, R. Yamada, S. Kamohara, M. Moniwa, K. Ohyu, and T. Yamanaka, Hitachi, Ltd., Tokyo, Japan

A new method for predicting the distribution of DRAM retention time by using Test Element Groups constructed of memory cells is shown. The main retention time distribution is extracted from the structure and the measurement condition to depict the limiting defect tail is described.

1.3 IS PRODUCT SCREEN ENOUGH TO GUARANTEE LOW FAILURE RATE FOR THE CUSTOMER?—M.W. Ruprecht, Infineon Technologies, Essex Jct., VT, G. La Rosa, and R.G. Filippi, IBM Microelectronics, Hopewell Junction, NY

An in-line monitoring process methodology to prevent wear-out fails during the product lifetime for deep-sub micron technology is presented. Standby current fails from DRAM modules caused by PMOSFET Hot Carrier degradation is shown to be a product failure mechanism, requiring optimized in-line monitoring.

1.4 ANALYSIS OF ERRATIC BITS IN FLASH MEMORIES—A. Chimenton, P. Pellati, and P. Olivo, Università di Ferrara, Ferrara, Italy

New experimental results concerning erratic bits in FLASH memories are presented. They are obtained by tracking the threshold voltage dynamics during erase operations, providing insight to their physical nature.The particular shape of the erase curves so obtained, are used to derive a direct link between the amplitude of erratic threshold variations and that of the equivalent barrier height controlling FN injection.

1.5 INDIVIDUAL CELL MEASURING METHOD FOR FERAM RETENTION TESTING—N. Tanabe, H. Koike, T. Miwa, J. Yamada, A. Seike, N. Kasai, H. Toyoshima, and H. Hada, NEC Corp., Kanagawa, Japan

A novel test structure measures the read signal voltages of individual cells and records their addresses, to establish long-term data retention of an FeRAM chip is discussed. The expected retention times for all bits are estimated to extrapolate the relation between the read signal voltage and the retention time. The estimation shows that the upper limit of the retention time for each bit has a Gaussian distribution.

1.6 YIELD ENHANCEMENT AND YIELD MANAGEMENT OF SILICON FOUNDRIES USING IDDQ "STRESS CURRENT SIGNATURE"—M. Rubin, S. Natan, and D. Leary, Agilent Technologies, Fort Collins, CO

A novel Iddq analysis technique, using a "Stress Current Signature" is correlated with reliability failures. Case studies involving foundry yield management and failure analysis are described.

1.7 DYNAMIC VOLTAGE STRESSING APPLYING IN THE REDUCTION OF THE EARLY FAILURE RATE—C.-Y. Tsao, R.Y. Shiue, C.C. Ting, Y.S. Huang, Y.C. Lin, and J. Yue, TSMC, Hsin-Chu, Taiwan

Dynamic voltage stress (DVS) is used to improve the early life failure rate (ELFR). The ELFR reduction is shown to be > 60% when a delta source to bulk current screening is integrated with DVS. This enables a burn-in reduction methodology.

Tuesday, May 1, 2:00 p.m., Parallel Session, Great Hall North

PROCESS & RELIABILITY INTERACTIONS *(Session 2A)*

Co-Chairs: Fred Kuper, Philips Semiconductors and Walter Riordan, Intel

2A.1 A STUDY OF FORMATION AND FAILURE MECHANISM OF CMP SCRATCH INDUCED DEFECTS ON ILD IN A W-DAMASCENE INTERCONNECT SRAM CELL—S.-M. Jung, H.S. Kang, W.S. Cho, J.S. Uom, Y.J. Bae, K.S. Yoo, G.Y. Kim, and K.T. Kim, Samsung Electronics Co., Yongin-City, Korea

The formation mechanism of CMP scratches and the failure mechanism under the electrical stress in a conventional double layer ILD CMP process is analyzed and modeled using 8M bit SRAM . It was found that the CMP scratches could cause not only an initial failure but also a fatal long-term reliability failure similar to the time dependent dielectric breakdown. New CMP scratch free W-damascene technology was developed.

2A.2 THE EFFECTS OF STI PROCESS PARAMETERS ON THE INTEGRITY OF DUAL GATE OXIDES—H. Lim, S.-J. Lee, J. M. Youn, T.-H. Ha, J.-H. Lim, B.-H. Choi, K.-J. Kim, and K.T. Kim, Samsung Electronics Co., Yongin-City, Korea

The thick oxide constructed by dual gate oxide process shows a larger susceptibility to STI process parameters than single-step-grown thin oxide due to the wet etch before 2nd oxidation. It was found that the Deposition/Sputter ratio and the densification temperature of HDP oxide are critical parameters for the stress at the STI boundary and charge-to-breakdown characteristics of dual gate oxides.

2A.3 IMPROVEMENT IN RETENTION RELIABILITY OF SONOS NONVOLATILE MEMORY DEVICES BY TWO-STEP HIGH TEMPERATURE DEUTERIUM ANNEALS—J. Bu and M.H. White, Lehigh University, Bethlehem, PA

Two-step high temperature deuterium anneals applied in SONOS device fabrication, improves the retention reliability and endurance characteristics over traditional hydrogen anneals. Electrical characterization shows deuterium-annealed SONOS devices have nearly one order of magnitude longer retention time than hydrogen-annealed devices after 10^7 erase/write cycles at 85 °C to providea 0.5 V detection window.

2A.4 DATA RETENTION FAILURE IN NOR FLASH MEMORY CELLS—W.H. Lee, D.-K. Lee, Y.-M. Park, K.-S. Kim, K.-O. Ahn, and K.-D. Suh, Samsung Electronics Co., Kiheung-Eup, South Korea

Data retention failures due to non-optimized processes in NOR-type flash memory devices are presented. Contrary to charge leakage through defective oxide dielectric surrounding the floating gate, the data loss observed depends on whether the bit line contact is close to the cell or not. Based on experimental results, sodium movement in side wall spacers is established as an origin for the data retention failure in NOR-type flash memory.

2A.5 A NEW CONDUCTION MECHANISM FOR THE ANOMALOUS CELLS IN THIN OXIDES FLASH EEPROMS—A. Modelli, F. Gilardoni, STMicroelectronics, Agrate Brianza, Italy, D. Ielmini, Politecnico di Milano, Milano, Italy, and A.S. Spinelli, Università degli Studi dell'Insubria, Como, Italy

The temperature dependence of the anomalous leakage current in the tail cells of flash memory is investigated on arrays with different oxide thickness. It is shown that both the conduction mechanism and the annealing kinetics of the leakage current change when the thickness is reduced below about 8 nm, becoming independent of temperature. The microscopic conduction of the tail cells is analyzed to investigate the conduction model in thin oxides.

2A.6 N-CHANNEL VERSUS P-CHANNEL FLASH EEPROM-WHICH ONE HAS BETTER RELIABILITIES—S.S. Chung, S.T. Liaw, Z.H. Ho, National Chiao Tung Univ., Hsinchu, Taiwan, C.J. Lin, TSMC, Hsinchu, Taiwan, C.M. Yih, National Chiao Tung Univ., Hsinchu, Taiwan, D.S. Kuo, and M.S. Liang, TSMC, Hsinchu, Taiwan

In this paper, a comprehensive study of n- and p-channel flash cells in terms of various reliability issues is presented. Results show that the cell speed, endurance, and gate/read disturb of p-channel cell is much better than those of n-channel cells; except that p-channel cell should use the DINOR structure to prevent drain disturb. As a whole, the p-channel cell features high speed, lower power, and better reliability. These make it more attractive for future applications.

2A.7 NEW TECHNIQUE FOR FAST CHARACTERIZATION OF SILC DISTRIBUTION IN FLASH ARRAYS—D. Ielmini, Politecnico di Milano, Milano, Italy, A.S. Spinelli, Università degli Studi dell'Insubria, Como, Italy, A.L. Lacaita, Politecnico di Milano, Milano, Italy, L. Confalonieri, and A. Visconti, STMicroelectronics, Agrate Brianza, Italy

The extraction of SILC distributions in Flash memory cells can lead to an improved understanding of the cell leakage mechanism, as well as to more refined reliability evaluations. A new technique for the extraction of cell SILC is presented, which does not require the tracking of the V_T evolution of individual cells, but only the cumulative behavior of the array. Validation of the technique with simulation of the cumulative distribution of V_T and of failure time is also carried out.

Tuesday, May 1, 2:00 p.m., Parallel Session, Scotland

MEMS RELIABILITY CHARACTERIZATION *(Session 2B)*

Co-Chairs: Danelle Tanner, Sandia National Labs and
Susanne Arney, Lucent Technologies

2B.1 RELIABILITY OF A MEMS TORSIONAL RATCHETING ACTUATOR—D.M. Tanner, S.M. Barnes, J.A Walraven, and N.F. Smith, Sandia National Labs, Albuquerque, NM

A new surface-micromachined actuator, the Torsional Ratcheting Actuator (TRA) has undergone reliability testing and failure analysis. Tests were performed at three frequencies (333 Hz, 1000 Hz, and 3000 Hz). A failure mechanism (observed in the guide dimples) was determined to be adhesion of rubbing polysilicon surfaces.

2B.2 FULL THREE-DIMENSIONAL MOTION CHARACTERIZATION OF A GIMBALLED ELECTROSTATIC MICROACTUATOR—C. Rembe, UC Berkeley, Berkeley, CA, L. Muller, Network Photonics, Inc., Boulder, CO, R.S. Muller, A.P. Pisano, and R.T. Howe, UC Berkeley, Berkeley, CA

We have developed a computer-controlled stroboscopic interferometer for characterization of rapid dynamic processes in Microelectromechanical Systems (MEMS). Digital image processing is used to achieve high-resolution measurement of out-of-plane motion as well as of in-plane motion. The nonlinear three-dimensional dynamic behavior of a gimballed electrostatic actuator for a hard disk drive is investigated.

2B.3 NON-DESTRUCTIVE RESONANT FREQUENCY MEASUREMENT ON MEMS ACTUATORS—N.F. Smith, D.M. Tanner, and S.L. Miller, Sandia National Labs, Albuquerque, NM

A method has been developed to determine the resonant frequency of MEMS actuators. This technique is non-destructive to the device because it does not require the device be stimulated at resonance. The technique has been applied to several devices and compared to results obtained from traditional techniques.

2B.4 SIZE EFFECT ON THE MECHANICAL PROPERTIES AND RELIABILITY ANALYSIS OF MICROFABRICATED POLYSILICON THIN FILMS—J.N. Ding, Y.S. Meng, and S.Z. Wen, Tsinghua Univ., Beijing, PR China

A new microtensile test device using a magnetic-solenoid force actuator was developed to evaluate the mechanical properties of microfabricated polysilicon thin films. Statistical analysis of the specimen size effects on the tensile strength was investigated. The recommendation for design with strain criterion of fracture in polysilicon thin films was given.

Tuesday, May 1, 4:05 p.m., Parallel Session, Scotland

PACKAGING AND ASSEMBLY *(Session 2C)*

Co-Chairs: Tom Moore, Texas Instruments and S. Sidharth, AMD

2C.1 (INVITED, ESREF BEST PAPER) A SIMPLE MODEL FOR THE MODE I POPCORN EFFECT FOR IC PACKAGES—P. Alpern, K.C. Lee, Infineon Technologies, R. Dudek, IZM, R. Tigner, Infineon Technologies

A simple model for the Mode I popcorn effect is presented here for packages with rectangular die pad (P-DSO). A package “stability parameter” relating to its moisture sensitivity is derived from the popcorn model which describes the critical factors for a robust package. Nomograms generated from the model enable an easy estimation of moisture sensitivity levels with different die pad sizes and molding compound underpad thicknesses and for different soldering temperatures ranging from 220°C to 260°C (Pb-free soldering).

2C.2 IMPROVING CORROSION-RESISTANCE OF SILICON-GLASS MICROPACKAGES USING BORON DOPING AND/OR SELF-INDUCED GALVANIC BIAS—B.H. Stark, M.R. Dokmeci, T.J. Harpster, and K. Najafi, Univ. of Michigan, Ann Arbor, MI

MEMS intended for use in harsh environments, such as the human body, use micro-packages to maintain their integrity. Two novel methods are reported for improving the corrosion resistance of glass-silicon micro-packages in high temperature saline soak tests. By using boron doping and/or galvanic biasing, the dissolution of polysilicon can be reduced by several orders of magnitude.

2C.3 A FATIGUE THEORY FOR SOLDERS—S. Wen and L.M. Keer, Northwestern Univ., Evanston, IL

A fatigue theory is presented for solders. It is assumed that resolved shear stress causes the formation of persistent slip bands (PSB's). Mura's theory of crack initiation is adopted for the microcrack formation within the PSB's. Grains with different crystallographic orientation fail at different numbers of cycles. By a process of percolation, the structure reaches failure when the total portion of failed grains reaches a critical value.

2C.4 A NEW MECHANICAL CONCEPT AND ITS APPLICATION IN RELIABILITY EVALUATION OF SOLDER JOINT CONNECTIONS USED IN ELECTRONIC PACKAGING—X. Ma, CEPREI, Guangzhou, PR China, Y. Qian, Harbin Institute of Tech., Harbin, PR China, and X. Zhang, CEPREI, Guangzhou, PR China

A new mechanical concept, relative damage stress (RDS) is presented to describe the failure behavior of solder joints during accelerated thermal fatigue testing of board-level assemblies. RDS encompasses the Mises equivalent stress, which governs plasticity of solder alloy, the stress triaxiality, which reflects the assembly constraint, the Poisson's ratio, and the yield stress, which reflects the temperature dependence of material properties. Therefore, we can directly compare the RDS at different temperatures during temperature cycling, and recommend improvements in the design of accelerated thermal fatigue tests.

Tuesday, May 1, 6:00 p.m. — 9:00 p.m., England/Ireland

POSTER SESSION & RECEPTION

Wednesday, May 2, 8:00 a.m., Parallel Session, Great Hall North

OXIDE I *(Session 3A)*

Co-Chairs: Robin Degraeve, IMEC and
Paul Nicollian, Texas Instruments

3A.1 (INVITED) DEFECT GENERATION AND RELIABILITY OF ULTRA-THIN SILICON DIOXIDE AT LOW VOLTAGE—J.H. Stathis and D.J. DiMaria, IBM, Yorktown Hgts., NY

The reliability of ultrathin SiO_2 layers and the consequences for continued thickness scaling are a critical technology issue. We review the defect generation and breakdown physics of ultrathin oxides at low voltages. Although the defect generation rate decreases exponentially as supply voltage is reduced, tunneling currents increase exponentially with decreasing oxide thickness, leading to a diminishing margin for reliability.

3A.2 (INVITED) IDENTIFICATION OF ATOMIC SCALE DEFECTS INVOLVED IN OXIDE LEAKAGE CURRENTS—P.M. Lenahan, J.J. Mele, J. Campbell, A. Kang, Penn State Univ., University Park, PA, R.K. Lowry, D. Woodbury, Intersil, Palm Bay, FL, and S.T. Liu, Honeywell Corp., Plymouth, MN

We identify atomic scale defects involved in Stress-Induced-Leakage-Currents (SILC) with a combination of electron spin resonance (ESR) and electrical measurements. In addition, we propose a model of SILC based upon these defects and the fundamental principles of the statistical mechanics of defects in solids.

3A.3 NANOSCALE OBSERVATIONS OF THE ELECTRICAL CONDUCTION OF ULTRA THIN SiO_2 FILMS WITH CONDUCTING ATOMIC FORCE MICROSCOPY—M. Porti, M. Nafría, X. Aymerich, Univ. Autònoma de Barcelona, Bellaterra, Spain, A. Olbrich, and B. Ebersberger, Infineon Technologies AG, Munich, Germany

For the first time, a Conducting Atomic Force Microscope (C-AFM) is used to study both the pre- and post-breakdown conduction of a single SiO_2 breakdown spot. The results provide direct evidence of the nanometer scale nature of the degradation and breakdown

3A.4 SOFTENING OF BREAKDOWN IN ULTRA-THIN GATE OXIDE NMOSFETS AT LOW INVERSION LAYER DENSITY—S. Lombardo, Consiglio Nazionale delle Ricerche, Catania, Italy, F. Crupi, Università di Messina, Messina, Italy, and J.H. Stathis, IBM, Yorktown Hgts, NY

The post breakdown I-V characteristics of ultra-thin gate oxides subjected to constant voltage Fowler-Nordheim stress in nMOSFETs were investigated. It is shown that under the same stress field conditions the oxide I-V characteristics after the breakdown event strongly depend on the density of electrons in the inversion layer.

3A.5 CALCULATING THE ERROR IN LONG TERM OXIDE RELIABILITY ESTIMATES—B.P. Linder, J.H. Stathis, and D.J. Frank, IBM, Yorktown Hgts, NY

Ultra-thin oxide reliability is a critical issue in integrated circuit scaling. Oxide reliability may actually prevent future scaling of SiO_2 gate dielectrics. The statistical error in long term oxide reliability projections has not been cohesively treated. Using Monte Carlo techniques, the amount of uncertainty in reliability projections is calculated. Analyzing typical published data, the uncertainty in the failure rate is greater than an order of magnitude.

Wednesday, May 2, 10:30 a.m., Parallel Session, Great Hall North

WLR FOR INTERCONNECTS *(Session 3B)*

Co-Chairs: J. Joseph Clement, Sandia National Labs and Armin Fischer, Infineon Technologies

3B.1 COMPARISON OF ISOTHERMAL, CONSTANT CURRENT AND SWEAT WAFER LEVEL EM TESTING METHODS—T. Lee, D. Tibel, and T. Sullivan, IBM Microelectronics, Essex Jct., VT

Data are presented from three wafer level test techniques – Isothermal, Constant Current, and SWEAT. The three techniques are compared and evaluated.

3B.2 REAL CASE STUDY FOR ISOTHERMAL EM TEST AS A PROCESS CONTROL METHODOLOGY—S.-Y. Lee, J.B. Lai, S.C. Lee, L.H. Chu, R.Y. Shiue, and J. Yue, TSMC, Hsin-Chu, Taiwan

The failure mechanism observed in fast wafer-level isothermal EM tests is found to be similar to that in conventional package EM tests, when the appropriate failure criterion is used. The capability of the isothermal test to detect metal reliability problems is shown to correlate well with conventional long-term tests in real case studies.

3B.3 EXPERIMENTAL COMPARISON OF WAFER LEVEL RELIABILITY (WLR) AND PACKAGED ELECTROMIGRATION TESTS—C. Ryu, T.-L. Tsai, A. Rogers, C. Jesse, T. Brozek, D. Zarr, M. Adamson, S. Nayak, and J. Walls, Motorola SPS, Chandler, AZ

The sensitivity of a wafer level reliability electromigration (WLR EM) test was investigated for various backend process variations. Although the WLR EM test uses very different test methodology from conventional long-term packaged EM testing, the WLR EM data was found to have good correlation with the packaged EM results.

3B.4 COMPARISON OF VIA/LINE PACKAGE LEVEL VS. WAFER LEVEL RESULTS—D. Tibel and T. Sullivan, IBM Microelectronics, Essex Jct., VT

Scaled isothermal wafer electromigration fail times are compared to conventional package test fail times, with reasonable agreement. Temperature and current acceleration appear to be analytically separable for wafer testing. Activation energies are similar, but wafer fail sites do not resemble package fail sites.

Wednesday, May 2, 8:00 a.m., Parallel Session, Scotland

OPTOELECTRONICS & COMPOUND SEMICONDUCTOR *(Session 3C)*

Co-Chairs: Sammy Kayali, JPL and
J.J. Liou, University of Central Florida

3C.1 ACCELERATED STRESSING AND DEGRADATION MECHANISMS FOR SI-BASED PHOTO-EMITTERS—A. Chatterjee and B.L. Bhuva, Vanderbilt Univ., Nashville, TN

Light emitters are stressed with ac, dc, and temperature. The results clearly show that the effects of ac and temperature stressing on light emission are negligible. DC stressing results in light coalescence with total light emission coming out of the junction remain constant. The light coalescence is also a strong function of the device layout. Reliability of light emission is extremely good under all the stress conditions considered for applications of on-chip interconnect.

3C.2 LOW-TEMPERATURE, HIGH-CURRENT LIFETESTS ON INP-BASED HBT'S—B.M. Paine, Hughes S&C Co., Los Angeles, CA, S. Thomas III, HRL Labs, Malibu, CA, and M.J. Delaney, Hughes S&C Co., Los Angeles, CA

Lifetests have been conducted on discrete InP HBTs, at relatively low temperatures and high collector currents. The goal is to test for low-activation-energy failure mechanisms that may have been undetectable in conventional lifetests. Analysis indicates relatively low probability of failure in typical applications.

3C.3 DEGRADATION CHARACTERISTICS OF AlGaN/GaN HIGH ELECTRON MOBILITY TRANSISTORS (HEMTS)—H. Kim, B. Green, V. Tilak, H. Cha, J.A. Smart, J.R. Shealy, and L.F. Eastman, Cornell University, Ithaca, NY

Results of reliability tests on AlGaN/GaN power HEMT's are presented for the first time. The degradation characteristics of these devices were measured under various stress conditions such as reverse gate bias, RF overdrive, and elevated temperature storage. The devices demonstrated good reliabilities for high power and high temperature applications under high stress conditions.

Wednesday, May 2, 10:30 a.m., Parallel Session, Scotland

ESD/LATCHUP *(Session 3D)*

Co-Chairs: Robert Gauthier, IBM and Jeremy Smith, Motorola

3D.1 CHARACTERIZATION AND INVESTIGATION OF THE INTERACTION BETWEEN HOT ELECTRON AND ELECTROSTATIC DISCHARGE STRESSES USING NMOS DEVICES IN 0.13µM CMOS TECHNOLOGY—A. Salman, George Mason Univ., Fairfax, VA, R. Gauthier*, S. Furkay*, M. Muhammad, GCI, Parsippany, NJ, C. Putnam*, VT, D. Ioannou, George Mason Univ., Fairfax, VA, P. Nguyen*, W. Stadler, and Kai Esmark, Infineon Technologies, Munich, Germany
*IBM Microelectronics, Essex Jct., VT

The high-current characteristics encountered during electrostatic discharge (ESD) events using a NMOS/LNPN protection device in a 0.13 µm CMOS technology are investigated for different device parameters. The effect of silicide blocking and hot electron (HE) shifts on the second breakdown current of the NMOS devices are studied for both

silicided and non-silicided devices. The impact of non-destructive ESD stressing on HE shifts is also studied for the same devices.

3D.2 NON-UNIFORM BIPOLAR CONDUCTION IN SINGLE FINGER NMOS TRANSISTORS AND IMPLICATIONS FOR DEEP SUBMICRON ESD DESIGN—K.-H. Oh, Stanford Univ., Stanford, CA, C. Duvvury, C. Salling, Texas Instruments, Dallas, TX, K. Banerjee, and R.W. Dutton, Stanford Univ., Stanford, CA

A detailed study of the non-uniform bipolar conduction phenomenon in single finger NMOS transistors and its implications for deep submicron ESD design is investigated. The impact of substrate bias to overcome this effect to achieve practical designs has been demonstrated. Additionally, a new concept of intrinsic second breakdown triggering current is introduced, which can be used to generate efficient ESD design guidelines for deep submicron processes.

3D.3 ADVANCED 2D LATCH-UP DEVICE SIMULATION-A POWERFUL TOOL DURING DEVELOPMENT IN THE PRE-SILICON PHASE—S. Bargstädt-Franke and K. Oettinger, Infineon Technologies AG, Munich, Germany

Parasitic device characteristics which change the latch-up sensitivity during the early technology development phase are not easily and accurately simulated with today's device simulators. In this paper, calibrated 2-D simulations are used for optimizing the technology for these parasitic effects, leading to an area optimization which helps to reduce the chip size/cost.

3D.4 AN ANALYSIS OF BIPOLAR BREAKDOWN AND ITS APPLICATION TO THE DESIGN OF ESD PROTECTION CIRCUITS—S. Joshi, Univ. of Ill, Urbana-Champaign, Urbana, IL, R. Iday, Motorola, Tempe, AZ, P. Givelinz, Motorola, Toulouse, France, and E. Rosenbaum, Univ. of Ill, Urbana-Champaign, Urbana, IL

Analytical expressions for the breakdown voltage of an NPN with a resistively grounded base, both with and without the zener diode trigger which is used in a common ESD protection circuit, are presented for the first time. The results are used to explain anomalous behavior in the I-V curve of the protection circuit and to achieve a more efficient ESD protection circuit design.

3D.5 PARASITIC BIPOLAR TRANSISTOR MODEL USING GENERATED-HOLE-DEPENDENT BASE RESISTANCE—K. Suzuki, H. Anzai, T. Nomura, and S. Satoh, Fujitsu Ltd., Atsugi, Japan

Injected electrons are known to modulate base resistance but this is found to not be the case during snapback due to the electric field associated with injected electrons being compensated by the holes generated in the drain region. A new model is developed that depends on generated holes as well as injected electrons.

3D.6 DESIGN AND ANALYSIS OF NEW PROTECTION STRUCTURES FOR SMART POWER TECHNOLOGY WITH CONTROLLED TRIGGER AND HOLDING VOLTAGE—V. De Heyn, G. Groeseneken, B. Keppens, N. Mahadeva Iyer, IMEC, Leuven, Belgium, L. Vacaresse, and G. Gallopyn, Alcatel Microelectronics, Oudenaarde, Belgium

An adjustable trigger and holding voltage device is designed in a smart power technology by changing the lateral bipolar base distance. The layout variation that controls the holding voltage also leads to a different snapback mechanism and a different current flow through the device. Excellent ESD capabilities of 16 mA/μm and 20 mA/μm of device width have been achieved.

Wednesday, May 2, 12:10 p.m., England/Ireland

AWARDS LUNCHEON

Wednesday, May 2, 2:00 p.m., Parallel Session, Great Hall North

PRODUCT RELIABILITY II *(Session 4A)*

Co-Chairs: Rich Blish, AMD and
Courtney Black, Silicon Bandwidth

4A.1 HISTORICAL TREND IN ALPHA-PARTICLE INDUCED SOFT ERROR RATES OF THE ALPHA MICROPROCESSOR—N. Seifert, D. Moyer, and N. Leland, Compaq Computer, Shrewsbury, MA

The historical trend in Alpha-Particle induced soft-error rates of Alpha microprocessors fabricated in different technologies demonstrates the increasing importance of failures occurring in the core logic to the overall chip-level FIT rate. The impact of scaling of the operating voltage and of the process on the SER is discussed.

4A.2 A RELIABILITY METHODOLOGY FOR LOW TEMPERATURE DATA RETENTION IN FLOATING GATE NON-VOLATILE MEMORIES—P.J. Kuhn, A. Hoefler, T.S. Harp, B.E. Hornung, R.E. Paulsen, D. Burnett, and J.M. Higman, Motorola, Austin, TX

A reliability assessment methodology consisting of a statistical model and experiments is used to evaluate the leakage mechanism responsible for Low Temperature Data Retention in floating gate non-volatile memories. The nature of the leakage mechanism and the methodology necessary to observe and accurately assess this phenomenon are described.

4A.3 HIGH-PERFORMANCE CHIP RELIABILITY FROM SHORT-TIME-TESTS: STATISTICAL MODELS FOR OPTICAL INTERCONNECT AND HCI/TDDB/NBTI DEEP-SUBMICRON TRANSISTOR FAILURES—A. Haggag, K. Hess, W. McMahon, K. Cheng, J. Lee, and J. Joseph, Univ. of Illinois, Urbana, IL

The failure-time distribution of both deep-submicron transistors and optical interconnects owing to the presence of a common defect activation energy distribution is derived. Short-time device degrdation may be used to extract the tails of this semi-symmetric distribution. Through the application of novel reliability qualification rules, “latent failures” can be avoided by design changes implemented for reliability.

4A.4 AN APPLICATION-SPECIFIC USAGE MODEL FOR FLASH MEMORY READ DISTURB RELIABILITY—T.S. Harp, P.J. Kuhn, J.M. Higman, R.E. Paulsen, and B.E. Hornung, Motorola, Austin, TX

We present a method to account for customer applications or usage profiles when evaluating read disturb reliability of flash memory products. Monte Carlo simulations explore reliability of read disturb mechanisms following Weibull and LogNormal statistics vs. application. Experimental data supporting the model will be available for final paper.

Wednesday, May 2, 3:40 p.m., Parallel Session, Great Hall North

FAILURE ANALYSIS *(Session 4B)*

Co-Chairs: Jacob Phang, National Univ. of Singapore and
Travis Eiles, Intel

4B.1 CASE HISTORY: NOVEL FA TECHNIQUES USED TO RECOVER EEPROM DATA FROM THE SWISSAIR 111 CRASH—R. Haythornthwaite, A. Earle, and A. Rahal, Chipworks Inc., Ottawa, Canada

The pre-crash memory contents were successfully read from a corroded and damaged 256K EEPROM from Swissair 111. High temperatures, etchants and SEM radiation were forbidden to preserve data. Wires were attached to missing bond pads using epoxy before FIB tracks were laid to the bonds and FIB repairs made.

4B.2 NOVEL NONDESTRUCTIVE AND NON-ELECTRICAL-CONTACT FAILURE ANALYSIS TECHNIQUE - SCANNING LASER-SQUID MICROSCOPY—K. Nikawa and S. Inoue, NEC Corp., Kawasaki, Japan

A novel failure analysis technique that can localize electrical defects has been developed. In this technique, the magnetic field produced by a laser-beam-induced current is detected by high Tc DC SQUIDs. The spatial resolution has been demonstrated to be better than 1.3.

4B.3 ANALYSIS OF VIA-VOID GENERATION MECHANISM FOR GIGA-BIT-SCALE DRAM—D.H. Kim, J.S. Park, B.C. Kim, S.C. Lee, M.K. Bae, J.W. Nam, I.S. Park, H.Y. Kim, T.K. Kim, J.S. Kim, Y.J. Park, J.I. Hong, and J.W. Park, Samsung Electronics Co., Younin-Si, Korea

The reaction of Al and stress enhancement after interconnection process induce volume shrinkage of the interconnection line. This is the generation mechanism of the via-void. The void-free, high reliable gigabit-scale DRAM could be realized when the reaction of Al and the interconnection stress are minimized.

4B.4 STUDY OF METAL IMPURITIES BEHAVIOR DUE TO DIFFERENCE IN ISOLATION STRUCTURE ON ULSI DEVICES—K. Matsukawa, Y. Kimura, H. Yamamoto, and Y. Mashiko, Mitsubishi Electric Corp., Itami, Japan

We have shown that the behavior of metal impurities such as Cu and Ni is different due to the difference of isolation structure. It's found that Cu is trapped easily at STI, and Ni is trapped in bulk micro defects (BMD) regardless of isolation structure.

4B.5 HIGH SRAM STANDBY CURRENT DUE TO THE PRINTING OF SPURIOUS IMAGES—S. Tang, M. Mims, T. Cynkar, P.J. Marcoux, and D. Eaton, Agilent Technologies, Fort Collins, CO

Photoemission microscopy of a 2Mbit SRAM identified a physical pattern of quiescent current (IDDq) failures on the regular array of this circuit. The pattern of IDDq failures correlated almost exactly with identifying marks on the edge of the SRAM gate reticle. This discovery led to the detection of contamination of the photolithographic imaging optics that resulted in ghost images.

Wednesday, May 2, 2:00 p.m., Parallel Session, Scotland

PROCESS INDUCED DAMAGE *(Session 4C)*

Co-Chairs: Terence Hook, IBM Microelectronics and Kin P. Cheung, Lucent Technologies

4C.1 THE IMPACT OF TRENCH GEOMETRY AND PROCESSING ON THE PERFORMANCE AND RELIABILITY OF LOW VOLTAGE POWER UMOSFETS—S.A. Suliman, N. Gallogunta, L. Trabzon, J. Hao*, G. Dolny*, R. Ridley*, T. Greb*, J. Benjamin*, C. Kocon*, J. Zeng*, O.O. Awadelkarim, S.J. Fonash, M. Horn, and J. Ruzyllo, Penn State Univ., University Park, PA
*Intersil, Mountaintop, PA

This paper reports on performance and reliability studies of vertical n-channel UMOSFETs. Using SEMs, charge pumping, and transistor parameter measurements, this study examines UMOSFET reliability in terms of trench geometry and trench processing. The effective mobility along the trench wall is shown to be a function of RIE-induced damage, and the reliability of the device to be strongly dependent on the depth and curvature of the trench.

4C.2 THE EFFECTS OF PLASMA INDUCED DAMAGE ON TRANSISTOR DEGRADATION AND THE RELATIONSHIP TO FIELD PROGRAMMABLE GATE ARRAY PERFORMANCE—F.E. Pagaduan, J.K. Lee, V. Vedagarbha, K. Lui, M.J. Hart, D. Gitlin, Xilinx, Inc., San Jose, CA, T. Takaso, S. Kamiyama, and K. Nakayama, Seiko Epson Corp., Yamagata-ken, Japan

This paper shows the effects of damage on a 4.5-nm gate oxide transistors and the resulting degradation observed on product-level performance of a Field Programmable Gate Array (FPGA). The magnitude of the PFET Negative Bias Temperature Instability is shown to be affected by a plasma ashing step. By eliminating this step the transistor degradation was reduced, and the product-level performance of the FPGA was also improved, correlating strongly with the measured transistor threshold shift.

4C.3 IMPROVEMENT OF MOSFET SUBTHRESHOLD LEAKAGE CURRENT BY ITS IRRADIATION WITH HYDROGEN RADICALS GENERATED IN MICROWAVE-EXCITED HIGH-DENSITY INERT GAS PLASMA—Y. Saito, H. Takahashi, K. Ohtsubo, M. Hirayama, S. Sugawa, Tohoku Univ., Aoba-ku, Japan, H. Aharoni, Ben-Gurion Univ., Beer-Sheva, Israel, and T. Ohmi, Tohoku Univ., Aoba-ku, Japan

In this paper it is shown that the drain leakage of MOSFETs is improved by irradiation with hydrogen radicals generated in a microwave-excited Ar/H_2 plasma. This specific conditions of the plasma were carefully chosen to produce a high flux of hydrogen radicals with minimal plasma-induced damage. Pressure, gas constituents, and the plasma generation technique were varied in these experiments to optimize the annealing effect without inducing damage.

Wednesday, May 2, 3:40 p.m., Parallel Session, Scotland

INTERCONNECT RELIABILITY *(Session 4D)*

Co-Chairs: Timothy Sullivan, IBM Microelectronics and James Walls, Motorola

4D.1 RESERVOIR MODELING FOR ELECTROMIGRATION IMPROVEMENT OF METAL SYSTEMS WITH REFRACTORY BARRIERS—M.J. Dion, Intersil, Melbourne, FL

Metal reservoirs have been shown to increase electromigration lifetimes in barrier metal systems. This study finds that EM lifetime increase is related to the log of reservoir length in a constant width line. Number of vias, via spacing, and metal overlap do not play significant roles in defining the EM lifetime.

4D.2 THE QUANTITATIVE ASSESSMENT OF STRESS-INDUCED VOIDING IN PROCESS QUALIFICATION—A. Fischer, A.E. Zitzelsberger, and M. Hommel, Infineon Technologies, Munchen, Germany

The primary stressmigration-related reliability risk is the resistance increase due to stress-induced voids. Based on experimental data, we present a new model for the estimation of the stressmigration-limited lifetime. Further, we show that reduced electromigration performance must be considered for stress-void damaged metal lines.

4D.3 STATISTICS OF ELECTROMIGRATION EARLY FAILURES IN CU/OXIDE DUAL-DAMASCENE INTERCONNECTS—E.T. Ogawa, K.-D. Lee, H. Matsuhashi, A.J. Bierwag, P.R. Justison, A.N. Ramamurthi, P.S. Ho, Univ. of TX at Austin, Austin, TX, V.A. Blaschke, and R.H. Havemann, SEMATECH, Austin, TX

Evidence of the statistical detection of two distinct ("weak" and "strong" mode) failures in dual-damascene Cu/oxide interconnects is reported. A combination of single and repeated serial chains of nominally identical interconnects are used in conjunction with statistical analysis based on "weakest-link" concepts. Results confirm the utility of the multi-link approach in electromigration reliability analysis.

4D.4 TRADE-OFF BETWEEN RELIABILITY AND POST-CMP DEFECTS WITH RECRYSTALLIZATION ANNEAL IN COPPER DAMASCENE INTERCONNECTS—G. Alers, Novellus Systems, San Jose, CA, D. Dornisch, Conexant, Newport Beach, CA, J. Siri, K. Kattige, L. Tam, E. Broadbent, and G. Ray, Novellus Systems, San Jose, CA

We have evaluated the impact of anneal on grain size, texture, stress, electromigration lifetime and density of post-CMP defects, such as pits and voids, in copper damascene interconnects. There appears to be a trade-off between full recrystallization of narrow trenches for improved electromigration lifetime and the occurrence of post-CMP defects which needs to be optimized.

4D.5 IMPACT OF LOW-K DIELECTRICS AND BARRIER METALS ON TDDB LIFETIME OF CU INTERCONNECTS—J. Noguchi, T. Saitoh, N. Ohashi, H. Ahihara, H. Maruyama, M. Kubo, and H. Yamaguchi, Hitachi, Ltd., Tokyo, Japan

TDDB characteristics of Cu interconnects using various low-k dielectrics and barrier metals were investigated. Degradation of TDDB due to Cu-ion diffusion is mainly caused, not by thermal stress, but by electrical stress. As the dielectric constant goes lower, the TDDB failure distributions shift to lower electric field strength.

Wednesday, May 2, 7:30 p.m. — 9:30 p.m., (rooms to be announced)

WORKSHOPS

Thursday, May 3, 8:00 a.m., Great Hall North

OXIDE II *(Session 5)*

Co-Chairs: Paul Nicollian, Texas Instruments and Robin Degraeve, IMEC

5.1 RELATION BETWEEN BREAKDOWN MODE AND BREAKDOWN LOCATION IN SHORT CHANNEL NMOSFETS AND ITS IMPACT ON RELIABILITY SPECIFICATIONS—R. Degraeve, B. Kaczer, A. De Keersgieter, and G. Groeseneken, IMEC, Leuven, Belgium

A method to determine the breakdown position in short channel nmosfets is introduced. We find that SBD occurs exclusively in the transistor channel while the hardest circuit killing breakdowns occur above the source and drain extension regions. Since these killing breakdowns make up only a small fraction of all breakdowns, a relaxation of the reliability specification is possible.

5.2 ANALYTIC MODELING OF LEAKAGE CURRENT THROUGH MULTIPLE BREAKDOWN PATHS IN SiO_2 FILMS—E. Miranda, Universidad de Buenos Aires, Buenos Aires, and J. Suñé, Universidad Autónoma de Barcelona, Bellaterra, Spain

An analytic model for the leakage current through broken down gate oxides in MOS structures is presented. It is based on the physics of mesoscopic conducting systems and the quantum properties of point contacts. The model covers the hard breakdown, the soft breakdown and the stress-induced-leakage-current conduction modes in a consistent manner.

5.3 EXPERIMENTAL STUDY OF GATE VOLTAGE SCALING FOR TDDB UNDER DIRECT TUNNELING REGIME—M. Takayanagi, S. Takagi, and Y. Toyoshima, Toshiba Corp., Yokohama, Japan

The slope of Tbd with respect to V_g for TDDB is experimentally studied as a function of T_{ox} and V_g for accurate voltage scaling. A model to explain the experimental voltage acceleration factor is presented. It is quantitatively shown that the significant decrease in hole generation due to lower electron energy greatly helps the TDDB reliability at operating voltage.

5.4 ACCURATE AND ROBUST NOISE-BASED TRIGGER ALGORITHM FOR SOFT BREAKDOWN DETECTION IN ULTRA THIN OXIDES—P. Roussel, R. Degraeve, B. Kaczer, and G. Groeseneken, IMEC, Leuven, Belgium

An algorithm for accurate and robust triggering on soft breakdown during constant voltage stress based on gate current noise increase is presented.

Triggering on current spikes or pre-BD events is avoided. This test assures correct SBD-detection in a wide range of stress conditions and various geometries.

5.5 SOFT BREAKDOWN TRIGGERS FOR LARGE AREA CAPACITORS UNDER CONSTANT VOLTAGE STRESS—J. Schmitz, H.J. Kretschmann, H.P. Tuinhout, and P.H. Woerlee, Philips Research Labs, Eindhoven, The Netherlands

This work discusses methods to identify a soft breakdown during constant voltage stress of large area capacitors (0.1-10 mm^2) with gate oxide thickness down to 1.8 nm. We show that with data filtering, the classical current increase trigger can still be used down to the thinnest oxide, while an increased RMS variation of the current does not identify all breakdowns.

Thursday, May 3, 10:30 a.m., Great Hall North

DISCUSSION PANEL

IS BURN-IN ELIMINATION POSSIBLE?

PANEL: Carl Peridier ..... Agere Systems
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Thursday, May 3, 2:00 p.m., Great Hall North

HOT CARRIERS *(Session 6)*

Co-Chairs: Giuseppe La Rosa, IBM Microelectronics and Roland Thewes, Infineon Technologies

6.1 ROLE OF E-E SCATTERING IN THE ENHANCEMENT OF CHANNEL HOT CARRIER DEGRADATION OF DEEP SUB-MICRON NMOSFETS AT HIGH V_{GS} CONDITIONS—S.E. Rauch III, G. La Rosa, and F. Guarin, IBM Microelectronics, Hopewell Jct., NY

We propose a new phenomenological CHC model, based on e-e scattering, that explains the worsening of the HC damage at high $V_{GS} = V_{DS}$ observed in deep sub-micron NMOSFETs and allows HC lifetime predictions over the full gate voltage range. This description takes into account the dependence of the electron concentration near the drain on the applied V_{GS} and describes, for the first time, its impact to the EES induced HC damage.

6.2 ANALYSIS OF NEW HOT CARRIER DEGRADATION PHENOMENA: "W" OR "S" SHAPE EVOLUTION OF LDD NMOSFET—J.-R. Shih, L.H. Chu, R.Y. Shiue, and J. Yue, TSMC, Hsin-Chu, Taiwan

A new hot carrier phenomenon with "W" or "S"-shape evolution has been observed and analyzed. It does not follow the power law or the two-step degradation model. A three-stage degradation model has been proposed. The transistor with SSRW channel and LDD with 0°-tilt angle will enhance this effect.

6.3 ON THE DOMINANT INTERFACE TRAP GENERATION PROCESS DURING HOT-CARRIER STRESSING—S. Ang and C.H. Ling, The National Univ. of Singapore, Singapore

Analysis of a kink, observed in the charge pumping current versus time curve, supports a recent claim of a new interface trap generation process during hot-carrier stressing of MOSFETs. This process, which may be related to the interaction between hot carriers and the Si/SiO2 interface, exhibits a distinctively high generation coefficient, and could ultimately limit the lifetime of N-MOSFETs under ac operation.

6.4 A NEW PHYSICAL AND QUANTITATIVE WIDTH DEPENDENT HOT CARRIER MODEL FOR SHALLOW-TRENCH-ISOLATED CMOS DEVICES—S.S. Chung, S.-J. Chen, W.-J. Yang, and J.-J. Yang, National Chiao Tung Univ., Hsinchu, Taiwan

Enhanced degradation in STI CMOS devices with reducing gate width was studied. A new physical and quantative model to describe the enhanced degradation for both n- and p-MOSFET's has been proposed. Results show that different mechanisms exist for either types of devices. The interface state is dominant for the n-MOSFET degradation, while the channel shortening induced oxide damage is dominant for p-MOSFET. Both are found to be related to the quality of the trench instead of the STI electric field.

6.5 HOT-CARRIER RELIABILITY OF p-MOSFET WITH ULTRA-THIN SILICON NITRIDE GATE DIELECTRIC—I. Polishchuk, Y.-C. Yeo, Q. Lu, T.-J. King, and C. Hu, Univ. of California, Berkeley, CA

Hot-carrier reliability of 0.1 μm p-MOSFET's with 14 Å $T_{OX, EQ}$ silicon nitride gate dielectric was found to be similar to that of SiO_2 p-MOSFET's. The device performance degradation is attributed to the interface traps created by hot holes.

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Time	Event	Room
Sunday		
3:00 p.m. - 9:00 p.m.	Symposium Registration	Hampton Court Assembly
7:00 p.m. - 9:00 p.m.	Companions' Prog. Reg.	Hampton Court Booth
Monday		
7:00 a.m.	Tutorials' Coffee/Danish	Great Hall East/West/Center
7:00 a.m. -5:30 p.m.	Info Tables / Demo Sign Ups	Great Hall East/West/Center
7:00 a.m. - 8:00 p.m.	Symposium Registration	Hampton Court Assembly
8:00 -11:30 a.m.	Tutorial 1	Scotland
8:00 - 9:30 a.m.	Tutorial 2	England
10:00 - 11:30 a.m.	Tutorial 3 – Panel Discussion	England
8:00 - 11:30 a.m.	Tutorial 4	Ireland
8:00 - 11:30 a.m.	Tutorial 5	Great Hall North
12:00 - 5:00 p.m.	Equip. Demonstrations	Exhibit Hall
1:30 -3:00 p.m.	Tutorial 6	Scotland
1:30 - 3:00 p.m.	Tutorial 7	Ireland
1:30 - 3:00 p.m.	Tutorial 8	Great Hall North
3:30 - 5:00 p.m.	Tutorial 9	Scotland
3:30 - 5:00 p.m.	Tutorial 10	Great Hall North
1:30 - 5:00 p.m.	Tutorial 11	England
5:30 p.m. - 7:00 p.m.	Demo Prog. Reception	Exhibit Hall
6:00 p.m. - 8:00 p.m.	Companions' Prog. Reg.	Hampton Court Booth
Tuesday		
7:00 a.m.	Coffee/Danish	Great Hall East/West/Center
7:00 a.m. - 5:30 p.m.	Info Tables / Demo Sign Ups	Great Hall East/West/Center
7:00 a.m. - 2:00 p.m.	Symposium Registration	Hampton Court Assembly
7:30 a.m. - 5:00 p.m.	Equip. Demonstrations	Exhibit Hall
8:00 - noon	Opening/Keynote/Tech. Sess.1	Great Hall North
9:40 - 10:05 a.m.	Coffee Break	Great Hall East/West/Center
2:00 - 5:20 p.m.	Technical Session 2A	Great Hall North
2:00 - 5:45 p.m.	Technical Session 2B–2C	Scotland
3:15 - 3:40 p.m.	Coffee Break	Great Hall East/West/Center
6:00 p.m. - 9:00 p.m.	Poster Session & Reception	England/Ireland
Wednesday		
7:00 a.m.	Coffee/Danish	Great Hall East/West/Center
7:00 a.m. - 5:30 p.m.	Info Tables / Demo Sign Ups	Great Hall East/West/Center
8:00 a.m. - 2:00 p.m.	Symposium Registration	Hampton Court Assembly
7:30 a.m. - 5:00 p.m.	Equip. Demonstrations	Exhibit Hall
8:00 - noon	Technical Session 3A–3B	Great Hall North
8:00 - 12:10 p.m.	Technical Session 3C–3D	Scotland
10:05 - 10:30 a.m.	Coffee Break	Great Hall East/West/Center
12:10 p.m.	Awards Luncheon	England/Ireland
2:00 - 5:45 p.m.	Technical Session 4A–4B	Great Hall North
2:00 - 5:45 p.m.	Technical Session 4C–4D	Scotland
3:15 - 3:40 p.m.	Coffee Break	Great Hall East/West/Center
7:30 p.m. - 9:30 p.m.	Workshops #1 to 10	To be posted on-site
Thursday		
7:00 a.m.	Coffee/Danish	Great Hall East/West/Center
7:00 a.m. - noon	Info Tables / Demo Sign Ups	Great Hall East/West/Center
8:00 a.m. - 2:00 p.m.	Symposium Registration	Hampton Court Assembly
7:30 a.m. - noon	Equip. Demonstrations	Exhibit Hall
8:00 - 10:05 a.m.	Technical Session 5	Great Hall North
10:05 - 10:30 a.m.	Coffee Break	Great Hall East/West/Center
10:30 a.m. - noon	Panel Discussion	Great Hall North
2:00 - 4:05 p.m.	Technical Session 6/Closing	Great Hall North

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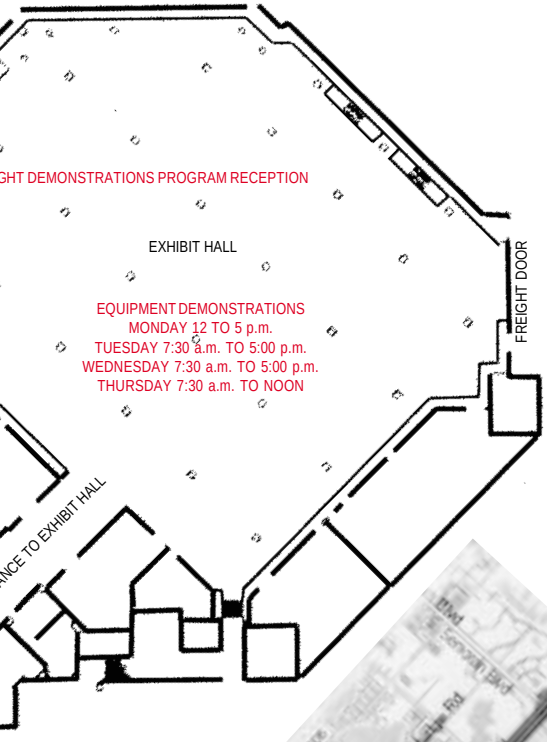
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