IEEE

2000

INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM

http://www.irps.org/

APRIL 10-13, 2000

Fairmont

FAIRMONT HOTEL
170 S. Market Street
SAN JOSE, CA

TELEPHONE: **(408) 998-1900**

FAX: **(408) 527-4727**

Sponsored by

the IEEE Electron Devices Society
and
the IEEE Reliability Society

HIGHLIGHTS* FOR 2000:

Tutorials	Monday	8:00 a.m.-5:00 p.m.
Workshops	Monday	7:30 p.m.-9:30 p.m.
Equipment Demos	Mon.-Thurs.	by Appointment*
Technical Program	Tuesday	8:00 a.m.-6:10 p.m.
"	Wednesday	8:15 a.m.-5:45 p.m.
" **	Thursday	8:15 a.m.-4:45 p.m.
**Oxide Panel	Thursday	10:20 a.m.-noon
Attendees Reception	Tuesday	6:30-9:30 p.m.
Banquet Reception	Wednesday	7:00 p.m.-8:00 p.m.
Awards Banquet	Wednesday	8:00 p.m.

*Read about details in this program

GENERAL INFORMATION

ADVANCE INFORMATION—Avoid delays and extra expense by registering in advance using the form in the center of this program. Mail it with a check or register via fax (315-336-9134) or on-line at www.irps.org/ with a credit card. Advance registration fees apply only to remittances postmarked on or before March 24, 2000. Written cancellation requests will be honored up to March 24, 2000.

SYMPOSIUM REGISTRATION FEES*

	IEEE Member	Non-Member
Advance Registration	$260	$310
Registration at Symposium	$310	$360

TUTORIAL ATTENDANCE FEES**

Advance Tutorial Fee	$210
Door Tutorial Fee	$250

Apply for IEEE membership at ieee.org/join.html. At the Symposium membership application forms will be available near the registration desk also. For additional registration information, see the card in the center of this program or at www.irps.org/.

*Includes copy of Symposium Proceedings (hard copy & cd), workshop attendance, and banquet ticket. Additional banquet tickets may be purchased in advance or on arrival at a cost of $25 per ticket.

** Tutorial fee includes a bound set of notes for all tutorials (including the ones you don't attend). Please register in advance and indicate tutorial selection on your advance registration form so that appropriate room arrangements can be made for each tutorial subject.

REGISTRATION HOURS

The registration desk will be open at the following times:

Sunday, April 9 ..... 3:00 p.m.-9:00 p.m.
Monday, April 10 ..... 7:00 a.m.-8:00 p.m.
Tuesday, April 11 ..... 7:00 a.m.-2:00 p.m.
Wednesday, April 12 ..... 8:00 a.m.-2:00 p.m.
Thursday, April 13 ..... 8:00 a.m.-2:00 p.m.

HOTEL RESERVATIONS

Attendees will make their own reservations using the form in the center of this program. Note that a one-night deposit or a credit-card guarantee is required with your room reservation. Early reservations are strongly recommended.

The Fairmont Hotel must receive your reservation by ***March 10, 2000*** for symposium attendees to get the special single/double rate of $134 for accommodations. When making reservations, refer to "IRPS".

A limited number of rooms is also available at government rates for qualified government employees. Government employees must show identification at hotel check-in to receive the government rates.

SYMPOSIUM PROCEEDINGS (hard copy and cd)

The Proceedings will be provided at the Symposium. Additional copies of the Proceedings can be ordered/purchased from: (1) IRPS Registration using the registration form via on-line, fax, or mail; (2) IRPS Registration at the Symposium; (3) IEEE after April 13 via mail order through the IEEE Service Center, Single Copy Sales Unit, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331. For IEEE Service Center credit card/cash sales call 800-678-IEEE. Request IEEE Catalog No. 00CH37059. A substantial discount will be allowed IEEE members.

PAST PROCEEDINGS/TUTORIALS/VIDEOTAPES—A limited number of past proceedings, past tutorial notes, and previous years' videotape sets will be sold in the Past Publications Booth near the Imperial & Regency Ballrooms. The booth will be open during regular registration hours.

VIDEOTAPES—Orders are being taken for a five volume videotape set of the 2000 paper presentations. Order using the registration form via on-line, fax, mail, or at the Symposium. Please order by April 21.

Jon E. Klema
General Chair

GENERAL CHAIR'S GREETING

Welcome to the 38th annual International Reliability Physics Symposium. The Management and Technical Program committees have prepared three full days of technical offerings and social activities. Come to hone your knowledge and keep up to date on the latest breaking developments.

The activities begin on Monday with tutorials during the day and Workshops in the evening. Tutorials are taught by recognized experts in the field and cover a wide range of topics from fundamental failure mechanisms and failure analysis methods to copper interconnects and low K dielectrics. These subjects are aimed at differing experience levels and offer an opportunity to improve your depth of knowledge in your specific field or to broaden your understanding of related subjects. You choose the options to best suit your needs.

The evening Workshops provide an opportunity to follow up on the morning's topics where users, manufacturers, and academia share ideas in an open and informal setting. This is your chance to speak your mind, to ask some tough questions and to listen to what others find important. The technical sessions of the symposium begin Tuesday morning and run through Thursday afternoon. This is the heart of the symposium - people who are actively involved in the field of reliability share their experiences of the latest developments in materials, methods and technology. See the Technical Program heading of this brochure for more details.

The Equipment Demonstration Program begins Monday at noon and runs through Thursday noon. The demos are a chance for symposium participants to see first hand what the hardware and software suppliers have available to help you improve your organization's product through improvements in measurement and analysis.

Scheduled social events include a Tuesday evening reception and the Wednesday evening awards banquet. You'll find more details under the Arrangements heading in this brochure.

San Jose, the heart of Silicon Valley and the beautiful Fairmont Hotel offer much to enhance your enjoyment. See the Arrangements section for further details on Companions Programs and local attractions.

I am looking forward to seeing you this April in San Jose. Come early to take advantage of the tutorials and stay through Thursday for the fine technical sessions the contributors have prepared.

Jon E. Klema
General Chair

TECHNICAL PROGRAM CHAIR'S WELCOME

William R. Tonti
Technical Program Chair

The Technical Program will showcase 68 papers peer selected from the global microelectronics community and will present the latest findings in reliability physics and engineering. Dr. Tak Ning of IBM Research will open the symposium with a keynote address titled "*Silicon Technology Directions in the New Millennium*".

This year the symposium will have world-renowned experts debate with the audience the following microelectronics issue: "***Is technology scaling limited by oxide reliability***". Please mark your calendar, bring your questions and don't miss out on this event.

Additionally the symposium will include our world class Monday tutorials program, which this year will feature 11 tutorials that provide in-depth presentations of important reliability issues. The Monday night workshops supplement the Technical Program and tutorials and provide an opportunity for informal, in-depth discussions in 10 topic areas. Please be sure to sign up for the workshops using the IRPS web page at http://www.irps.org/ws/.

As introduced last year, the Technical Program remains electronic. The initiative was well received by you the technical community, as over 75% of the total number of abstracts submitted were submitted electronically. Abstracts were received from all over the world and were reviewed by a team of 85 industry and academic experts in reliability engineering and physics. These committee members are all volunteers and their efforts in selecting very high quality papers for the symposium are to be commended. The Technical Program Committee is organized into sub-committees dealing with specific areas of reliability physics. This year's sub-committees focused on traditional favorites at the IRPS such as failure analysis, interconnects, device and process, ESD and latch-up, device dielectrics, and hot carrier aging, as well as newer areas of reliability concern involving plasma process induced damage, Copper/Low-K, and micro-electro-mechanical systems (MEMS), with a renewed emphasis on compound semiconductors. The compound semiconductor session includes an invited paper, introducing the reliability concerns associated with high field operation of Silicon Germanium Heterojunction Bipolar Transistors integrated in a high performance BICMOS technology.

The arrangement of paper sessions within the Technical Program reflects this sub-committee structure.

The Technical Program begins on Tuesday at 8:15 a.m. The following Dielectrics plenary session discusses the latest advances in the reliability physics of thin insulators, and includes an analysis of energy controlled time-to breakdown versus the traditional physics oxide field breakdown. The remainder of the Program has been organized to include sessions consciously arranged to minimize overlap between subject areas. The Tuesday afternoon parallel sessions cover Dielectrics II, Hot Carriers, MEM's and Device and Process I. Hot Carriers covers analytical models useful in the deep sub-micron regime, LDD degradation, analysis of worst case mosfet stress conditions, and width dependencies on HER reliability.

MEM's reliability is a growing field, and this year will topically cover actuators, shock and vibration, and characterization techniques.

The Wednesday morning parallel sessions begin with Device and Process II, and Packaging. Device and process I and II covers many exciting aspects of semiconductor reliability, including moisture effects, antifuse, flash, mosfet, yield correlation, SER susceptibility, metal anneal, Cu/Low-K, and oxide breakdown impact to mosfet operation. The packaging session discusses Analysis and simulation of BGA packages, Lifetime prediction for IGBT modules, stability of hall plates and the effect

temperature cycling has on reliability prediction.

This session concludes with Compound Semiconductors, incorporating an invited SiGe paper, GaAs reliability, and optical fiber sensor reliability.

Wednesday afternoon has parallel sessions in ESD, which has the 1999 best ESREF paper describing ESD smart power reliability, and also includes discussions of protection using today's advanced dielectrics and metal systems. The parallel Interconnect session will contain interesting work on low-k inter level dielectrics, and copper interconnect integration issues.

Thursday reverts back to plenary sessions. The morning includes Process Induced Damage, which investigates various techniques and models to both detect and characterize damage using charge pumping, on-chip probes, and rapid ramp breakdown. The morning continues with the invited Dielectrics panel discussion, and attendee questions.

Thursday afternoon concludes IRPS 2000 with Failure Analysis where advances in defect based testing, novel probing techniques and process contributions to failures are discussed.

William R. Tonti
Technical Program Chair

ARRANGEMENTS INFORMATION

Chair: **Bernie Pietrucha, Lucent Technologies**

Vice Chair: Steve Kirch, Intel

TRANSPORTATION *(see www.irps.org)*

Reduced rates have been arranged with United Airlines and Avis Rent-A Car. Please refer to the back of the program for specific details regarding these air and car rental arrangements. Ground transportation via taxi from the airport to the Fairmont Hotel is also available. Daily parking is available for hotel guests at $11.75 per day and $15.50 per day for non-guests. Local parking facilities are also available within easy walking distances and at lower daily fees. The Fairmont Hotel is located in downtown San Jose adjacent to the "light rail" transportation system. Local attendees may want to consider using this mode of transportation and its remote "Park and Ride" facilities.

CONFERENCE ACTIVITIES

Registration, tutorials, workshops, and tutorials will be held on the Ballroom level of the hotel. Equipment Demonstrations will be held in Parkside Exhibit Hall across Plaza de Cesar Chavez from the hotel. See the following page for details on the Demos and consult the map at the back of this Program for directions to the Parkside Exhibit Hall. The Demo Sign-Up/Coffee Sponsors/Break area is in the foyer of the Ballroom (Pre-function area) toward the front of the hotel.

COMPANIONS' PROGRAM

The IRPS, is again, pleased to offer a Companions' Tour Program. In addition there will be a Hospitality Suite, for spouses and guests of IRPS attendees, open Monday through Thursday, 8:00 a.m. to 10:00 a.m.. For more information on the Companions' Program please contact Sandy Barber, P.O. Box 2098, Banner Elk, NC 28604-2098, or phone 828-898-6375 (Monday through Friday, 10:00 a.m. to 4:30 p.m. EST), or send an Email to: sandyirps@aol.com.

FITNESS CENTER

The Fairmont Hotel offers health club facilities for a nominal daily charge. The facility is located on the third floor of the hotel. There is also an outdoor swimming pool for guests, located on the fourth floor.

TUESDAY EVENING RECEPTION

This year the Tuesday event will be held at The Tech Museum of Innovation which is located within short walking distance directly across Plaza de Cesar Chavez from the hotel. Attendees will long remember designing their own roller coaster and test driving it using 3-D simulation software, or maneuvering a remotely-operated vehicle through a 7700 gallon water-

filled tank. Galleries include Communication: Global Connections, Innovation: Silicon Valley and Beyond, Exploration: New Frontiers, and Life Tech: The Human Machine. A light buffet will be provided for Symposium attendees and their guests.

WEDNESDAY EVENING SYMPOSIUM BANQUET

The Symposium Awards Banquet will be held on Wednesday, April 12, at 8:00 p.m. in the Fairmont Hotel Regency Ballroom. A no-host reception prior to the Banquet will run from 7:00 p.m. to 8:00 p.m. in the Ballroom foyer. Awards for 1999 IRPS Best and Outstanding Papers will be presented immediately following dinner. Registered attendees for the Symposium will receive one ticket for admission to the banquet. Additional tickets may be purchased at the Registration Desk for $25.

EQUIPMENT DEMONSTRATIONS

Chair: **Shekhar D. Khandekar, Level One Comm.–Intel**
Vice Chair: Thomas L. Polgreen, ESD Solutions

The Equipment Demonstration program of the IRPS focuses on providing attendees with an opportunity to learn about reliability software and equipment in a confidential, "hands-on" fashion. Unlike typical trade events, sales pressures are minimized, and manufacturers are prepared to help attendees learn about, and test their latest equipment and software developments. Attendees are strongly encouraged to contact the demonstrators prior to the conference, and to make arrangements to bring their own samples, if desired. The following abstracts provide an overview of the nature of each company's demonstration, along with contact information. The **www.irps.org** web site will contain the latest information as more demonstrators are added to the program.

Demonstrators and other companies providing a variety of reliability physics products and services are also represented in the coffee break area. There, they will provide information on their products and sign-up sheets for demonstrations. You can sign-up for demonstrations at any time during the conference. This service is included in your registration and you can sign-up for as many demonstrations as you like, on a first-come, first-serve basis. *So there is really no better way to evaluate so many state-of-the-art systems, and to collect so much information on services, latest equipment, and software developments …than to participate in* ***IRPS Demos****!*

The coffee break area is located adjacent to the Technical Program and the demonstration area is in Parkside Exhibit Hall across Plaza de Cesar Chavez from the hotel. Hours for equipment demonstrations are as follows:

Monday, April 10:	Noon - 5:00 p.m.
Tuesday, April 11:	7:30 a.m. - 5:00 p.m.
Wednesday, April 12:	7:30 a.m. - 5:00 p.m.
Thursday, April 13:	7:30 a.m. - Noon

DEMONSTRATORS (as of January 24)

Demo#1: COPPER AND ALUMINUM RELIABILITY TEST SYSTEMS FOR PACKAGE LEVEL AND CONVENTIONAL WAFER LEVEL TESTING—Aetruim Inc., Randy Snede; Tel: 651-704-1800; Fax: 651-704-0339; www.aetrium.com

Our revolutionary Model 1164 Reliability Test System has a massively parallel architecture that allows you to run many tests at many temperatures simultaneously. You can configure each system for any mix of Copper and Aluminum Electromigration and TDDB, MOS Hot Carrier, plus a NEW capability to test high power devices addressing RF Life-test applications. NEW custom-designed DUT fixtures and ovens test above 350°C without corrosion or contact relaxation for long term measurement reliability. Modularity improves throughput, eliminates scanning, and maintains high performance, flexibility, and low cost. Full-featured software easily provides powerful analysis for lifetime predictions.

Demo#2: COMPLETE PREDICTIVE WAFER LEVEL RELIABILITY SOLUTIONS—Agilent Technologies (A subsidiary of HP), Jay Thomas; Tel: 408-553-2212; www.agilent.com

Agilent's fast PDQ-WLR solution is the choice for more and more companies to develop, qualify and monitor their process reliability. For example, customers have reduced COPPER and LOW-K development tests from two months to two days—all while maintaining agreement with traditional tests. As part of a complete solution, revolutionary integrated analysis makes sure you spend even less time getting the answers you need. Agilent also introduces a new multi-site wafer level hot carrier stressing system based on the 4156B Semiconductor Parameter Analyzer. Features include simple front panel control and innovative prober card cabling for fA level measurement integrity.

Demo#3: PORTABLE EMISSION MICROSCOPE—Alpha Innotech, Tracy Mettier; Tel: 510-483-9620 Fax: 510-483-3551; www.alphainnotech.com

Alpha Innotech will demonstrate our Portable Emission Microscope, which easily interfaces to probestation, testhead, and overhead wafer sort, including our patented VibeCoupler ™ for elimination of 100x image jitter. Attendees can perform hands-on imaging of their samples. Portable Emission Microscopy brings the photoemission tool to the problem, accelerating root cause determination.

Demo#4: ESD TEST EQUIPMENT—Barth Electronics, Jon Barth; Tel: 702-293-1576; Fax: 702-293-7024; email: jonbarth@aol.com; http://users.aol.com/jonbarth

The Barth Model 4002 TLP electrical inspection tool for ESD protection structures will be available to measure the complete I/V characteristics on your wafer or packaged part. This test method allows a silicon circuit designer to measure the electrical characteristics curve with the first commercial TLP Pulse Curve Tracer. Bring your ESD protection structure for testing and get an insight into its electrical operation, or see how closely it matches its planned protection objective.

Demo #5: OXIDE AND HOT CARRIER TESTING AND SIMULATION—BTA Technology, Inc., Karolien Cools, Tel: 408-451-1210; Fax: 408-451-1211; www.btat.com

BTA Technology will demonstrate 1) hot carrier analysis software suite, BTABERT, RelPro+ and BSIMPro, which can help design and reliability engineers analyze hot carrier impact on circuit performance and push for design performance and 2) TDDB and Burn-In simulation software, TDDBWorks. We will also demonstrate BTA9812A and NoisePro, automatic wafer level 1/f noise characterization system with hot carrier stress and TDDB testing function, which can quantify hot carrier and TDDB impact on 1/f noise characteristics of devices automatically.

Demo #6: AUTOMATIC & SEMI-AUTOMATIC PROBERS—Cascade Microtech, Daniel Harris; Tel: 503-601-1000; 800-854-8400; Fax: 503-601-1601; www.cmicro.com

Cascade Microtech will demonstrate their PS21 parametric autoprober with eight inch capacity, 25 wafer cassette, femtoAmp level 48-pin probe card interface, & -55 to 200 °C guarded thermal chuck with <5 picoFarad capacitance. In addition, the Summit series semi-automatic analytical probe stations offer fast transition, -65 to 300 degree thermal chucks optimized for all WLR disciplines. Included in the series is the Summit 12861 for DC/CV characterization featuring the patented AttoGuard™ thermal system with < 1 picoFarad chuck capacitance, 3 femtoFarad chuck variation, < 20 femtoAmp noise & leakage, & 50 milliSecond recovery time from a 100 Volt pulse.

Demo #7: PACKAGE LEVEL RELIABILITY TEST SOLUTIONS—Cottonwood Technology Group, Inc., Judy Longhurst, 480-970-3333; 480-970-3322; www.ctgi.com

Cottonwood Technology Group offers package level reliability solutions for: (1) Power Cycle Testing, (2) Temperature and Humidity Testing,

(3) In-situational Thermal Stress Testing. We willshow how our solutions help quality and reliability engineers achieve greater effectiveness in their work by: (1) Decreasing test set up time from days to hours, (2) Reducing problem isolation time from weeks to hours, (3) Employing closed loop control to provide extremely accurate stresses, (4) Allowing trend data analysis while the stress is running. Metrics Technology will also be present to discuss their new WLR solutions as well as the joint application developed with Cottonwood to perform I-V and C-V measurements and analysis for design verification, process troubleshooting, reliability engineering and failure analysis.

Demo#8: TEST SYSTEMS THAT PERFORM HIGH RESOLUTION *IN-SITU* MEASUREMENTS—Destin, Luc Tielemans; Tel: 32-11-21 -4636; Fax: 32-11-21-4626

Destin test systems perform high resolution *in-situ* measurements to monitor the degradation of test samples. This technique allows the performance of reliability tests in short test times (typically a few days to a week) at low stresses. This will be demonstrated for both electromigration and thermal degradation of packages. The software package "Failure" is a powerful tool to analyze reliability data. This program allows the prediction of lifetime and calculates the uncertainty of the prediction. The IDDQ failure analysis test system is a helpful tool to locate failures with the aid of liquid crystals or emission microscopes.

Demo#9: BEST RANGE APPLICATIONS FOR SERIOUS INVESTIGATORS OF RELIABILITY PHYSICS—Digital Instruments, Veeco Metrology Group, Marlene Carlyle; Tel: 805-967-1400; Fax: 805-967-7717.

Digital Instruments will demonstrate the Dimension 3100 scanning probe microscope (SPM) system. The applications include electrical applications modules for: Scanning Capacitance Microscopy (SCM) allowing the user unprecedented imaging resolution of electron device structure & operation through 2 & 3D dopant metrology. Scanning Spreading Resistance Microscopy (SSRM) permits high sensitivity nanometer resolution of resistivity in semiconductors. Tunneling AFM (TUNA) gives a 2D map of gate oxide thickness & integrity for dielectric characterization Each of these & other techniques such as Scanning Thermal Microscopy (SThM) & Electric force Microscopy (EFM) provide unique material & device property characterization & failure analysis on a nanometer scale, without requiring vacuum & in a manner that is non-destructive to the samples. You are encouraged to bring samples to image.

Demo#10: SEMICONDUCTOR FAILURE ANALYSIS SYSTEM—Hamamatsu Photonic Systems, Mary L. Boyle; Tel: 908-231-1116; Fax: 908-231-0852; mboyle@hamamatsu.com

Hamamatsu will demonstrate the µAmos-200. The µAmos is a semiconductor failure analyzer that utilizes a revolutionary new IR-OBIRCH (InfaRed Optical Beam Induced Resistance Change) method for localization of leakage current path. µAmos also observes the abnormal resistance of contacts (via contacts) in LSI devices. Hamamatsu will also introduce the PHEMOS-1000 an IR Confocal Laser Scanning Emission Microscopy system.

Demo#11: BACKSIDE EMISSION MICROSCOPY: CHIP UNZIP BACKSIDE WAFER PREPARATION SYSTEM—Hypervision Inc., Dan Hurley; Tel: 510-651-7768; Fax: 510-651-1415; www.hypervisioninc.com

The patented Chip UnZip™ hardware process safely thins semiconductor die for backside inspection of wafers and packages. It allows the BEAMS emission microscope to inspect devices and wafers from the backside. The proprietary SmartCam™ 3-D software interface program automatically creates code to control both the CAD software and the CNC mill.

Demo#12: EMISSION and ATOMIC FORCE MICROSCOPY, 300 mm WAFERS, LOW NOISE TESTING—Karl Suss America, Inc., Paige Lowry, Tel: 802-244-5181; Fax 802-244-5103; www.suss.com

Karl Suss will be exhibiting the world's first Real-Time Probe which can see and test devices below 0.25 microns. Karl Suss and Micron Force Instruments have partnered to develop a Real-Time, contact probe that utilizes the unique advantages of Atomic Force Microscopy (AFM). In addition, the SUSS display will include new, innovative probing solutions relating to emission microscopy, low current/low noise temperature testing, and 300 mm applications. The SUSS Probeshield system overcomes issues relating to mechanical infringements with microscope and probe arm movements, as well as, providing a true, frost free environment.

Demo#13: FAILURE MECHANISM MODELING TESTS ON WAFERS–Keithley Instruments, Tim Turner; Tel: 440-498-2874; Fax: 440-498-2911; www.keithley.com

Keithley Instruments will demonstrate equipment for the performance of Failure Mechanism Modeling tests on Wafers and for Fast Process Reliability Monitoring. The equipment showcases advanced low current measurement capability (10^{-17} Amps) and a complete system including instruments, prober and advanced multisite probe card.

Demo #14: AUTOMATIC ESD AND LATCHUP TESTERS—KeyTek, Kim Baltier; Tel: 978-275-0800; Fax: 978-275-0850; www.keytek.com

KeyTek will demonstrate two testers: (1) PARAGON, an advanced ESD and latch-up test system for testing from 256 to 1024 pin systems (2) RCDM, a Robotic CDM ESD test system. Attendees may also operate the equipment themselves, and time permitting, to perform ESD tests on one or two of their own devices. (Prior arrangements should be made to ensure appropriate DUT boards are available.)

Demo#15: FULL SCALE SCHEMATIC TOOLS PACKAGE FOR FA—Knights Technology, Scott Shen, Tel: 408-522-8880; Fax: 408-739-4438; email: sshen@knights.com; www.electroglas.com

Merlin's Framework, the industry standard CAD Nav software product will be shown with it's new features, branches, and versions. Among them, a package of full-scale schematic tools is ready for failure analysis. KEDIT and Image Overlay options are helping FA engineers. PC version of Merlin software is available now. FA Wizard is the on-line documentation for all level of FA people, and its' Web version is available now. LogicMap is the new Fault Localization tool for the logic designs. After all above, a new generation of Merlin, Merlin 2000, is ready to demonstrate its' architectures.

Demo #16: DATA ANALYSIS TOOLS AND PROCESS EVALUATION TEST SYSTEMS—Micro Instrument Co., Curt Haas: Tel: 760-746-2010; Fax: 760-746-0433; www.microinstrument.com

Micro Instrument Company will provide a hands-on demonstration of new testing capabilities in our (NEW) SPC4000 test system for electromigration and TDDB. Our (NEW) CH4000 chamber has capability for both aluminum and copper testing with temperatures in the 70 °C to 450 °C Range. Coupled with our new high resolution Instrumentation for Electromigration and TDDB the system provides an ideal test platform. New test software allows our existing and new instrumentation to operate within the same environment. Multi-Lead capability of our new DM610 instrumentation can perform TDDB, and some Hot Carrier tests. See our upgraded PE9010A for Hot Carrier testing and a PE9020A for small lot, multiple temperature, testing to 350 °C.

Demo#17: VERSATILE EOS/ESD SUSCEPTIBILITY TEST INSTRUMENTS—Oryx Instruments, Casandra Goguen, Tel: 510-249-1144; Fax: 510-249-1150; www.oryxinstruments.com

Oryx Instruments offers the most comprehensive, affordable line of ESD Test Systems and Latch-Up. Capabilities include: Manual and Automated systems, pin counts from 64 to 2016, package and wafer level test support, ESD - Human Body model, Machine Model, ESD - Charged Device Model, Transmission Line Pulsing, JEDEC 78 Latch-Up, Transient Latch-Up.

Demo#18: TURN-KEY SEMICONDUCTOR RELIABILITY TEST—QualiTau, Tom Bensing; Tel: 408-522-9200; Fax: 408-522-8110; www.qualitau.com

QualiTau will exhibit various turn-key semiconductor reliability test solutions for performing electromigration, dielectric breakdown, & hot carrier degradation testing for package & wafer level, featuring various plug-in modules & complete analysis software. Featured systems are the MIRA, INFINITY, ACE & a multiple die probing system. In addition to the various test applications available on the MIRA, also featured will be the latest design of our High temperature DUT boards & our new 450 °C oven system & a current source for every DUT. The state-of–the-art INFINITY system features capability for package level & wafer level TDDB testing with an independent SMU for each DUT.

Demo#19: SAGITTA NEXT-1 EXACT X-SECTIONING TOOL—Sagitta. LTD, Tony Ruffini; Tel: 408-390-3066; Fax: 503-961-9403; www.sagitta-usa.com

Sagitta has introduced a new concept of automating sample preparation for SEM & TEM analysis using polishing technology, advanced image processing, and process control. This allows sample preparation with high success rates and accuracy regardless of operator experience. The advanced control and machine vision enables to 0.1 micron accuracy at higher than 90% success rates with an unattended process. The latest software developments allow SEM and TEM sample preparation on the same system with greater ease of use. Attendees will have hands-on involvement in the preparation of their samples. Sagitta encourages customers to bring their own samples for precise cross-sectioning.

Demo#20: WAVEFORM MEASUREMENT RESULTS OBTAINED ON AN OPTICAL PROBING SYSTEM—Schlumberger Test & Transactions, Trina Santos; Tel: 408-453-3684; Fax: 408-437-5375; www.slb.com/ate

An innovative technology incorporating a laser beam has recently been developed by Schlumberger that probes through silicon and detects voltage swings directly on the active regions of transistors in CMOS ICs. Schlumberger will present waveform measurement results, user interface and system technology and hardware overview. Analog and Mixed Signal device products are developed faster with the new Schlumberger Analog Measurement System (AMS). Not only does the AMS provide multiple FIB chemistries for probepoint but also provides <10 mm resolution for precision probe placement in the dense geometries of 0.18 micron process technologies.

Demo#21: SCANNING ACOUSTIC MICROSCOPY WITH HIGH RESOLUTION—Sonix Inc., Jim Stradling; Tel: 703-440-0222; Fax: 703-440-9512; www.sonix.com

Sonix will demonstrate the state of the art in Scanning Acoustic Microscopy –the UHR2000 Ultra High Resolution SAM with advanced TAMI imaging capability and the ICEBERG offline analysis package. TAMI allows the operator to generate multiple focused C-scan images (slices) of the sample in one scan. ICEBERG offers unparalleled analysis capabilities since all the RF data is stored. Unlimited A-, B- and C- scans can then be generated off line. C-scans can also be generated from frequency domain information (FFTs) rather than the time domain. Attendees (up to four per hour) are invited to bring their IC packages and see them in a different light.

Demo#22: NEW VISUAL ACOUSTICS™ OPERATING SOFTWARE BASED ON TRUE WINDOWS NT OPERATING SYSTEM—Sonoscan, Inc., Donald L. Commare; Tel: 847-437-6400; Fax: 847-437-1550; email: info@sonoscan.com; www.sonoscan.com

Sonoscan's new D9000 and D24 series of digital C-SAM ® Acoustic Microscopes features faster and more accurate scanning and are equipped with pulse/receivers having 500 MHz bandwidth. Sonoscan also offers a complete family of 230 MHz transducers (currently 6 different designs) optimized for a variety of applications including the inspection of flip

chips. The D9000 & D24 feature Very High-Res™ scanning, which produces images with up to 8192 x 7680 data points. Sonoscan's new Visual Acoustics™ operating software, based on a true Windows® NT operating system, is extremely simple and intuitive to use. New features within Visual Acoustics Operating Software include Zip Slice™, 3V™, & C-SAM Interactive™.

Demo #23: LOW NOISE, LOW CURRENT ANALYTICAL PROBING—The Micromanipulator Co., Karen Schanhals; 775-882-2400; Fax: 775-882-7694; www.micromanipulator.com

Probe at resolutions up to 0.05 microns using Micromanipulator's 8860 semi-automatic analytical test stations. Learn how to probe at very low femtoamp levels (less than 10 fA range) & at elevated temperature using triaxial probes, triaxial chucks, integrated shielding and unique high-stability probes. Discussions & examples of incorrect test setups & common errors that can introduce unwanted leakage, electrical and/or physical noise into probing measurements, and practical solutions to these problems will be presented.

Demo#24: ELECTRICAL CHARACTERIZATION OF INTEGRATED CIRCUITS FOR FAILURE ANALYSIS—UltraTest International, Bob Herriford; Tel: 408-433-2244; Fax: 408-433-5508; www.ultratest.com

UltraTest will demonstrate their new MegaTrace DC Parametric Test System and Automated Digital Curve Tracer. The system is capable of testing devices up to 2,160 pins. Basic curve trace concepts, techniques and interpretation of waveform results will be discussed. Also demonstrated will be the system's capability to perform DC parametric testing, logical pre-conditioning, CMOS Latch-up testing with up to 50A capability and new "curve compare" software. UTI will introduce several new software features and significant improvements in the system's "vectoring" capability, including IDDQ.

ADDITIONAL COFFEE BREAK SPONSORS

- Accurel Systems
- B&G Enterprises
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- Cody Electronics
- CR Technology
- FEI Company
- IBM Analytical Services
- LEO Electron Microscopy, Inc.
- Micro Control Company
- Reedholm
- SELA-USA,Inc.
- Sandia National Laboratories
- TPEC
- Viko Test Lab – ADEC

TUTORIAL PROGRAM

Chair: **Edward I. Cole, Jr. Sandia National Laboratories**

Vice Chair: Thomas M. Moore, Texas Instruments

The 2000 IRPS Tutorials Program offers attendees the opportunity for focused instruction in core topics as well as emerging areas of interest in reliability physics. For those who are new to the field of reliability, the Tutorials Program provides an excellent background and preparation for the symposium by learning from the experts. Experienced engineers benefit from hearing of new developments, exchanging technical viewpoints, and broadening of their technical skills.

Core topics for 2000 include gate oxide reliability, hot carrier fundamentals, and product reliability qualification. In response to last year's survey feedback, a set of 4 tutorials dealing with different reliability aspects of Cu metallizaiton and low dielectric constant materials is a major theme for this year. In addition to these topics, focused ion beam basics and developments, design for safety-critical applications, challenges in packaging and assembly, and wet etches for failure analysis are available for participants.

The Tutorial Program is a great value for IRPS attendees and far more economical than bringing experts to your location. With you registration you will receive a copy of the Tutorial Notes which includes the abstracts

and viewgraphs of all the offered courses (over 20 hours of reference material!). To facilitate meeting room planning your are encouraged to register early and indicate your intended attendance choices on the registration card.

Monday April 10, 2000

Room	8:00 a.m. to 9:30	10:00 to 11:30	1:30 to 3:00	3:30 to 5:00 p.m.
Imperial Ballroom	Topic 1		Topic 11	
Regency Ballroom I	Topic 2	Topic 3	Topic 9	Topic 10
Crystal Room	Topic 4	Topic 5		
Regency Ballroom II	Topic 6		Topic 7	Topic 8

Topic 1. THIN GATE OXIDE RELIABILITY: PAST AND PRESENT TRENDS IN CHARACTERIZATION, PHYSICAL MODELING, AND ASSESSMENT - J.S. Suehle and E.M. Vogel, NIST, Gaithersburg, MD *(8:00 a.m. - 11:30 a.m., Imperial Ballroom)*

The reliability of gate oxides has become a critical concern as oxide thickness is scaled below 3 nm in advanced technologies. It has been proposed that the fundamental limit to further device scaling is the intrinsic reliability of the gate dielectric. An overview of past and present thin oxide reliability characterization techniques and wear-out physics will be presented. A special emphasis will be placed on issues relating to the characterizing and understanding of breakdown in current technology ultra-thin gate oxides where excessive tunneling currents and soft breakdown complicate reliability assessment.

Topic 2. LOW-DIELECTRIC CONSTANT MATERIALS FOR Cu INTERCONNECTS - K. Taylor, Texas Instruments, Dallas TX *(8:00 a.m. - 9:30 a.m., Regency Ballroom I)*

The demands of lower power consumption, faster speed, and reduced crosstalk continue to pressure semiconductor companies to replace SiO_2 with a low-dielectric-constant material as the intermetal dielectric. An overview is given of low-dielectric-constant materials and several ways of being incorporated into copper-based metallization schemes. This will include various methods of deposition as well as subsequent physical and electrical characterization. This course would be suitable for technologists who have limited experience in working with low-dielectric-constant materials but have strong traditional backgrounds in CVD/SOG/PVD dielectric and metallization technology.

Topic 3. RELIABILITY CONSIDERATIONS FOR Cu METALLIZATION SYSTEMS FOR ULSI CIRCUITS, T.D. Sullivan and A.K. Stamper, IBM Microelectronics, Essex Junction, VT *(10:00 a.m. - 11:30 a.m., Regency Ballroom I)*

The drive toward smaller, faster microelectronics chips is requiring use of Cu and low-K dielectrics in place of present Al/SiO_2 wiring systems in order to reduce RC signal delay. Cu addresses the resistive component of this delay. Besides having 30% lower resistivity and a higher elastic modulus compared to Al, Cu is a relatively low-cost replacement. But Cu behaves differently from Al in several ways. Cu is not self-passivating like Al, and has been found to diffuse through oxide. Diffusion barriers must therefore be used around Cu lines to protect active devices from Cu poisoning. Because Cu oxidizes easily, wiring and bond pads must be protected from air during high-temperature testing. Cu adhesion to SiO_2 appears to be poorer and Cu interfacial diffusion higher, allowing for significant electrochemical migration and a different dependence of electromigration lifetime on linewidth than that seen with Al. For electromigration and stress voiding, Cu is generally more robust than Al. However, fabrication details can substantially modulate this behavior if not carefully controlled. Introduction of low-K dielectrics, anticipated to

address the capacitive component of signal delay, will present additional challenges for both integration and reliability, because most low-K materials have lower mechanical strength, lower thermal conductivity, and are more permeable than SiO_2.

Topic 4. HOT CARRIER RELIABILITY FUNDAMENTALS IN LOGIC AND MEMORY TECHNOLOGY- P. Fang, AMD, Sunnyvale, CA *(8:00 a.m. - 9:30 a.m., Crystal Room)*

The fundamentals of the hot carrier effects for both logic and flash memory technologies will be reviewed and discussed in this tutorial. The temperature effects for low sub-1.5 Vcc operation and different gate oxide nitridation and D2 anneals on hot carrier reliability will be presented. The DC-AC hot carrier lifetime projection methodology and the criteria evolution are also highlighted. The basic flash memory operation configurations and respective reliability concerns will be introduced.

Topic 5. ASIC DESIGN FOR SAFETY-CRITICAL APPLICATIONS-T. Ambler, University of Texas Austin, Austin Texas *(10:00 a.m. - 11:30 a.m., Crystal Room)*

The requirement for highly reliable integrated circuits in safety-critical applications is increasing. The transportation industry, for example, uses increasing amounts of electronic control in life-critical situations, the nuclear industry uses electronics in reactor protection systems. This presentation will discuss the problems and some of the solutions to the difficulties posed in attaining verifiably high reliability in modern integrated circuit design.

Topic 6. FOCUSED ION BEAM TECHNOLOGY AND APPLICATIONS TO MICROELECTRONICS - M.T. Abramo, IBM Microelectronics, Burlington, VT and A.N. Campbell, Sandia National Laboratories, Albuquerque, NM *(8:00 a.m. - 11:30 a.m., Regency Ballroom II)*

During the past decade, focused ion beam (FIB) systems have become indispensable tools in the arsenal of analytical techniques available to failure analysts and IC designers. FIB systems are similar to scanning electron microscopes (SEM) in that a charged particle beam is generated, raster-scanned, and used for high resolution imaging. In addition, the use of massive Ga ions permits the FIB system to be used for both material removal (milling) and deposition, enabling applications such as precision cross sectioning and chip repair. This tutorial will explore the fundamentals of FIB system operation, describe a wide range of applications, and discuss FIB approaches for chip repair and failure analysis from the back side of the chip. The effects of FIB exposure on transistor parameters and the reliability of FIB-modified ICs will also be discussed.

Topic 7. WET ETCHES FOR SILICON SEMICONDUCTOR FAILURE ANALYSIS - T.W. Lee, Varian, Tempe, AZ *(1:30 p.m. - 3:00 p.m., Regency Ballroom II)*

Wet etches are required in FA for the selective removal, delineation by decoration or differential etching and identification of damage or defects in layers of various materials. Many etch recipes have been formulated to address specific manufacturing tasks. This tutorial contains the results of a literature search on etches such as Dash, Sirtl, Wright and 25 others. Classical and named wet etches are described according to general type and applicability to FA with a ternary diagram, 3-D surface, and spreadsheets. The work of the original researchers is identified in an extensive list of references.

Topic 8. Analytical Challenges in Packaging and Assembly – G. Samuelson, R. Dias, D. Goyal, S. Tandon, Intel, Chandler, AZ, T.M. Moore, C. Hartfield, Texas Instruments, Dallas, TX *(3:30 p.m. - 5:00 p.m., Regency Ballroom II)*

The challenges in assembly analytical tool/technique development are in the areas of nondestructive imaging, board level fault isolation and materials property measurement. This tutorial will deal with tools/techniques in each of these major areas. The pros and cons of state of the

art analytical capabilities will be discussed along with likely future directions. Finally, major obstacles to evolution of existing technologies will be highlighted urging industry participation to engage multiple industry/academic partners for development of breakthrough technology roadmaps.

Topic 9. ANALYSIS OF Cu WITH VARIOUS LOW K DIELECTRIC MATERIALS TO DETERMINE A VIABLE Cu-LOW K DIELECTRIC CANDIDATE FOR ADVANCED INTERCONNECT TECHNOLOGY – S.U. Kim, Consultant, Rio Rancho, NM *(1:30 p.m. - 3:00 p.m., Regency Ballroom I)*

This tutorial focuses on analysis and characterization techniques to determine the new failure mechanisms for the Cu-low k system. It includes inter- and intra-Cu line to line leakage current using a new test structure design, thermal stability and B-T (bias-temperature) stress methodology, identification of Cu damascene process induced defect, root cause analysis techniques, high frequency (GHZ) dependent dielectric degradation such as fatigue, hysteresis, and polarization, and carrier conduction and failure mechanisms. The tutorial material is based on the work performed at SEMATECH and UT, Austin on Cu with various low k dielectric combinations to determine a viable Cu-low k dielectric candidate for advanced ULSI interconnect technology. Data on Cu-low k process induced defects, impact of such defect on thermal stability and B-T stress failure, and new carrier conduction failure mechanisms will be presented and discussed.

Topic 10. THERMAL DEFORMATION AND INTERFACIAL ADHESION IN AREA-ARRAY PACKAGES FOR Cu/LOW-K CHIPS - P. S. Ho, University of Texas *(3:30 p.m. - 5:00 p.m., Regency Ballroom I)*

This presentation will first discuss the thermal deformation behavior in high-density area-array packages with an underfilled flip-chip configuration. The effect of replacing Al oxide interconnects with Cu low k interconnects on packaging reliability will be discussed, emphasizing the difference in thermomechanical properties between oxide and low k materials. Interfacial adhesion has emerged to become a critical concern for packaging reliability. The measurement of adhesion and its impact on reliability will be discussed.

Topic 11. PRODUCT RELIABILITY ASSESSMENT AND QUALIFICATION METHODOLOGIES: CURRENT PRACTICES AND FUTURE TRENDS - N.E. Lycoudes, Motorola Semiconductor Products Sector, Chandler, AZ *(1:30 p.m. - 5:00 p.m., Imperial Ballroom)*

Product Reliability Assessment and Qualification methodologies such as Stress Test Driven, Process Based etc. are reviewed with respect to their current usage and a brief historical perspective is given. New industry proposals such as Application Specific, Use Condition Based, Knowledge Based, Innovation Process Based, Virtual Qualification etc. are reviewed and related to current practices. It is emphasized that in all cases the objective of Reliability Assessment and Qualification is the identification and estimation of the probability of occurrence of potential failure mechanisms during the life of the product under normal use conditions. An existing challenge is restated that NO PRODUCT QUALIFICATION IS NEEDED if the product potential failure mechanisms and their probabilities of occurrence are known. Examples of such cases will be given. The evolution of alternative Reliability Assessment and Qualification methodologies (future trends) are examined within the framework of industry current practices and new proposals.

WORKSHOPS—Monday, April 10

Workshops #1 to #10: 7:30 p.m. - 9:30 p.m.

Chair: **A.G. Rawers, Quicklogic, (rawers@quicklogic.com)**

Vice Chair: M.T. Abramo, IBM (mabramo@us.ibm.com)

Ten workshops covering important topics in reliability physics are available to all symposium registrants. Moderators will discuss topics of current interest & attendees are asked to participate, and share their thoughts. Topics of discussion and hot issues that attendee's would like to have addressed can be forwarded to the moderators prior to the actual workshop. Send your requests, prepare questions or better yet, bring data on the related topics you wish to discuss. Send your requests or post data and questions via the IRPS website at www.irps.org/ws.

Overhead projectors will be available in the meeting rooms. Please note that the workshops will be held on Monday evening after the tutorials. Please register for the workshop of your choice either on-line , use the form below, or alternately when you register at the conference. Topics and sign-up forms are listed below. For further information on the workshop program contact either Arthur Rawers or Marsha Abramo.

• Workshop 1: **New Packages Technologies**

Advanced semiconductor packaging solutions continue to evolve and to satisfy the variety of reliability and performance requirements, new materials are developed and traditional materials are pushed to performance limits. Come and discuss the challenges you are facing in this complex field. Topics sure to be addressed are delamination and cracking, inter-level dielectric performance issues, solder joint reliability assessment strategies, thermal performance of materials, new material applications, etc.

• Workshop 2: **Focused Ion Beam**

The FIB workshop brings together FIB practitioners to share their experience and those who are new to the field and want to become familiar with the diverse aspects of FIB techniques.

Topics to be discussed include, but are not limited to, the challenges of high aspect ratio contact hole preparation and filling, back side device processing, the challenge of coping with metal fill patterns, design for repairability, is there reliability in FIB micro surgery?, CAD layout overlay, repair site navigation on deep submicron ICs.

• Workshop 3: **Standards for Product Qualification**

This workshop will discuss the practices for product Qualification and address the related topic of product reliability screening tests. There are a variety of qualification methods, specifications and requirements that exist in our industry today. Which are the best ones? Which methods are more effective than others.? How does product reliability assessment differ from qualification testing? Come here what others have to say or come and express your opinion about your favorite tests.

• Workshop 4: **Dielectrics**

Planning and execution for dielectric reliability data requires a discipline to ensure timely and meaningful information. It is a labor and time intensive effort in which, perhaps, one gets only one chance to make it work, and there is never enough time. This workshop will concentrate on these issues as they relate to: processing conditions, model for voltage (or field) and temperature, area dependence, process/device layout sensitivities (area vs perimeter, etc.), and DC vs transient conditions. Discussions will address topics like planning for dielectric data acquisition, advice on methods to analyze the data for maximum information, and how to handle potential conclusions based on available data.

• Workshop 5: **Hot Carriers**

Hot Carrier (HC) reliability requirements are starting to become a limiting factor for the development of deep submicron technologies (< 0.25 nm). Global HC reliability rules, extensively used in the past, are starting to impact the performance/reliability tradeoffs to not acceptable levels . It is becoming more and more important to carefully quantify the link between

DC HC studies and circuit reliability/performance requirements. This workshop will focus on possible methodologies to quantify circuit level reliability at very early stage in the technology development cycle. The main discussion will be on existing software tools to allow HC reliability by design, their limits and future developments to satisfy the needs of both reliability and circuit design. New stress/test methodologies to optimize and calibrate the reliability projections by simulation will be also covered.

• Workshop 6: **ESD/Latchup for High Performance CMOS**

ESD continues to be a major reliability threat as technologies advance further into the deep submicron regime and IC designs get more complex. This workshop will address the latest concerns for ESD including: 1) core damage, 2) new latchup issues and the tradeoff with ESD, 3) new packaging and processes, 4) building-in ESD reliability, 5) mixed voltage circuits, 6) Charged Device Model, 7) oxide reliability and charge trapping, 8) simulation and modeling efforts to solve ESD, 8) ESD testing standards, and 9) any other topics of interest to the audience.

• Workshop 7: **Failure Analysis**

This highly popular workshop will focus on recent developments in the field of failure analysis. A discussion of techniques orientated at the analysis of current and next generation processes will focus on methods of fault localization and isolation. The challenges of flip chip and back-side techniques could also be addressed. Its all up to those who attend and the discussions that evolve. Attendees are encouraged to prepare questions and presentation material on those issues that they would like to discuss in detail.

• Workshop 8: **Wafer Level Reliability**

The Wafer Level Reliability workshop will discuss the status and accomplishments of various WLR standards and the progress of investigations being performed by committees. The recent work of JEDEC Committee on WLR, JC14.2 will be summarized as well as related WRL activities in our industry. Attendee's are encouraged to bring to the workshop their recent experiences and any related questions regarding test techniques, methods or standards. The workshop draws together a mixed group ranging from expert to novice which provides for an excellent exchange of various topics related to WLR.

• Workshop 9: **Interconnects/Copper/Low-K**

Do you know how to answer your metallization reliability questions? What about the new Cu-base systems that are right around the corner? These are changing times with new materials, challenges and questions. At a time where development cycle time and performance dominate process development, knowing the right test and what to do with the results is crucial. Please join a group of development and production engineers like yourself and share your views on testing Al or Cu-based systems. Because of the importance of Low-K dielectrics on Cu based systems, the performance effects of this material has been added to the discussion list. Topics will include, but are not limited to Electromigaiton, Stress Voiding, Defect Detection and Control, Corrosion, Low-K material performance, etc.

• Workshop 10: **MEMS**

MEMs reliability today is where semiconductor reliability was before we had activation energy concepts and accelerated life procedures using elevated temperatures. Another year has passed and we have new developments and more empirical data. What have we learned? Are our models coming closer to explaining intrinsic characteristics or are we still in the phenomenological theory phase of our understanding? Come and discuss what you have experienced this past year with your colleagues. Listen to what others have to say about their recent work and discuss what's been going on in the laboratory or what you have been reading in publications.

TECHNICAL PROGRAM

Tuesday, April 11, 8:00 a.m., Imperial Ballroom

SYMPOSIUM OPENING: **Jon E. Klema, Symposium General Chair**
William R. Tonti, Technical Program Chair

KEYNOTE: SILICON TECHNOLOGY DIRECTIONS IN THE NEW MILLENIUM—Tak H. Ning, IBM Thomas J. Watson Research Center, Yorktown Heights, NY

Although its performance and density are fast approaching saturation, scaled bulk CMOS will remain the platform for evolving silicon technology into several application-specific directions. Besides logic and memory, there will be emphases on low power, on EEPROM, RF, and analog, and integration of these functions on the same chip or package. The opportunities and challenges will be discussed.

DIELECTRICS *(Session 1)*

Co-Chairs: Ernest Wu, IBM MicroElectronics and
Robin Degraeve, IMEC

1.1 EXPERIMENTAL EVIDENCE FOR VOLTAGE DRIVEN BREAKDOWN MODELS IN ULTRATHIN GATE OXIDES—P.E. Nicollian, W.R. Hunter, and J.C. Hu, Texas Instruments, Inc., Dallas, TX

We have performed an experiment proving that the widely accepted E-field TDDB model is a physically incorrect description of breakdown in ultra-thin gate oxides. Although interface traps are the dominant SILC mechanism below 5V stress, we confirm that breakdown remains limited by bulk trap generation and is voltage-driven.

1.2 TUNNELING CURRENT CHARACTERISTICS AND OXIDE BREAKDOWN IN P+POLY-SILICON PFET CAPACITORS—J. McKenna and E.Y. Wu, IBM Microelectronics Division, Essex Junction, VT

It was found that measured tunneling currents in lightly doped P+ polysilicon gate are much higher and result in much shorter times-to-breakdown as compared with heavily doped P+ poly-silicon. Our results strongly suggest that oxide breakdown is energy- and fluence- driven rather than time- and field driven as commonly accepted.

1.3 FIELD ACCELERATION FOR OXIDE BREAKDOWN - CAN AN ACCURATE ANODE HOLE INJECTION MODEL RESOLVE THE E VS. 1/E CONTROVERSY?—M.A. Alam, J. Bude and A. Ghetti, Lucent Technologies, Murray Hill, NJ

We show that an anode hole injection model can resolve the controversies involving oxide reliability projection including E vs. 1/E field acceleration, the polarity gap, and the thickness dependence of field acceleration. The most accurate extrapolations can be made by placing accelerated breakdown data on a voltage versus $\ln(t_{BD})$ curve whose shape is universal.

1.4 ANODE HOLE INJECTION VERSUS HYDROGEN RELEASE: THE MECHANISM FOR GATE OXIDE BREAKDOWN—J.Wu, E. Rosenbaum, University of Illinois, Urbana, IL, B. MacDonald, AMD, Sunnyvale, CA, E. Li, University of Illinois, Urbana, IL, J. Tao, B. Tracy, and P. Fang, AMD, Sunnyvale, CA

The gate oxide reliability of deuterium annealed MOS devices is similar to that of hydrogen annealed devices while the hot carrier lifetime is over one order of magnitude larger. This finding sheds doubt on a gate oxide breakdown model that purports that a necessary step is release of interfacial hydrogen by tunneling electrons.

1.5 TEMPERATURE DEPENDENCE OF SOFT BREAKDOWN AND WEAROUT IN SUB 3nm SiO_2 FILMS—J.S. Suehle and E. Vogel, NIST, Gaithersburg, MD, B. Wang and J.B. Bernstein, University of Maryland, College Park, MD

The temperature dependence of breakdown for sub-3 nm SiO_2 films was studied. The results indicate that both soft and hard breakdown modes exhibit the same thermal acceleration. The thermal activation energy is

observed to decrease for higher gate voltages which may explain the observation of increased temperature acceleration for ultra-thin films.

1.6 STUDY OF THE TEMPERATURE AND VOLTAGE ACCELERATION BEHAVIOR OF SOFT BREAKDOWN AND HARD BREAKDOWN IN ULTRA-THIN SiO_2 GATE DIELECTRICS—T. Pomp, H. Wurzer*, M. Kerber, Infineon Technologies, Muenchen, Germany, and I. Eisele, Universitaet der Bundeswehr Muenchen, Neubiberg, Germany

*Infineon Technologies, Dresden,Germany

It is shown that soft breakdown (SBD) has significantly different temperature and voltage acceleration behavior than does hard breakdown (HBD). These properties influence reliability characterization of ultra-thin SiO_2 gate dielectrics. A mix-up of times to SBD and HBD during TDDB testing can result in erroneous conclusions.

1.7 QUASI-REAKDOWN IN ULTRA-THIN SiO_2 FILMS : OCCURRENCE CHARACTERIZATION AND RELIABILITY ASSESSMENT METHODOLOGY—S. Bruyere, E. Vincent, STMicrolectronics, Crolles, France and G. Ghibaudo, LPCS, ENSERG, Grenoble, France

The area, electric field, and temperature dependencies of quasi-breakdown and breakdown are investigated. We demonstrate that the physical defects related to the quasi-breakdown phenomenon are different from those related to breakdown. We introduce the concept that breakdown and quasi-breakdown are competing mechanisms.

Tuesday, April 11, 2:00 p.m., Parallel Sessions 2A–2B & *2C–2D*

DIELECTRICS II *(Session 2A, Imperial Ballroom)*

(in parallel with 2C–2D and followed by 2B)

Co-Chairs: Ernest Wu, IBM MicroElectronics and Bonnie E. Weir, IMEC

2A.1 EVIDENCE FOR RECOMBINATION AT OXIDE DEFECTS AND NEW SILC MODEL—D. Ielmini, A.S. Spinelli*, A.L. Lacaita, Politecnico di Milano, Milano, Italy, and G. Ghidini, STMicroelectronics, Agrate Brianza, Italy

*Università dell'Insubria, Como, Italy

A detailed experimental study of SILC dependencies on time, stress fluence, and polysilicon doping shows that electron-hole recombination at bulk oxide defects plays a primary role in low-field SILC. A numerical model based on this novel mechanism successfully reproduces leakage phenomena for oxide thicknesses ranging from 2.8 to 8.2 nm.

2A.2 EXPERIMENTAL ANALYSIS OF GATE OXIDE DEGRADATION –EXISTENCE OF NEUTRAL TRAP PRECURSOR, SINGLE AND MULTIPLE TRAP-ASSISTED TUNNELING FOR SILC MECHANISM– —R.Yamada, J.Yugami, and M. Ohkura, Hitachi, Ltd., Kokubunji, Tokyo

We have analyzed gate oxide degradation and conclude that neutral traps are generated when hot holes attack the trap precursors. These neutral traps induce an excess leakage current, the so-called SILC. The conduction mechanism of SILC changes from single trap-assisted tunneling (TAT) to multiple-TAT as the neutral trap density increases in thick (> 6 nm) oxides.

2A.3 TEMPERATURE EFFECT ON THE RELIABILITY OF ZrO_2 GATE DIELECTRIC DEPOSITED DIRECTLY ON SILICON—W.-J. Qi, R. Nieh, B.H. Lee, L. Kang, Y. Jeon, K. Onishi, S. Gopalan, and J.C. Lee, University of Texas, Austin, TX

The effect of temperature on the reliability of ZrO_2 films is investigated. At 150 °C, an operating voltage of -1.95V yields an extrapolated 10 year lifetime. No enhanced trap generation is observed at elevated temperatures. ZrO_2 exhibits a lower activation energy than does thermal oxide which indicates an improved temperature accelerated dielectric breakdown.

HOT CARRIERS *(Session 2B, Imperial Ballroom)*

(following 2A and in parallel with 2C–2D)

Co-Chairs: Ronald C. Lacoe, The Aerospace Corporation
Giuseppe La Rosa, IBM MicroElectronics

2B.1 CHANNEL-WIDTH DEPENDENT HOT-CARRIER DEGRADATION OF THIN-GATE pMOSTs— Y.-H. Lee, K. Wu, T. Linton, N. Mielke, S. Hu, and B. Wallace, Intel Corp., Santa Clara, CA

Channel width dependent pMOST hot-carrier degradation has been investigated in a 0.25 µm CMOS technology. Two distinct trapping mechanisms were observed in the narrow (electron trapping) and wide (hole trapping) devices. Simulations indicate that the electric field difference between the STI edge and channel area is responsible for these results.

2B.2 THE ROLE OF THE SPACER OXIDE IN DETERMINING WORST-CASE HOT-CARRIER STRESS CONDITIONS FOR NMOS DEVICES—E.E. King, R.C. Lacoe, The Aerospace Corp., Los Angeles, CA and J. Wang-Ratkovic, AMD, Sunnyvale, CA

Experimental data and a model are presented that explain the contribution of the LDD series resistance increase to the cross over in worst-case bias condition (from maximum substrate current to maximum gate voltage) for NMOS LDD transistors. The dependence of this effect to channel length and temperature are also described.

2B.3 GENERATION OF HOT CARRIERS BY SECONDARY IMPACT IONIZATION IN DEEP SUBMICRON DEVICES: MODEL AND LIGHT EMISSION CHARACTERIZATION—B. Marchand, D. Blachier*, G. Ghibaudo, C. Leroux, F. Balestra, and G. Reimbold*, LPCS-ENSERG, Grenoble, France
*LETI-CEA, Grenoble, France

A simple and accurate analytical model of the gate current due to the secondary impact ionization in deep submicron MOS devices is given, taking the substrate bias and the temperature influences into account. In addition, for the first time the related light emission spectrum and photon origin are presented.

2B.4 ANALYSIS OF HOT-CARRIER-INDUCED DEGRADATION IN MOSFET BY GATE-TO-DRAIN AND GATE-TO-SUBSTRATE CAPACITANCE MEASUREMENT—C. Hsu, M. Lau, and Y.T. Yeow, The University of Queensland, Brisbane, Australia, and Z.Q. Yao, Quality Semiconductors Australia, Sydney, Australia

This paper describes and demonstrates the use of gate-to-drain capacitance measurements at below liquid nitrogen temperature as a tool to characterize the hot carrier induced charge centers. In addition, a new method based on gate-to-substrate capacitance is proposed to extract the spatial distribution of fixed oxide charges.

2B.5 HOT CARRIER INDUCED DEGRADATION IN DEEP SUBMICRON MOSFETs AT 100 °C—E. Li, E. Rosenbaum, and L.F. Register, University of Illinois at Urbana-Champaign, Urbana, IL, and J. Tao, and P. Fang, AMD, Sunnyvale, CA

For deep submicron n- and p-MOSFETs, Vg=Vd is demonstrated to be the worst-case hot-carrier stress condition. Degradation is more severe at 100 °C than at room temperature, even at stress voltages greater than 2.5V. The effect of the channel length on the temperature dependence of the substrate current is examined.

2B.6 EARLY STAGE HOT CARRIER DEGRADATION OF STATE-OF-THE-ART LDD n-MOSFETs—S.K. Manhas, M.M. De Souza, De Montfort University, Leicester, U.K., A.S. Oates, S.S. Chetlur, Lucent Technologies, Orlando, FL, and E.M. Sankara Narayanan, De Montfort University, Leicester, U.K.

Detailed hot carrier degradation experiments beginning as early as 10 µs in submicron n-channel LDD MOSFETs reveal a new early two-stage series resistance degradation process, which deviates from the power law behavior. Detailed quantitative analysis suggests this LDD induced-damage saturates within 10 seconds, far earlier than reported in the literature.

MEMS *(Session 2C, Regency Room in parallel with 2A–2B)*
Co-Chairs: William M. Miller, Sandia National Laboratories
Sam Kayali, Jet Propulsion Laboratory

2C.1 RELIABILITY CHARACTERIZATION OF THERMAL MICRO-STRUCTURES IMPLEMENTED ON 0.8 MICRON CMOS CHIPS—L. Y. Sheng, C. De Tandt, W. Ranson, and R. Vounckx, The University of Brussels, Brussels, Belgium

This paper discusses the reliability characterization of thermal microstructures implemented on industrial 0.8 µm CMOS chips. Various failure mechanisms are identified and evaluated under high temperature operations. The results can be used to optimize the design of thermally-based microsensors on CMOS chips.

2C.2 RELIABILITY STUDIES OF BENT-BEAM ELECTRO-THERMAL ACTUATORS—L. Que, J.-S. Park, M.-H. Li, Y.B. Gianchandani, University of Wisconsin, Madison, WI

This paper reports on the first lifetime studies of bent beam electro-thermal microactuators that are being used to drive safing and arming micromechanisms. Lifetimes are linked to actuation conditions and dimensional parameters, suggesting an inverse correlation between lifetime and beam stress. Some devices are stable for >30 million actuation cycles.

2C.3 NONTACTILE RELIABILITY TESTING OF A MICRO OPTICAL ATTENUATOR—C. Rembe, H. Aschemann, S. aus der Wiesche, E.P. Hofer, University of Ulm, Ulm, Germany, and H. Debeda, J. Mohe, and U. Wallrabe, Institute of Microstructure Technology, Karlsruhe, Germany

The reliability investigations presented in this paper have been performed on a micro optoelectromechanical actuator developed for switching and attenuation of light propagation in optical fibers. It is demonstrated that high speed cine-photomicrography together with model based evaluation of the image sequences is a powerful diagnostic tool for reliability testing of dynamic processes in MEMS.

2C.4 MEMS RELIABILITY IN A SHOCK ENVIRONMENT—D.M. Tanner, K.S. Helgesen, J.A. Walraven, J.J. Clement, L.W. Irwin, F.A. Brown, and D.L.Gregory, Sandia National Laboratories, Albuquerque, NM

A surface-micromachined MEMS device, consisting of an electrostatic comb-drive actuator driving a single gear, has been tested in an extreme shock environment along three axes. The microengines survived stress levels 20 times higher than those expected in actual use, showing them to be extremely robust.

2C.5 MEMS RELIABILITY IN A VIBRATION ENVIRONMENT—D.M. Tanner, K.S. Helgesen, J.A. Walraven, J.J. Clement, L.W. Irwin, F.A. Brown, and D.L.Gregory, Sandia National Laboratories, Albuquerque, NM

A surface-micromachined MEMS device, consisting of an electrostatic comb-drive actuator driving a single gear, has been tested using three modes of extreme white noise vibration. The microengines survived stress levels four times higher than those expected in actual use, showing them to be extremely robust.

2C.6 EFFECT OF W COATING ON MICROENGINE PERFORMANCE—S. S. Mani, J. G. Fleming, J. A. Walraven, J. J. Sniegowski, M.P. de Boer , L.W. Irwin, D.M. Tanner, D.A. LaVan, J. Jakubczak, and W.M. Miller, Sandia National Laboratories, Albuquerque, NM

A process was used to selectively coat MEMS devices with tungsten (W) using chemical vapor deposition (CVD) techniques. This coating is very conformal, having excellent step coverage, and is extremely uniform. Tungsten coated MEMS microengines tested for reliability show improved wear characteristics with longer lifetimes than polysilicon microengines.

DEVICE & PROCESS I *(Session 2D, Regency Ballroom)*
(following 2C & in parallel with 2A–2B)
Co-Chairs: E. Ajith Amerasekera, Texas Instruments, Inc.
Klaus F. Schuegraf, Conexant Systems

2D.1 NEUTRON-INDUCED BORON FISSION AS A MAJOR SOURCE OF SOFT ERRORS IN DEEP SUBMICRON SRAM DEVICES—R.C. Baumann and E.B. Smith, Texas Instruments, Dallas, TX
Reports the impact of cosmic neutron induced 10B fissions in production logic devices. Using a specially designed cold neutron source to probe soft-error events caused by 10B fissions in deep-submicron SRAM devices fabricated with and without borophosphosilicate glass establishes both the presence and magnitude of these soft-error events.

2D.2 MULTI PARAMETER METHOD FOR YIELD ANALYSIS AND RELIABILITY ASSESSMENT—Y. Mitnick, B. Lisenker, U. Sasson, Intel, Haifa, Israel, and R. Miller, Intel, Chandler, AZ
Introduces a new criteria for product margin and reliability risk assessment using a 0.25 µm CMOS microprocessor technology, based on standby current, fmax and XY die location. The criteria provide the rule for segregating units into groups with differerent margins with respect to parametric variations and stresses. Data analysis at Sort permits prediction of final test fall-out for high-risk groups with > 16% probability.

2D.3 CMOSFET CHARACTERISTICS INDUCED BY MOISTURE DIFFUSION FROM INTER-LAYER DIELECTRIC IN 0.23 µm DRAM TECHNOLOGY WITH SHALLOW TRENCH ISOLATION—S.-K. Park, M.-S. Suh, J.Y. Kim, G.-H. Yoon, Hyundai Microelectronics Co. Ltd., Cheongju-si, Korea
Investigates the impact of moisture diffusion from ILD layer in 0.23 µm DRAM on CMOSFET characteristics. The nMOSFET shows an anomalous short-channel hump, while the CMOSFET shows decreased short-channel margin. This study investigates the use of different barrier films to suppress these effects.

Tuesday, April 11, 6:30 — 9:30 p.m.

SYMPOSIUM RECEPTION
THE TECH MUSEUM OF INNOVATION

The Tech Museum of Innovation which is located within short walking distance directly across Plaza de Cesar Chavez from the hotel. Attendees will long remember designing their own roller coaster and test driving it using 3-D simulation software, or maneuvering a remotely-operated vehicle through a 7700 gallon water-filled tank. Galleries include Communication: Global Connections, Innovation: Silicon Valley and Beyond, Exploration: New Frontiers, and Life Tech: The Human Machine. A light buffet will also be provided for Symposium attendees and their guests.

Wednesday, April 12, 8:15 a.m., Parallel Session 3A &3B–3C

DEVICE & PROCESS II (Sess. 3A, Imperial Ballroom)
Co-Chairs: E. Ajith Amerasekera, Texas Instruments, Inc.
Klaus F. Schuegraf, Conexant Systems

3A.1 ONE TIME PROGRAMMABLE DRIFT ANTIFUSE CELL RELIABILITY—P. Candelier, N. Villani, and J.-P. Schoellkopf, STMicroelectronics, Crolles, France
An innovative non-volatile memory cell compatible with standard CMOS process and based on tunnel oxide breakdown is presented. Both device architecture and design are limiting non-selected cells oxide stress to reach the 10-year lifetime criteria. Broken-down oxide read current stability under bias and temperature is also shown.

3A.2 HOT-CARRIER RELIABILITY OF LATERAL DMOS TRANSISTORS—V. O'Donovan, S. Whiston, and A. Deignan, Analog Devices, Limerick, Ireland
Investigates degradation induced by hot electrons in lateral DMOS transistors. Illustrates limitation of existing CMOS/BiCMOS stressing techniques

and models. Simulation results support the validity of modified LDMOS stressing techniques. Experimental results determine a hot-electron safe-operating-area for reliable LDnMOS and LDpMOS operation.

3A.3 HIGH PERFORMANCE DEEP-SUBMICRON nMOSFETs BY NITROGEN IMPLANTATION AND *IN-SITU* HF CLEAN—J.H. Chen, T.F. Lei, National Chiao Tung University, Hsinchu, Taiwan, C.L. Chen, T.S. Chao, National Nano Device Laboratory, Hsinchu, Taiwan, W.Y. Wen, and K.T. Chen, Winbon Electronics Corp., Hsinchu, Taiwan

Significant improvement of nMOSFETs results from using nitrogen implantation and *in-situ* HF vapor clean in oxide processing. The interface becomes smoother with less Arsenic incorporation in the channel region, thereby improving device performance and reliability.

3A.4 ROLE OF H_2 ANNEAL IN THIN OXIDE FOR MULTI-METAL-LAYER CMOS PROCESS—Y.-H. Lee, R. Nachman, and K. Seshan, Intel Corp., Santa Clara, CA

Investigates the impact of H_2 in the final annealing cycle of a 5-layer CMOS process and its effect on device behavior using Al/Ti metallization technology. Bias-temperature and hot-carrier data show little difference for changes in H_2 dilution. Differences are reported for devices with varying degrees of metal coverage.

3A.5 ANALYSIS OF EVOLUTION TO AND BEYOND QUASI-BREAKDOWN IN ULTRA-THIN OXIDE AND OXYNITRIDE—M. Okandan, J.S. Fonash, The Penn. State Univ., University Park, PA, B. Maiti, H.H. Tseng, and P. Tobin, Motorola, Austin, TX

Presents the wearout, quasi-breakdown and annealing behavior of 30Å ultrathin oxide and oxynitride films. Shows distinctive differences between devices subject to quasi-breakdown and full breakdown. Demonstrates the impact of thermal annealing on these devices as well as the ramifications for next generation CMOS technologies.

3A6 A NEW DATA RETENTION MECHANISM AFTER ENDURANCE STRESS ON FLASH MEMORY—H. Kameyama, UL Media Ltd., Tokyo, Japan, Y.Okuyama, S. Kamohara, K. Kubota, H. Kume, M. Kato, A. Nozoe, H. Uchida, M. Hidaka, Hitachi Ltd., Tokyo, Japan, and K, Ogura, UL Media Ltd., Tokyo, Japan

Data retention after endurance cycling in FLASH memory is explained by combining two retention models. One model for temperatures greater than 150 °C indicates the inherent retention characteristics are ruled by the thermal emission model. Another model for temperatures between 85 °C and 125 °C indicates that retention is determined by hopping conduction through trap-assisted B-mode SILC currents.

3A.7 ANALYSIS OF DETRAP CURRENT DUE TO OXIDE TRAPS TO IMPROVE FLASH MEMORY RETENTION—R. Yamada, Y. Mori, Y. Okuyama, J. Yugami, T. Nishimoto, and H. Kume, Hitachi Ltd., Tokyo, Japan

Gate oxide detrapping currents are measured to improve flash memory retention. These detrapping currents can be divided into two categories. One is due to direct tunneling to the silicon substrate from deep oxide traps, while the other is due to emission into the SiO_2 conduction band from shallower oxide traps. The deeper traps are generated at the $SiSiO_2$ interface by hot electrons during gate negative FN stress and the shallower taps are generated at Poly/SiO_2 interface by hot holes.

3A.8 BIAS TEMPERATURE DEGRADATION OF pMOSFETs: MECHANISM AND ITS SUPPRESSION—M. Makabe, T. Kubota, and T. Kitano, NEC Corp., Sagamihara, Kanagawa, Japan

The bias-temperature mechanism and its suppression are analyzed in pMOSFETs. Degradation is found to be due to trapped holes produced by impact ionization of electrons injected from the gate electrode. This degradation can be suppressed by doping the gate oxide with boron and by reducing the electric-field strength between the drain and the gate electrodes.

PACKAGING *(Sessions 3B, Regency Ballroom)*

(in parallel with 3A and followed by 3C)

Co-Chairs: Thomas M. Moore, Texas Instruments, Inc.
S. Sidharth, Advanced Micro Devices

3B.1 LIFETIME PREDICTION OF IGBT MODULES FOR TRACTION APPLICATIONS—M. Ciappa and W. Fichtner, Swiss Federal Institute of Technology (ETH), Zurich, Switzerland

Bond wire lift-off caused by thermal fatigue is one of the dominant failure mechanisms of high power Insulator Gate Bipolar Transistor multichip modules used in traction applications (railway). A model is proposed which predicts the lifetime of devices submitted to severe cyclic loads encountered in current converters of railway systems. It assumes linear accumulation of the thermal cycle fatigue damage and takes into account bondwire redundancy in the multichip module.

3B.2 FAILURE ANALYSIS & STRESS SIMULATION IN SMALL CHIP MULTICHIP BGAs—T.D. Moore, Analog Devices, Limerick, Ireland, and J.L. Jarvis, University of Limerick, Limerick, Ireland

Although many studies have been published on stress-related failures in flip chip joints and BGA solder ball joints, little has been published on structural weaknesses within flip chip BGAs. Structural failures within small multichip PBGAs are examined with details of the failure modes which occur in practice. These failure modes are then associated with stresses determined by FEA sinulation. The failure analysis methods used to reveal the failures are also reviewed.

3B.3 SHORT AND LONG-TERM STABILITY PROBLEMS OF HALL PLATES IN PLASTIC PACKAGES—D. Manic and R.S. Popovic, Swiss Federal Institute of Technology, Lausanne, Switzerland

Stability of silicon Hall plate sensitivity (in SOP and TSSOP packages) is studied. A parametric shift is observed when reflow soldering, temperature cycling or humidity testing are performed which is a reliability concern for Hall devices. Moreover, this shift is not stable over time and is correlated to a similar shift in package-induced stress.

3B.4 IMPROVED RELIABILITY PREDICTION THROUGH REDUCED-STRESS TEMPERATURE CYCLING—A.R. Cory, LSI Logic, Fort Collins, CO

With the Coffin-Manson equation as a model, reliably packaged devices are shown to be unreasonably sensitive to commonly accepted temperature cycling criteria. For example, an unlikely product failure mechanism in Condition C temperature cycling masks a common field failure mechanism. A case is presented for replacing conventional stress criteria with conditions designed to detect meaningful failure mechanisms.

COMPOUND SEMICONDUCTORS *(Sess. 3C, Regency Ballroom)*

(following 3B and in parallel with 3A)

Co-Chairs: Fausto Fantini, University of Modena
J.J. Liou, University of Central Florida

3C.1 TRENDS IN SiGe BiCMOS PROCESS INTEGRATION—J. Dunn, D. Harame, S. St. Onge, A. Joseph, N. Feilchenfeld, K. Watson, S. Subbanna, G. Freeman, S.H. Voldman, and R. Johnson, IBM MicroElectronics

A new base-after-gate integration scheme has been developed for a 0.24 µm SiGe BiCMOS. The details of the approach which decouple the Heterojunction Bipolar Transistor from the CMOS thermal cycles while maintaining device performance are discussed. The reliability aspects associated with using SiGe for applications with high collector-base voltage with high emitter current are explored. Finally, the ESD characteristics of the SiGe BiCMOS technology elements are summarized.

3C.2 PULSED MEASUREMENTS AND CIRCUIT MODELING OF A NEW BREAKDOWN MECHANISM OF MESFETs AND HEMTS—E. Zanoni, G. Meneghesso, D. Buttari, M. Maretto, and G. Giovanni, Università di Padova, Padova, Italy

The on-state breakdown characteristics of HMETs were measured in a non-destructive way by using the transmission line pulsing technique. Based on the experimental observations, we developed a new model, which is suitable for SPICE simulation to predict the on-state breakdown of HMETs.

3C.3 BIAS AND TEMPERATURE STRESS RELIABILITY OF InGaP/GaAs HBTs—A.A. Rezazadeh, S.A. Bashar, H. Sheng, F.A. Amin, King's College, London, UK, L. Cattani, Universita di Parma, Parma, Italy, and J.J. Liou, University of Central Florida, Orlando, FL

The reliability of InGaP/GaAs HBTs with different base metal contact systems under current and temperature stress is studied in this paper. We further report the effects of different base dopants and isolation implantation ions on the stability of HBT dc current gain.

3C.4 BREAKDOWN AND DEGRADATION ISSUES AND THE CHOICE OF A SAFE LOAD LINE FOR POWER HFET OPERATION—D. Dieci, R. Menozzi*, T. Tomasi, G. Sozzi*, C. Lanzieri**, and C. Canali, University of Modena, Modena, Italy
*Università di Parma, Parma Italy
**Alenia Marconi Systems, Roma, Italy

This work shows experimental data of hot electron degradation of power AlGaAs/GaAs HFETs. Based on the data, general indications on the bias point dependence of the device degradation, the choice of a safe load line for RF applications, and the breakdown voltage are presented.

3C.5 RELIABILITY OF OPTICAL FIBER BRAGG GRATING SENSORS AT ELEVATED TEMPERATURE—U. Sennhauser, A. Frank, P. Mauron, and P.M. Nellen, EMPA, Dubendorf, Switzerland

Reliability of fibers and Bragg gratings at elevated temperature up to 250 °C are modeled and their parameters are determined. Stress corrosion and grating decay are investigated for two commercially available Bragg grating types, and their temperature dependence on the operating conditions are analyzed.

Wednesday, April 12, 2:00 p.m., Parallel Session 4A & 4B

ELECTROSTATIC DISCHARGE *(Sess. 4A, Imperial Ballroom)*

Co-Chairs: Charvaka Duvvury, Texas Instruments Inc.
Robert J. Gauthier, IBM

4A.1 (ESREF INVITED) HBM AND TLP ESD ROBUSTNESS IN SMART POWER PROTECTION STRUCTURES—G. Meneghesso, L. Volpato, A. Buson, S. Santirosi*, E. Novarini*, C. Contiero*, E. Zanoni, Università di Padova, Padova, Italy
*STMicroelectronics, Milano, Italy

In this paper we will present data concerning the ESD robustness of smart power protection structures (BCD technology) for input-output circuits. A comparison between the robustness of p-body and p-well based structures and a study of the influence of layout parameters on the ESD robustness will be given. The correlation between ESD robustness obtained with different test methods (HBM and TLP) will also be presented.

4A.2 ANALYSIS OF OXIDE BREAKDOWN MECHANISM OCCURRING DURING ESD PULSES—C. Leroux, P. Andreucci, and G. Reimbold, LETI-CEA, Grenoble, France

The oxide tolerance and failure modes under ESD-like short duration high current density pulses are investigated by taking into account the three effects of charge to breakdown, thermal breakdown, and current crowding effects. Due to current crowding, F-N model and the 1/E model cannot be used to predict the failure threshold of thin oxide under ESD.

4A.3 MICROANALYSIS OF VLSI INTERCONNECT FAILURE MODES UNDER SHORT-PULSE STRESS CONDITIONS—K. Banerjee, D.-Y. Kim, Stanford University, Stanford, CA, A. Amerasekera, Texas Instruments, Inc., Dallas, TX, C. Hu, University of California,

Berkeley, CA, S.S. Wong and K.E. Goodson, Stanford University, Stanford, CA

This work presents a detailed microanalysis of interconnect failure mechanisms under short-pulse stress conditions arising during peak current and ESD events. A thermo-mechanical model is formulated for the open circuit failure mode and direct evidence of latent interconnect damage is reported. Suitable design guidelines are proposed to avoid this latent damage.

4A.4 TRANSMISSION LINE MODEL TESTING OF TOP-GATE AMORPHOUS SILICON THIN-FILM TRANSISTORS—N. Tosic, F.G. Kuper*, and T. Mouthaan, University of Twente, The Netherlands

*also Philips Semiconductors, Nijmegen, The Netherlands

In this paper, Transmission Line Model (TLM) characterization is used to analyze ESD events in amorphous silicon thin film transistors (μ-Si:H TFT). Above ESD failure threshold voltage of degradation, either deterioration of electrical characteristics sets in or voltage dielectric breakdown occurs. Simulations were used to confirm the deterioration process which was experimentally found to be due to creation of positive interface charges.

4A.5 PROCESS AND LAYOUT DEPENDENT SUBSTRATE RESISTANCE MODELING FOR DEEP SUB-MICRON ESD PROTECTION DEVICES—X.Y. Zhang, K. Banerjee, Stanford University, Stanford, CA, A. Amerasekera, Texas Instruments Inc., Dallas, TX, Z. Yu, and R.W. Dutton, Stanford University, Stanford, CA

A new methodology for analyzing and predicting the impact of layout and process variations on the effective substrate resistance of deep sub-micro ESD devices is demonstrated using quasi mixed-mode approach. The substrate resistance which is important for ESD design, simulated by this method shows good agreement with experimental data.

4A.6 SIMULATION AND EXPERIMENTAL STUDY OF TEMPERATURE DISTRIBUTION DURING ESD STRESS IN SMART-POWER TECHNOLOGY ESD PROTECTION STRUCTURES—K. Esmark, C. Fürböck*, H. Gossner, G. Groos, M. Litzenberger*, D. Pogany*, R. Zelsacher**, M. Stecher, and E. Gornik*, Infineon Technologies, Munich, Germany

*Vienna University of Technology, Vienna, Austria

**Infineon Technologies, Villach, Austria

Electro-thermal simulation and laser-interferometry thermal mapping are performed to study temperature distribution in smart power technology electrostatic discharge (ESD) protection npn transistors. Simulations utilizing improved model calibration predict two separate hot spots due to vertical and lateral current paths in the base region. The location of hot spots, their temperature evolution, and dependence on stress level agree well with experiments.

4A.7 ELECTROSTATIC DISCHARGE AND HIGH CURRENT PULSE CHARACTERIZATION OF EPITAXIAL BASE SILICON-GERMANIUM HETEROJUNCTION BIPOLARE TRANSISTORS—S.H. VoIdman, P. Juliano*, R. Johnson, N. Schmidt, A. Joseph, S. Furkay, E. Rosenbaum*, J. Dunn, D. Harame, IBM MicroElectronics, Essex Junction, VT and B. Meyersor, IBM Watson Research, Yorktown Heights, NY *University of Illinois at Champaign-Urbana, IL

ESD robustness of SiGe HBT devices are investigated for the first time. High current characterization using transmission line pulse methods and Wunch-Bell power-to-failure curve analysis on the epitaxial graded-Ge base devices show higher failure current levels compared to Si homojunction BJT devices and this is supported by the relatively higher failure thresholds from HBM stress data.

INTERCONNECTS *(Session 4B, Regency Ballroom)*

Co-Chairs: J. Joseph Clement, Sandia National Laboratories
James R. Lloyd, JPL

4B.1 THE ROLE OF COPPER IN ELECTROMIGRATION: PROPERLY ACCOUNTING FOR A Cu-VACANCY BINDING ENERGY—M.J. Tammaro, University of Rhode Island, Kingston, RI

The precise role of copper in extending electromigration lifetimes in Al-Cu interconnects is still not well understood. A model based on microscopic diffusion kinetics is proposed that reproduces all of the relevant features of experiments. A novel analysis based on rate equations for atomic pair probabilities is developed.

4B.2 ELECTROMIGRATION LIFETIME ENHANCEMENT FOR LIFETIMES WITH MULTIPLE BRANCHES—M.J. Dion, Intersil Corp., Melbourne, Fl.

With clock or power supply interconnect "trees", there is often a very high current "trunk" feeding current to multiple branches. This work demonstrates increased trunk lifetime with increasing number of branches, which terminate at via plugs. Comparative Black's model parameters are developed and failure analysis is described. Implications for electromigration design rules are discussed.

4B.3 EFFECT OF Ti INSERTION BETWEEN Cu AND TiN LAYERS ON ELECTROMIGRATION RELIABILITY IN Cu/(Ti)/TiN/Ti LAYERED DAMASCENE INTERCONNECTS—K. Abe, S. Tokitoh, S.C. Chen, J. Kanamori, and H. Onoda, OKI Electric Industry Co., Ltd., Tokyo, Japan

It is important to control the Cu/barrier interface, since it can be the dominant diffusion path for electromigration. This work demonstrates superior electromigration performance can be achieved by inserting a thin Ti layer between Cu and the TiN barrier layer. This improvement is associated with Cu-Ti compound formation, not only at the Cu/barrier interface, but also in the Cu grain boundary.

4B.4 TDDB IMPROVEMENT IN Cu METALLIZATION UNDER BIAS STRESS—J. Noguchi, N. Ohashi, J. Yasuda, T. Jimbo, H. Yamaguchi, N. Owada, K. Takeda, and K. Hinode, Hitachi, Ltd., Tokyo, Japan

Time-dependent dielectric breakdown (TDDB) between Cu interconnects depends strongly on the surface condition of the Cu interconnect and the surrounding dielectrics. An NH_3-plasma treatment prior to cap-pSiN deposition improves TDDB lifetime. This is shown to reduce CuO and to introduce a nitridation layer on the Cu surface, which prevents Cu-silicide formation at the interface.

4B.5 CONDUCTION PROCESSES IN Cu/LOW-k INTERCONNECTION—G. Bersuker, V. Blaschke, S. Choi, and D. Wick, SEMATECH, Austin, TX

Electrical characterization of leakage currents in damascene Cu/low-k structures was performed. Ionic conduction due to contamination inherent to the dielectric was found to be the leading cause of intrinsic intra-metal line leakage at low temperatures, while at elevated temperatures a contribution from electron current was detected. Dielectric and barrier layer parameters that control the conduction process were evaluated.

4B.6 LEAKAGE AND BREAKDOWN RELIABILITY ISSUES ASSOCIATED WITH LOW-k DIELECTRICS IN A DUAL-DAMASCENE Cu PROCESS— R.Tsu, J. McPherson, and R. McKee, Texas Instruments, Inc., Dallas, TX

Leakage and breakdown characteristics of low-k dielectrics are becoming critically important reliability issues for interconnects scaled to 0.18 μm and beyond. TDDB is a significant concern for breakdown strengths of < 2 MV/cm. Cu out-diffusion through the barrier confinement and moisture absorption are shown to greatly exacerbate the low-k TDDB issue.

4B.7 QUANTITATIVE PROJECTIONS OF RELIABILITY AND PERFORMANCE FOR LOW-k/Cu INTERCONNECT SYSTEMS—K. Banerjee, Stanford Univ., Stanford, CA, A. Mehrotra, Univ. of Illinois, Urbana-Champaign, IL, W.R. Hunter, Texas Instruments, Dallas, TX, K.C. Saraswat, S.S. Wong, Stanford Univ., Stanford, CA

A methodology for quantitative analysis of the role of electromigration and performance in determining optimal interconnect design is presented. This methodology is applied to various low-k/Cu interconnect systems. It is demonstrated that electromigration design limits for signal lines are automatically satisfied, when the interconnect performance is optimized.

4B.8 EXPERIMENTAL DATA AND STATISTICAL MODELS FOR BIMODAL EM FAILURES—A.H. Fischer, Infineon Technologies, München, Germany, A. Abel, Technical University Dresden, Dresden, Germany, M. Lepper, and A.E. Zitzelsberger, Infineon Technologies, München, Germany

Electromigration (EM) failure times are usually fit by asignal log-normal distribution. But, in some cases relevant deviations are observed. We discuss two types of non log-normal distributions, observed on via-line structures. They can be modeled by two types of bimodal distributions, each composed of two log-normal distributions. Both models consider different failure mechanisms within the sample. We will present experimental data sets coinciding with either model. The physical failure analysis confirms the model assumptions and supports the bimodal distribution concept.

Wednesday, April 12, 7:00-8:00 p.m., Ballroom Pre-function Area

BANQUET RECEPTION

Wednesday, April 12, 8:00 p.m., Regency Ballroom

SYMPOSIUM BANQUET

A no-host reception prior to the Banquet will run from 7:00 p.m. to 8:00 p.m. in the Ballroom foyer. Awards for 1999 IRPS Best and Outstanding Papers will be presented immediately following dinner. Registered attendees for the Symposium will receive one ticket for admission to the banquet. Additional tickets may be purchased at the Registration Desk for $25.

Thursday, April 13, 8:15 a.m, Imperial Ballroom

PROCESS INDUCED DAMAGE *(Session 5)*

Co-Chairs: Terence B. Hook, IBM Microelectronics
Paul E. Nicollian, Texas Instruments Inc.

5.1 A MODEL FOR EVALUATING CUMULATIVE OXIDE DAMAGE FROM MULTIPLE PLASMA PROCESSES—K. Noguchi, A. Matsumoto, and N. Oda, NEC Corp., Sagamihara, Kanagawa, Japan

A model for evaluating cumulative oxide damage caused by multiple plasma processes is proposed. By considering a sub-linear dependence of the charging current on the antenna ratio, damage of a device with various antenna configurations is estimated. A modified antenna rule is proposed, and a realistic design guideline is obtained.

5.2 ON-CHIP PROBES FOR SILICON DEFECTIVITY RANKING AND MAPPING—A. Zanchi, F. Zappa, M. Ghioni, Politecnico di Milano, Milano, Italy, and A.P. Morrison, University College Cork, Cork, Ireland

On-wafer probes capable of localizing lattice defects in silicon are described. These probes are based on single-photon avalanche diodes that sense the defect-induced thermal generation of single carriers within the junction. These probes give suitable figures of merit for ranking the overall defectivity and mapping the spatial variation.

5.3 DETECTION OF THIN OXIDE (3.5 nm) DIELECTRIC DEGRADATION DUE TO CHARGING DAMAGE BY RAPID-RAMP BREAKDOWN—T.B. Hook, D. Harmon, IBM MicroElectronics, Essex Junction, VT, and C. Lin, Infineon Microelectronics, Hopewell Junction, NY

For thin dielectrics (<4.0 nm) it is difficult to detect charging damage, the traditional techniques of Fowler-Nordheim or hot-carrier stressing no longer being adequately sensitive, and leakage measurements being confounded by tunneling current and also requiring very high resolution. In this paper we

propose rapid ramp breakdown as a practical and quantitative method of characterizing the impact of charging damage.

5.4 CHARGE PUMPING TECHNIQUE FOR THE EVALUATION OF PLASMA INDUCED EDGE DAMAGE IN SHALLOW S/D EXTENSION THIN GATE OXIDE nMOSFETs—S.S. Chung, S. J. Chen, H. L. Kao, S. J. Luo, National Chiao Tung University, Taiwan, R.O.C., and H.C. Lin, Nano Device Lab., Taiwan, R.O.C.

Plasma etching of polysilicon during the gate definition induces the so-called plasma edge damage at the edge of the gate. This damage has been verified on test patterns with various shapes and areas, and is shown to exacerbate the device degradation after hot-electron stress. Results from a charge-pumping analysis show that interface traps are the dominant mechanism of the degradation in drain current from the plasma-induced edge damage. Application of this techique to antenna effect studies is demonstrated.

OXIDE PANEL *(Imperial Ballroom)*

IS TECHNOLOGY SCALING LIMITED BY OXIDE RELIABILITY?

PANEL:	Joe McPherson	Texas Instruments
	David Dumin	Clemson University
	Chenming Hu	UC Berkeley
	Eric Vogel	NIST
	John Suehle	NIST
	William Abadeer	IBM MicroElectronics
	Bonnie Weir	Lucent Technologies
	Robin Degraeve	IMEC
	Scott A. Hareland	Intel Corporation
MODERATORS:	William R. Tonti	IBM MicroElectronics
	Tony Oates	Lucent Bell Labs

Thursday, April 13, 2:00 p.m., Imperial Ballroom

FAILURE ANALYSIS *(Session 6)*

Co-Chairs: Daniel Barton, Sandia National Laboratories
Jacob Phang, National University of Singapore

6.1 QUANTITATIVE THERMAL PROBING OF DEVICES AT SUB-100 nm RESOLUTION—L. Shi, O. Kwon, G. Wu, A. Majumdar, University of California, Berkeley, CA

The paper reports the use of a micromachined scanning thermal probe for quantitatively probing semiconductor devices with sub-100 nm spatial resolution. The thermal design of the probe was optimized to improve accuracy in temperature measurement and spatial resolution. Temperature distributions on different submicron and subsurface VLSI via structures were measured.

6.2 ELECTRICAL PROBING OF DEEP SUB-MICRON ICS USING SCANNING PROBES—K. Krieg, R. Qi, Micron Force Instruments, D. Thomson and G. Bridges, University of Manitoba, Canada and Micron Force Instruments

A contact probing system is presented that fits on a standard probe-station and utilizes a conductive atomic force microscope tip to rapidly measure the surface topography and acquire real-time high-frequency signals from features as small as 0.18 µm. The probe achieves a bandwidth greater than 3 GHz.

6.3 A STUDY OF IMPLANT-INDUCED THIN OXIDE FILM EXPANSION DURING DRY PHOTORESIST ETCHING,—K. P. Lin, K.-M. Ching, K.-S. Huang, and S.-L. Hsu, Taiwan Semiconductor Manufacturing Company Ltd., Taiwan

Bubble-like protrusion defects were found in source and drain areas after stripping the implant mask photoresist. Stress voiding from vacancies created by these defects beside metal interconnections can cause a severe

reliability issue. This case study focuses on the identification of the root cause behind the formation of the protrusions. Methods to prevent void formation are also discussed.

6.4 RELIABILITY ASSESSMENT BY DEFECT BASED TESTING—B. Lisenker and Y. Mitnick, Intel, Haifa, Israel

This paper introduces a new fault model that represents deep-sub-micron CMOS ULSI circuits in standby mode as a single effective MOSFET. It is shown that normal units can be separated from defective ones by means of measuring ISB current versus VCC. Product data shows that 0.25 µm process creates defects that have four types of behavior. A strong correlation between rejected devices and early failure rate is demonstrated.

6.5 LOCALIZING POWER TO GROUND SHORTS IN A CHIPS-FIRST MCM BY SCANNING SQUID MICROSCOPY—E. Vanderlinde, M.E. Cheney, E.B. McDaniel, and K.L. Skinner, Microelectronics Research Laboratory, Columbia, MD, L.A. Knauss, B.M. Frazier, and H.M. Christend, Neocera, Inc., Beltsville, MD

A novel technique called scanning SQUID microscopy was used to locate power-to-ground shorts in a copper/polyimide chips-first MCM. Other F/A techniques were unsuccessful in locating the shorts, but the magnetic current imaging quickly found the defects. Mechanical cross-sections through the part showed shorted metal from a process defect.

6.6 SINGLE CONTACT OPTICAL BEAM INDUCED CURRENTS (SCOBIC) - A NEW FAILURE ANALYSIS TECHNIQUE—J.M. Chin, J.C.H. Phang, D.S.H. Chan, National University of Singapore, and C.E. Soh, AMD, Singapore

The Single Contact Optical Beam Induced Currents (SCOBIC) is a new failure analysis technique. By connecting the substrate or power pins of an integrated circuit to the amplifier, many junctions can be imaged. In contrast, in the OBIC technique, only the junction directly connected to the current amplifier is imaged.

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Take HWY 101 south.
Exit Guadalupe Parkway. (HWY 87)
Continue down Guadalupe three miles to the Park Ave. exit.
Make a left on Park Ave. and continue down two blocks.
Make a right turn on Almaden Blvd.
Next light will be San Carlos St., Turn left.
Continue down one block to market.
Make a left turn on Market St. The hotel will be on block up on the right side. Can't miss it!

From Highway 280/680 in either Direction:

Take HWY 87 North (Guadalupe Parkway).
Continue down Guadalupe One quarter of a mile to Santa Clara St., Exit.
Make a right on Santa Clara St. go four lights to Market St. and make a Right.
Continue on Market two blocks and circle City Plaza Park.
The hotel Is located at 170 S. Market St. The cross street is San Fernando.

From Highway 880/17 in either Direction:

Take the Coleman Ave. exit.
Make a left on Coleman from either direction.
Continue on Coleman two miles where it will become Market St. Circle City Plaza Park.
The hotel is located at 170 S. Market St. The cross street is San Fernando.

From the South on Highway 101 (Los Angeles):

Take HWY 101 North to HWY 280 North.
The third exit will beGuadalupe Parkway (HWY 87). Exit (HWY) North.
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Make a right on Santa Clara St. Go four lights to Market St. and make a right.
Continue on Market St. two blocks and circle Plaza de Cezar Chavez Park. The hotel is located on 170 S. Market St. The cross street is San Fernando.

Event/Location/Time Table

Time	Event	Room
Sunday		
3:00 p.m. - 9:00 p.m.	Symposium Registration	Gold Room (Ballroom Level)
7:00 p.m. - 9:00 p.m.	Companions' Prog. Reg.	Gold Room (Ballroom Level)
Monday		
7:00 a.m.	Tutorials' Coffee/Danish	Ballroom Pre-function Area
7:00 a.m. - 6:00 p.m.	Info Tables / Demo Sign Ups	Ballroom Pre-function Area
7:00 a.m. - 8:00 p.m.	Symposium Registration	Gold Room (Ballroom Level)
8:00 -11:30 a.m.	Tutorial 1	Imperial Ballroom
8:00 - 9:30 a.m.	Tutorial 2	Regency Ballroom I
10:00 - 11:30 a.m.	Tutorial 3	Regency Ballroom I
8:00 - 9:30 a.m.	Tutorial 4	Crystal Room
10:00 - 11:30 a.m.	Tutorial 5	Crystal Room
8:00 -11:30 a.m.	Tutorial 6	Regency Ballroom II
12:00 - 5:00 p.m.	Equip. Demonstrations	Parkside Hall A/B
1:30 - 3:00 p.m.	Tutorial 7	Regency Ballroom II
3:30 - 5:00 p.m.	Tutorial 8	Regency Ballroom II
1:30 - 3:00 p.m.	Tutorial 9	Regency Ballroom I
3:30 - 5:00 p.m.	Tutorial 10	Regency Ballroom I
1:30 - 5:00 p.m.	Tutorial 11	Imperial Ballroom
6:00 p.m. - 8:00 p.m.	Companions' Prog. Reg.	Gold Room
7:30 p.m. - 9:30 p.m.	Workshops #1 to 10	To be posted on-site
Tuesday		
7:00 a.m.	Coffee/Danish	Ballroom Pre-function Area
7:00 a.m. - 5:30 p.m.	Info Tables / Demo Sign Ups	Ballroom Pre-function Area
7:00 a.m. - 2:00 p.m.	Symposium Registration	Gold Room (Ballroom Level)
7:30 a.m. - 5:00 p.m.	Equip. Demonstrations	Parkside Hall A/B
8:00 - noon	Opening/Tech. Sess.1	Imperial Ballroom
9:55 - 10:20 a.m.	Coffee Break	Ballroom Pre-function Area
2:00 - 6:10 p.m.	Technical Session 2A & 2B	Imperial Ballroom
2:00 - 6:10 p.m.	Technical Session 2C & 2D	Regency Ballroom
3:15 - 3:40 p.m.	Coffee Break	Ballroom Pre-function Area
6:30 p.m.- 9:30 p.m.	Symposium Reception	Tech Museum
Wednesday		
7:00 a.m.	Coffee/Danish	Ballroom Pre-function Area
7:00 a.m. - 5:30 p.m.	Info Tables / Demo Sign Ups	Ballroom Pre-function Area
8:00 a.m. - 2:00 p.m.	Symposium Registration	Gold Room (Ballroom Level)
7:30 a.m. - 5:00 p.m.	Equip. Demonstrations	Parkside Hall A/B
8:15 - noon	Technical Session 3A	Imperial Ballroom
8:15 - 12:25 p.m.	Technical Session 3B–3C	Regency Ballroom
9:55 - 10:20 a.m.	Coffee Break	Ballroom Pre-function Area
2:00 - 5:20 p.m.	Technical Session 4A	Imperial Ballroom
2:00 - 5:45 p.m.	Technical Session 4B	Regency Ballroom
3:15 - 3:40 p.m.	Coffee Break	Ballroom Pre-function Area
7:00 p.m. - 8:00 p.m.	Awards Banquet Reception	Ballroom Pre-function Area
8:00 p.m.	Awards Banquet	Regency Ballroom
Thursday		
7:00 a.m.	Coffee/Danish	Ballroom Pre-function Area
7:00 a.m. - noon	Info Tables / Demo Sign Ups	Ballroom Pre-function Area
8:00 a.m. - 2:00 p.m.	Symposium Registration	Gold Room (Ballroom Level)
7:30 a.m. - noon	Equip. Demonstrations	Parkside Hall A/B
8:15 - 9:55 a.m.	Technical Session 5	Imperial Ballroom
9:55 - 10:20 a.m.	Coffee Break	Ballroom Pre-function Area
10:20 a.m.- noon	Oxide Panel	Imperial Ballroom
2:00 - 4:45 p.m.	Technical Session 6/Closing	Imperial Ballroom
3:15 - 3:40 p.m.	Coffee Break	Ballroom Pre-function Area

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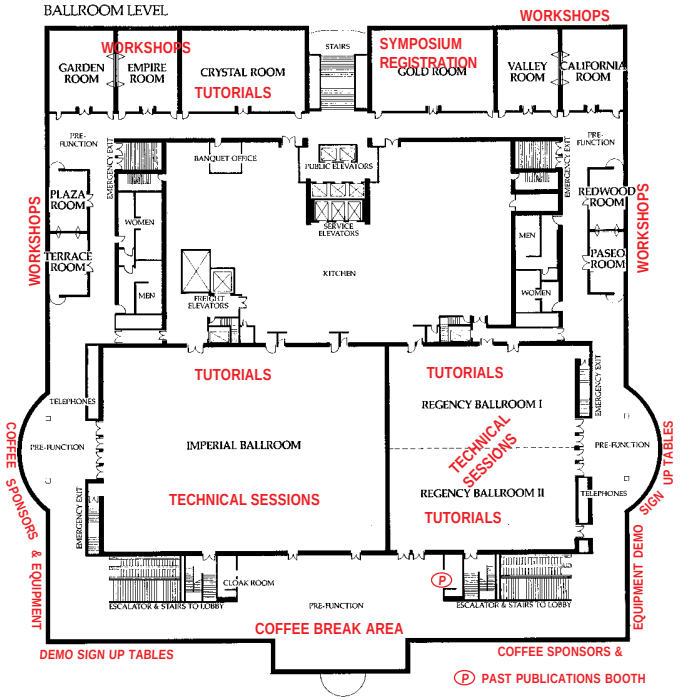
- **Market & San Pedro Street Garage**
  between Santa Clara and St. John Streets
- **Third Street Garage**
  between Santa Clara and St. John Streets
- **Second & San Carlos Street Garage**
  between Second & third Streets, north of San Carlos & next to Camera Cinemas
- **Market & San Carlos Street Surface Lot**
  on the corner, across from the Hyatt Sainte Claire

(continued)



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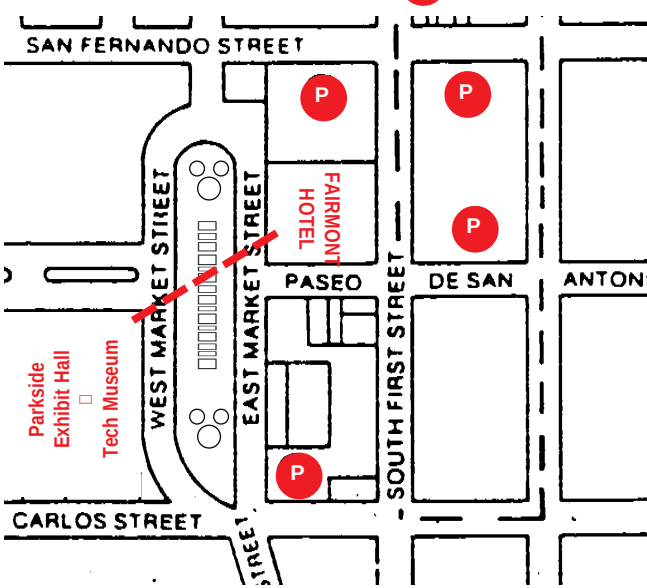

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